SAR ADC’s and Delta Sigma ADC’s:
Different Architectures for Different Applications
## Selecting ADC Topology

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SAR vs. Delta-Sigma

What is the ADC actually converting?

SAR ADC takes “snapshots”
Each conversion command captures the signal level, at that point in time, onto the sample/hold

ΔΣ ADC calculates an average
The signal is sampled continuously
How does the ADC control happen?

- SAR conversions have Start Conversion Signal
- Delta-Sigma is always sampling/converting
How Does a SAR ADC Work?

- Similar to a balance scale
How Does a SAR ADC Work?

• Similar to a balance scale
How Does a SAR ADC Work?

• Similar to a balance scale
How Does a SAR ADC Work?

• Similar to a balance scale

The MSB is determined first

MSB

1

1/2 1/4
How Does a SAR ADC Work?

• Similar to a balance scale

The test is repeated for each Binary weighted bit
How Does a SAR ADC Work?

• Similar to a balance scale

The LSB is determined last

MSB | Mid | LSB
1 | 0 | 1

1/2
Typical Topology of a SAR ADC

- $V_{IN}$
- $S_1$
- $S_2$
- C
- SAR
- Data Output Register
- N-bit Search DAC
SAR ADC Acquisition Phase

- **V_{IN}**
- **SAMPLE & HOLD**
- **DAC**
- **COMPARATOR**
- **V_{IN}**
- **S_{1}**
- **S_{2}**
- **C**
- **N-bit Search DAC**
- **Data Register**
- **SAR**
SAR ADC Acquisition Phase

- **V** IN
- **DAC**
- **COMPARATOR**
- **V** CS H(t)
- **V** SH0
- **V** IN
- **C**
- **S**1
- **S**2
- **SAR**
- **Data Register**
- **N-bit Search DAC**

1/2 LSB

**Graph:**
- **V** IN
- **V** CS H(t)
- **V** SH0
- **t**0
- **t**AQ
- **Time**

**Texas Instruments**
SAR ADC Acquisition Phase

\[ V_{CSH}(t) = V_{CSH}(t_0) + [V_{IN} - V_{CSH}(t_0)] \times (1 - e^{-\frac{t}{\tau}}) \]

\[ \tau = R_{S1} \times C_{SH} \]
SAR ADC Conversion Phase

Digital Output Code = 10100
SAR ADCs

- Very Popular Topology
- Attractive in “Point in Time” or Multiplexed Measurements
- Advantages
  - “no latency”
    - input is sampled once
    - “balancing” done internally
  - good tradeoff between speed, resolution and power
- Speed: DC to 4MSPS
- Resolution: 8 to 18 bits; and moving towards higher resolutions
- TI Part Numbers:
  - ADS7xxx
  - ADS8xxx
Delta Sigma Topology

Analog Input \(\sim\) Delta Sigma Modulator \(\rightarrow\) Digital Filter \(\rightarrow\) Decimator \(\rightarrow\) Digital Output
Delta Sigma Topology

Delta Sigma Modulator

SAMPLING RATE (Fs)

Analogue Input
(Samples at High Frequency)

High frequency, 1 bit PCM data stream

Digital Filter

Decimator

Digital Decimating Filter

Digital Output
Delta Sigma Topology (3)

Input Oversampling

High frequency, 1 bit PCM data stream

Lower data rate, very high resolution digital output
Oversampling

Ideal N-Bit ADC
SNR = 6.02N + 1.76 dB

Average Noise energy distributed from DC to fs/2
On a Delta-Sigma Converter, the analog input is sampled at a Frequency much higher than the Nyquist rate.

Ideal N-Bit ADC

\[ \text{SNR} = 6.02N + 1.76 \text{ dB} \]

Average Noise energy distributed from DC to \( \frac{fs}{2} \)

Digital Low Pass filter

\[ \text{SNR} = 6.02N + 1.76 \text{ dB} + 10 \log(\text{OSR}) \]

Average Noise energy distributed over a wider range from DC to \( K \frac{fs}{2} \)
Delta Sigma Modulator

Analogue Input

Digital Filter

Delta Sigma Modulator

Decimator

Digital Decimating Filter (usually implemented as a single unit)

Digital Output
First Order Delta-Sigma Modulator

Noise Shaping

\[ A(f) = \frac{1}{f} \]

Input Signal \( X_i \)

\[ \sum \]

Integrator (Low-Pass)

\[ Y_i \]

Quantization Noise \( e_i \)

1-Bit ADC

1-Bit DAC
First Order Delta-Sigma Modulator

Noise Shaping

\[ Y = (X - Y) A(f) + e(n) \]  \hspace{1cm} (1)

\[ Y = e(n) \left( \frac{f}{1 + f} \right) + X \left( \frac{1}{1 + f} \right) \]  \hspace{1cm} (2)
First Order Delta-Sigma Modulator

Noise Shaping

$$Y = (X - Y) A(f) + e(n)$$  \hspace{1cm} (1)

$$Y = e(n) \left( \frac{f}{1 + f} \right) + X \left( \frac{1}{1 + f} \right)$$  \hspace{1cm} (2)
First Order Delta-Sigma Modulator

Noise Shaping

Modulator Output:
TIME DOMAIN

Believe it or not, the sine wave is in there!
(drawing is approximate)
First Order Delta-Sigma Modulator (5)
Noise Shaping

**Modulator Output:**
TIME DOMAIN

Believe it or not, the sine wave is in there!
(drawing is approximate)
First Order Delta-Sigma Modulator

Noise Shaping

Modulator Output:
TIME DOMAIN

Believe it or not, the sine wave is in there!
(drawing is approximate)

Modulator Output:
FREQUENCY DOMAIN

Signal

0
Believe it or not, the sine wave is in there!
(drawing is approximate)

Quantization Noise

SIGNAL

Fs
Higher Order Delta-Sigma Modulators

- First Order ΔΣ Modulator
- Second Order ΔΣ Modulator
- Third Order ΔΣ Modulator

Frequency vs. $F_S$
Delta-Sigma A/D Signal Path

Analog Input → Delta Sigma Modulator → Digital Filter → Decimator → Digital Output

Digital Decimating Filter
(usually implemented as a single unit)
Modulator Noise Shaping and Digital Filter

Modulator Noise Shaping

Frequency

$F_S$
Modulator Noise Shaping and Digital Filter

ΔΣ Modulator Noise Shaping
Modulator Noise Shaping and Digital Filter

Filter set by Oversampling Ratio

$\Delta \Sigma$ Modulator Noise Shaping

Frequency $F_S$
Digital Filter

- Digital filter architecture determines overall ADC response.
- Common filters: “Sinc” and “Flat Passband”
Sinc Digital Filter

- Typically used for DC measurements, or slow moving signals

**Advantages**
- Economical silicon area, easy to implement
  - Low cost
  - Low power
- Low latency
- Filter notches can target specific frequencies (ex. 50/60 Hz)

**Disadvantages**
- Pass band signal droop
- Weak Stop band attenuation for low-order Sinc filters
Sinc Digital Filter Settling

Settling time for an input step change, Sinc³ filter
Need n cycles to settle for a Sinc^n filter

Uncertainty of Analog Edge → 4 Data Cycles

Fdata periods
Analog Inputs

3 full cycles
3 full cycles

Valid data
Valid data

4 cycles
Delta Sigma: Zero Cycle Latency

- Zero cycle Latency =
  - Zero latency
  - Single cycle conversion
  - Single cycle settling
  - No Latency

Analog IN

Data OUT
Delta-Sigma: Zero Cycle Latency

- Zero cycle Latency =
  - Zero cycle latency
  - Single cycle conversion
  - Single cycle settling
  - No Latency

Analog IN

Data OUT

"Hidden Conversions"
Flat Pass Band Filter

Advantages

• Frequency Response
  • Very low ripple pass band
  • Sharp Nyquist transition band
  • Large stopband attenuation: lower than -100dB (simplify aliasing requirement)

• Frequency response scalable with master clock

Disadvantages

• Large area – Costly
• Higher-order / high-tap filter – large latency
• The latency of the filter depends on the number of delay blocks used
• Flat Passband filters require a lot delay blocks to maintain desired AC response
• Many Delta-Sigma Converters incorporate filters with programmable settings:
  – Optimize for lower latency, power consumption or for AC performance/higher resolution
ΔΣ ADCs: Simplifying the Signal Chain

Sensor

Signal Conditioning and Protection

Gain Stage

In

R1

R2

Out

MUX

ADC Drive Circuitry

ADC

Processor

Iso

MCU
Delta-Sigma ADCs integrate many signal chain elements into one device.
Delta-Sigma ADC’s

- Highest Resolution and High Stability with moderate power consumption
- Incorporate a Digital Filter
- Frequency Response, and Latency dependent on Digital Filter
- Typically Highly Integrated devices:
  - Digital Filter, Buffer, PGA, MUX, Vref, Calibration/diagnostics
- Typically Requires Configuration of Registers
SAR ADCs

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More Precision ADC Information

Precision ADC Web Page: [www.ti.com/precisionadc](http://www.ti.com/precisionadc)
- Data Sheets & Technical Reference Manuals
- Application Notes
- Software, Tools & SPICE Model Downloads
- Order Evaluation & Performance Demonstration Kits

PA SAR ADC E2E™ Support Forum: [www.ti.com/precisionadcsupport](http://www.ti.com/precisionadcsupport)
- Ask Technical Questions
- Search for Technical Content

Precision HUB Blog Series: [e2e.ti.com/blogs_/b/precisionhub](http://e2e.ti.com/blogs_/b/precisionhub)
Tips, tricks and techniques from TI precision analog experts

TI Designs - Precision: [www.ti.com/precisiondesigns](http://www.ti.com/precisiondesigns)
- Reference Designs
- Board Schematics & Verification Results