TI mmWave Sensors
IWR14xx/16xx Device Overview
Agenda

• Device Overview
  – TI mmWave sensor portfolio
  – IWR1xx Signal processing chain
  – Example System topologies

• Functional Blocks
  – Device Block Diagram
  – RF and Analog Subsystem
  – Radar Subsystem (aka BSS or BIST Subsystem)
  – Master Subsystem (MSS)
  – DSP Subsystem (DSS: IWR16xx only)
  – Radar Hardware accelerator

• Boot modes

• Software Platform
Device Overview
mmWave Sensors – 76-81 GHz Portfolio

**mmWave Sensor + HW Accelerator**

- **Use Case**
  - Satellite Sensor with MCU
    - 4X IWR14 + Central Processor
    - 2X IWR14 + Central Processor
  - Entry-level Single-chip Sensor
    - Power-optimized applications
    - HW acceleration for limited processing

**mmWave Sensor + DSP**

- **Use Cases**
  - Full functionality single-chip radar
    - Increased on-board memory for higher range and resolution measurement
    - On-chip DSP for advanced algorithms
Key Features

- FMCW Radar transceiver with 76-81 GHz operating frequency with 4 GHz chirp bandwidth
- MIMO: Up to three transmitter and four receiver chains
- Programmable, flexible chirp profiles for both long and short range sensing in the same radar frame
- 200MHz ARM Cortex R4F MCU for user application processing
- Radar Hardware accelerator for FFT and CFAR processing (14xx only)
- C674x DSP for FMCW signal processing and advanced tracking, clustering and object classification (16xx only)
- Continuous monitoring and calibration of Analog/RF through a second dedicated Cortex R4F MCU
- CAN support for ECU Interface
- QSPI Serial Flash support for autonomous boot
- MIBSPI, SPI, I2C, and UART Serial Interfaces Support
- CSI2 (IWR14xx only) and LVDS interfaces for high speed raw data transfer
IWR1xxx mmWave Signal Processing

- RF Front-End
  - ADC
  - ADC Data
  - Pre-Processing (Interference Mitigation)
  - 1st Dim FFT (Range)
  - 2nd Dim FFT (Velocity)
  - Detection (CFAR)
  - 3rd Dim FFT (Angle Arrival)
  - Point Cloud [Range, Velocity, Angle]
  - Clustering
  - Tracking
  - Object Classification
  - Objects

IWR1443
IWR1642
Example System Topologies

**Fluid Level Sensing**

- MSP432
- IWR14xx
- SPI
- 2-Wire, IO-Link, CAN

**Transport and Mobile Robots: Front-View and Landing**

- DM5xx
- AM437x
- FPGA
- SPI

- IWR16xx
- IWR14xx
Example System Topologies

Transport and Mobile Robots: Surround Sensing

Traffic Monitoring

DM5xx
AM437x
FPGA

IWR16xx
IWR14xx

SPI

IWR16xx
IWR14xx

SPI

IWR16xx
IWR14xx

SPI

SPI

SPI

DM8127

Ethernet

IWR16xx
IWR14xx

SPI
Functional Blocks
Block Diagram: IWR14xx/IWR16xx

- RX x4
- TX x2
- Crystal
- Oscillator

**Radar SS**
- DFE
- GPADC Buf
- FFT Engine

**RPT/Analog SS**
- LNA
- ADC

**Decimation Filters chain**
- AGC/DC est
- Cleanup PLL
- GPADC

**Master SS**
- STC
- Cortex R4F
- DRAM
- PRAM
- Boot ROM
- DMAx2
- MailBox
- CRC
- Encryption

**DSP SS**
- C674x
- L1P
- L1D
- UMC
- EMC
- L2 RAM
- L3 RAM
- EDMAX4
- Ramp gen
- RTI/WD, TIMER

**Development Interface**
- Cortex R4F
- RAM
- DMA
- Uart4

**Handshake RAM**
- Handshake RAM1
- Handshake RAM2

**Development Interfaces**
- Handshake RAM
- ESM
- SPI/I2C
- SPI
- UART1, 2, 3
- RTI/WD, TIMER
- CSI2

**Cryptography**
- CRC

**Safety MCU/PMIC**
- SPI
- SPI
- UART1, 2, 3
- RTI/WD, TIMER
- CSI2

**Flash Interface**
- SPI

**Sync**
- SPI

**High speed raw data**
- RTI/WD, TIMER

**Safety MCU**
- SPI
- SPI
- UART1, 2, 3

**Development Interfaces**
- Cortex R4F
- DMA
- Uart4

**Crypto**
- CRC

**Handshake RAM**
- Handshake RAM1
- Handshake RAM2

**Testing**
- Test/Debug

**Development Interface**
- Temp
- VMON

**JTAG/Trace**
- nReset

**HIL**
- MDO

**Test/Debug**
- Temp
- VMON

**Development Interface**
- Cortex R4F
- DMA
- Uart4

**RTI/WD, TIMER**
- RTI/WD, TIMER

**ESM**
- SPI
- SPI
- UART1, 2, 3

**Safety MCU**
- SPI
- SPI
- UART1, 2, 3

**Development Interfaces**
- Cortex R4F
- DMA
- Uart4

**Handshake RAM**
- Handshake RAM1
- Handshake RAM2

**Development Interfaces**
- Cortex R4F
- DMA
- Uart4

**Testing**
- Test/Debug

**Development Interface**
- Cortex R4F
- DMA
- Uart4
Block Diagram: IWR14xx/IWR16xx

- RX x4
- TX x2
- Crystal
- LNA
- ADC
- Decimation Filters chain
- AGC/DC est
- Cleanup PLL
- Synth
- Chirp Gen
- X4
- Oscillator
- Radar SS
- DFE
- GPADC Buf
- FFT Engine
- Cortex R4F
- DMA
- Uart4
- Ctl Registers
- AVDD
- RVDD
- AVREF
- SAVDD
- RESET
- Master SS
- STC
- MDO
- CAN
- SPI/I2C
- QSPI
- SPI
- UART1,2,3
- RTI/WD, TIMER
- CSI2
- ESM
- DSP SS
- Handshake RAM1
- Handshake RAM2
- CRC
- RTI/WD, TIMER
- ADC buffers
- DMM
- LVDS
- HIL
- IOs
- Test/Debug
- Temp
- VMON
- TOP SS
- Development Interface
- JTAG/Trace
- MDO
- CAN
- Safety MCU/PMIC
- Flash Interface
- Safety MCU
- Development Interfaces
- Sync
- High speed raw data
- nError
- nReset
RF and Analog Subsystem
RF and Analog: Clock Subsystem

- Supports 40MHz crystal.
- Clean-up PLL provides high-frequency reference for modulated synthesizer and clocks to digital, ADCs.
- FMCW waveforms synthesized in a 19-20.25GHz closed loop frequency synthesizer.
RF and Analog: Transmit Subsystem

- Single-ended antenna interface matched to a 50 ohm GCPW on the PCB at the edge of the package.
- Power/impedance monitors at the edge of the die.
- Binary (0/180) phase modulation for MIMO radar and interference mitigation.

 ![Diagram of Transmit Subsystem](image)
RF and Analog: Receive Subsystem

- Complex (I/Q) baseband.
- Programmable high pass filters to compensate for channel loss.
- CTSDM ADC supports IF bandwidths up to 15MHz.
Radar Subsystem (aka BSS)
Radar Subsystem (BSS)

- Also known as the BSS, includes the DFE (digital front-end) and Ramp Generator
- Also includes a dedicated Cortex R4F MCU for configuration, monitoring, and calibration of the low-level RF/Analog components
- Access to the Radar subsystem provided through hardware mailboxes and a well defined API
Master Subsystem (MSS)
Block Diagram: IR14xx/IR16xx

- RX x4
- TX x2
- Crystal
- Oscillator
- DFE
- GPADC Buf
- FFT Engine
- Ctrl Registers
- Ramp gen
- RTI/WD, TIMER
- DMA
- Uart4
- Cortex R4F
- GPADC
- LNA
- PA
- ADC
- Decimation Filters chain
- AGC/DC est
- Cleanup PLL
- Cortex R4F
- Boot ROM
- DMAx2
- MailBox
- CRC
- CPR
- Crypto
- STC
- CAN
- SPI/I2C
- SPI
- UART1,2,3
- RTI/WD, TIMER
- CSI2
- ESM
- Handshake RAM1
- Handshake RAM2
- CRC
- RTI/WD, TIMER
- ADC buffers
- DMM
- LVDS
- HIL
- MDO
- Temp
- VMON
- IOs
- Test/Debug
- JTAG/Trace
- Development Interface
- nReset
- Automotive Interface
- Safety MCU/PMIC
- Flash Interface
- Safety MCU
- Development Interfaces
- Sync
- High speed raw data
- nError
Master (Control) Subsystem

- The MSS includes an ARM Cortex R4F processor clocked at 200 MHz for running application code.
- User application running on MSS controls overall operation of the device, including Radar subsystem (BSS) control via well-defined API messages and perform radar signal processing.
- This subsystem also includes the various external interfaces available on the 14 or 16xx devices.
DSP Subsystem (DSS)
Block Diagram: IWR14xx/IWR16xx

- **RX x4**
- **TX x2**
- **Crystal**
- **Oscillator**
- **Radar-SS**
  - DFE
  - GPADC Buf
  - FFT Engine
  - C674x
  - Cortex R4F
  - Ramp gen
  - RTI/WD, TIMER
- **RPI/Analog-SS**
  - LNA
  - ADC
  - Decimation Filters chain
- **Cleanup PLL**
- **Chirp Gen**
- **AGC/DC est.**
- **PA**
- **STC**
  - Cortex R4F
  - DRAM
  - PRAM
  - Boot ROM
  - DMAx2
  - MailBox
  - CRC
  - Cleanup PLL
  - GPADC
  - Ramp gen
  - RTI/WD, TIMER
- **C674x**
  - L1P
  - L1D
  - UMC
  - EMC
  - L2 RAM
  - L3 RAM
  - EDMAx4
- **CRC**
- **DMM**
- **RTC/WD, TIMER**
- **SPI/I2C**
- **QSPI**
- **SPI**
- **Uart1,2,3**
- **SPI**
- **ESM**
- **Handshake RAM1**
- **Handshake RAM2**
- **Flash Interface**
- **Development Interfaces**
- **Sync**
- **High speed raw data**
- **nError**
- **Automotive Interface**
- **Safety MCU/PMIC**
- **Safety MCU**

- **TOP-SS**
  - DMA
  - Uart4
  - I/Os
  - Test/Debug
- **MDO**
- **HIL**
- **I2C**
- **JTAG/Trace**
- **Temp**
- **VMON**
- **nReset**
- **Texas Instruments**
DSP Subsystem (DSS): IWR16xx only

- C674x DSP clocked at 600 MHz for advanced Radar signal processing
- High bandwidth interconnect for high performance (128-bit, 200MHz)
- 256 KB L2 and 1 MB of L3 memory
- Four DMAs for data transfer, LVDS interface for Measurement data output, ADC buffers, CRC engine and data handshake memory
Radar Hardware Accelerator
Radar Hardware Accelerator

• Accelerates FFT and CFAR detection operations
• Simple pre-FFT processing and Magnitude and Log-Magnitude computation capability
• Flexible data flow and data sample arrangement to support efficient multi-dimensional FFT operations and transpose accesses
• Chaining and Looping mechanism to sequence accelerator operations with minimal intervention from the main processor
• CFAR-CA detector support (linear and logarithmic)
Boot Modes
Boot Modes

**Flashing Mode:**
- Bootloader enables the UART driver
- Expects a data stream comprising of User Application (Binary Image)
- Loads data to appropriate sections of the serial FLASH

**Functional Mode:**
- Bootloader looks for a valid image in the serial flash memory, interfaced over the QSPI port.
- Bootloader transfers the same to Master System’s memory sub-system
Software Platform
**mmWave Software**

**Simplified evaluation and development**

**mmWave SDK**

- **Includes:**
  - TI RTOS
  - Drivers
    - SPI
    - CAN
    - LVDS / CSI-2
    - EDMA
    - UART
    - I2C
    - GPIO
    - Timers
    - FFT HW
  - Signal Processing Library
    - On DSP
    - On HW Accelerator
  - mmWaveAPI
  - mmWaveLink
  - mmWaveLib

**mmWave Examples**

- **TI Designs:**
  - Power-Optimized Field Transmitter
  - Traffic monitoring

- **Examples:**
  - mmWaveDemo (OOB)

- **Labs:**
  - Water Vs Ground Lab
  - Vital Sign Lab

**mmWave Studio**

- **Includes:**
  - System Estimator – define chirp configuration through abstracted parameters like max range, minimum range, etc
  - Capture – capture raw ADC data from capture HW onto the PC
Simplified mmWave sensor configuration

• Generate mmWave sensor chirp configurations through system-level parameters to control [Range, Velocity, Angle] output
• mmWave OOB GUI for visualization of the output

<table>
<thead>
<tr>
<th>Customer Inputs</th>
</tr>
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<tbody>
<tr>
<td>Maximum Range</td>
</tr>
<tr>
<td>Minimum Object Size</td>
</tr>
<tr>
<td>Minimum Range / Resolution</td>
</tr>
<tr>
<td>Frame Rate</td>
</tr>
<tr>
<td>Maximum Velocity</td>
</tr>
<tr>
<td>Sensitivity</td>
</tr>
<tr>
<td>Minimum Velocity / Resolution</td>
</tr>
<tr>
<td>Field of View</td>
</tr>
<tr>
<td>Device (IWR14x vs IWR16x)</td>
</tr>
<tr>
<td>Frequency Band</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Internal RF Chirp Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Range FFT Size</td>
</tr>
<tr>
<td>Doppler FFT Size</td>
</tr>
<tr>
<td>Chirp Duration &amp; Ramp Slope</td>
</tr>
<tr>
<td>Chirp Bandwidth</td>
</tr>
<tr>
<td>Chirp Ramp Slope</td>
</tr>
<tr>
<td>...</td>
</tr>
<tr>
<td>+40 other parameters</td>
</tr>
</tbody>
</table>
mmWave SDK – The TI components

mmWave SDK
- Modular design
- Well defined APIs
- Documentation – doxygen, release notes, user guide
- MISRA-C compatibility for all foundational components
- Applicable for IWR1443/IWR1642

RTOS Drivers
- Encapsulate the functionality of the hardware IPs in the SOC
- Provide a well defined API to the higher layers.
- OS-agnostic via the OSAL layer

OSAL
- An abstraction layer for some of the common OS services. (Semaphore, Interrupts, Clock)
- Sample TI RTOS based port in mmWaveSDK
- Customers can port the OSAL for their custom OS, as per their requirements

BSS Firmware
- ROM Firmware for mmWave Front End
- Provides well defined APIs to configure, start and monitor mmWave Front End
- Communicates with MSS via Mailbox and proprietary protocol

mmWaveLink
- Low level control for mmWave Front End
- Communicates over Mailbox to BSS (front end)
- Implements the communication protocol between the BIST subsystem and Master subsystem

mmWave API
- Simple APIs for application to perform the task of radar sensing
- High level control for mmWave Front End and DSS
- Runs on top of mmWaveLink/IPC and Drivers.

mmWaveLib
- Provides functions for elements or sub functions of typical radar processing chain
- Optimized for C674x
- Accelerate customer code development and reduce SW effort to achieve a working radar processing chain
mmWave SDK - Packaging

Source Code

- common
- demo
- OOB demo

- drivers
- <drivers>
- osal
- soc
- pinmux

- control
- mmWaveLink
- mmWaveApi
- mmWaveLib

- alg
- platform
- ccs
- flash

- utils

- docs
  - Release Notes
  - User Guides

- bin
  - BSS Firmware

- • Uses TI compiler tools (Cortex-R4F, C674X) provided as part of CCS
  - Demo built over TI RTOS
  - Simple makefile based build system
Learn more about Industrial mmWave Sensors

• Learn more about IWR1x devices, please visit the product pages

• Get started evaluating the platform with IWR1x EVMs, purchase EVM at

• Download mmWave SDK @ [http://www.ti.com/tool/MMWAVE-SDK](http://www.ti.com/tool/MMWAVE-SDK)

• Ask question on TI’s E2E forum @ [http://e2e.ti.com](http://e2e.ti.com)