Clocking and time synchronization challenges in real-time Ethernet

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• Career
  – Earned electrical engineering degree (Dipl. Ing. (FH)) at the University of Applied Sciences in Wiesbaden, Germany.
  – System engineer in the factory automation and control team with focus on industrial communication and industrial PC at Texas Instruments in Freising/Germany.

• Expertise
  – Responsible for developing reference design solutions for the industrial segment.
  – Extensive experience in industrial communications like Industrial Ethernet and fieldbuses and industrial applications.
  – System expert for PRU-ICSS block on Sitara processors
  – Synchronization and clocking over industrial Ethernet.
Agenda

• Introduction
  – Importance of clock synchronization in real-time Ethernet
  – Application examples for clock synchronization
• Fundamental
  – Key parameters for clock synchronization
  – Industrial Ethernet protocols
  – Jitter and delay sources in industrial Ethernet
  – Clocking technologies
• Synchronization in industrial Ethernet
  – Timestamping methods
  – Synchronization with IE protocols
• Summary & Outlook
Introduction

Why is clock and time synchronization in real-time Ethernet getting important?
Introduction

What is clock and time synchronization in factory automation?

- Synchronize tasks and events over PLCs, sensors, actuators, drives and remote I/Os.
- Clock master provides reference time.

Synchronization examples

- Diagnostics data over multiple devices.
- Common measurements across multiple sensors.
- Synchronize the position and speed of conveyer belts.
- Synchronize sensors, actuators, motor drives in printing machines.

Industrial communication protocols

- Serial fieldbus: CAN, RS-485, PROFIBUS.
- Ethernet: std. Ethernet, EtherCAT, PROFINET, Sercos, Ethernet/IP, HSR/PRP, TSN.
- Synchronous Ethernet (SyncE).
Industrial Ethernet standards overview

Top Ethernet based standards:

• Profinet RT/IRT
  – Factory automation including drives, strong in Europe.

• EtherCAT:
  – Large IO systems and drives, getting momentum in Asia.

• Ethernet/IP
  – IEEE compliance, CIPSync for drives, strong in process automation.

• Sercos III
  – Optimized technology for drives, supports network redundancy via ring topology.

• Powerlink
  – Open technology, popular in inverters, strong in China.

• Time Sensitive Network (TSN)
  – 802.1Q defined technology to provide deterministic messaging on standard Ethernet.
### Industrial Ethernet vs. standard Ethernet in factory automation

<table>
<thead>
<tr>
<th>Industrial Ethernet</th>
<th>Standard Ethernet</th>
</tr>
</thead>
<tbody>
<tr>
<td>deterministic</td>
<td>best effort</td>
</tr>
<tr>
<td>exchange of process data, diagnostic, IP</td>
<td>exchange of anything (video, files, web-server)</td>
</tr>
<tr>
<td>PLC, remote I/O, sensor, actuator, drives</td>
<td>PC, printer, modem, Internet</td>
</tr>
<tr>
<td>plant floor, factory automation</td>
<td>office, back-end</td>
</tr>
<tr>
<td>on-the-fly or cut-through frame handling</td>
<td>store-and-forward frame handling</td>
</tr>
<tr>
<td>specialized MAC implementation</td>
<td>standard Ethernet MAC in every PC</td>
</tr>
<tr>
<td>error handling in MAC</td>
<td>error handling in layer 3 and above</td>
</tr>
<tr>
<td>signal immunity, harsh environment</td>
<td>consumer environment</td>
</tr>
<tr>
<td>managed frame exchange</td>
<td>non-managed frame exchange, frame collisions</td>
</tr>
</tbody>
</table>
What is Synchronization?

• When Network nodes boot up, they have different local time.
• Synchronization is the process after which all node local times follow the master clock.
• Simply sending information about master time is not enough. Why?
• Accuracy is the residual error after synchronization (Δ).
• Even with the same clock frequency, drift will affect the accuracy. So synchronization must be repeated frequently.
Application examples

Applications that require sub-micro second synchronization

- Motion control: newspaper printing: 4 µs (relative time).
- Laser cutting and marking machines: <100ns (relative time).
- Electrical substations: differential protection: 10 µs (absolute time).
- Electrical grids: wide area protection: 1 µs (absolute time).
- Drive (GTO, IGBT firing): 1 µs (relative time).

Accuracy of typical time synchronization protocols:

- SNTP: 10’000 µs accuracy.
- PTP: 1 µs.
- GPS / Galileo: 0,1 µs accuracy.
Basics of time synchronization, NTP, PTP and time stamping
Time synchronization foundation

- Two delay paths must be calculated, the Master to Slave and the Slave to Master.
- T1 is the precise time of the sync message from the Master. This timestamp is sent in the follow-up message since the time of T1 was sampled when the sync message was transmitted on the Ethernet port.
- T2 is the precise time of the sync message as it is received at the Slave.
- Master to Slave difference = T2 - T1.
- T3 is the precise time of the delay request message from the Slave.
- T4 is the precise time of the delay request message when received at the Master.
- Slave to Master difference = T4 - T3.
- The one-way delay can be calculated once the Master to Slave and Slave to Master difference is available at the Slave.
  - One way delay = (Master to Slave difference + Slave to Master difference) / 2
- Clock Offset = Time Slave − Time Master + One way delay.
- Assumes medium symmetry.
Time stamping methods for time synchronization

- Time stamping: read out a timer when a receive or transmit frame event occurs.
- Software time stamping
  - Function to read out timer upon a receive or transmit event:
    - Software jitter, interrupts, latency: millisecond accuracy.
- Hardware time stamping
  - Hardware takes timestamp, software processes the synchronization process.
  - MAC or PHY
    - Start of frame (SOF → preamble starts).
    - Start frame delimiter (SFD).
  - PHY: dedicated pin, which needs to get connected to a timer peripheral input (processor, FGPA, ASIC).

<table>
<thead>
<tr>
<th>Preamble</th>
<th>Start of frame delimiter</th>
<th>MAC destination</th>
<th>MAC source</th>
<th>802.1Q tag (optional)</th>
<th>Ethertype (Ethernet II) or length (IEEE 802.3)</th>
<th>Payload</th>
<th>Frame check sequence (32-bit CRC)</th>
<th>Interpacket gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 octets</td>
<td>1 octets</td>
<td>6 octets</td>
<td>6 octets</td>
<td>(4 octets)</td>
<td>2 octets</td>
<td>46-1500 octets</td>
<td>4 octets</td>
<td>12 octets</td>
</tr>
</tbody>
</table>
**Timestamping error sources**

- Inaccuracy of the timestamping itself
  - Software vs MAC / PHY Timestamping
  - Transmit or receive timestamp doesn’t correspond exactly to the time when the packet was actually sent or received by the MAC when using SW timestamping.

- On a HLOS (e.g. Linux), there are three different places where the timestamps can be generated
  - User space (i.e. the NTP/PTP daemon), typically before making a send() system call and after a select() or poll() system call.
  - Kernel, before the packet is copied to the NIC ring buffer and when the NIC issues an interrupt after receiving a packet. This is called software timestamping.
  - In the MAC itself, when the packet enters and leaves the link or physical layer. This is called hardware timestamping.
Key components influencing clock synchronization

- Clock and time synchronization dependent on a combination of components working together:
  - Analog components
    - Ethernet PHY (RX/TX latency, SOF timestamping (TS)).
    - Oscillators (jitter, accuracy over time and temperature).
    - Clock distribution devices.
  - Processor components
    - Media Access Controller (MAC).
      - RX/TX FIFOs, data path synchronization.
      - SOF time stamping.
    - Processor / ASIC / FPGA
      - Timer peripheral.
      - Software, firmware, RTOS, HLOS, tasks, interrupts, memory access, TS, timer.
  - Cable length (latency)
  - Type of synchronization software.
Types of synchronization

- Free running master/slave clocks have not the same frequency. The frequency will slightly change and the phase is unknown
  - Time synchronization: Getting clocks or a timer to run at the same time of day, hour, minute, second, microsecond, ...
  - Frequency synchronization: Getting clocks to run in the same rate.
  - Phase synchronization: Getting frequency synchronized clocks to run in phase.
Definition of Jitter, latency in industrial applications

- “Real-time” does not refer to “fast”!
- Cycle time is equidistant and deterministic.
- Latency, jitter, minimum, maximum.
- Worst case latency = determinism.
- The term “real-time” is senseless without setting a deadline for the given system.
- Soft real-time
  - Occasional violation of deadline is acceptable.
- Hard real-time
  - Each single violation of deadline is equal to a software error and must be handled by an exception routine.
- Industrial Ethernet requires hard real-time for many protocols.
Latency and jitter sources in industrial Ethernet

• Media Access Control (MAC)
  – Mode of operation: on-the-fly (<1 μs), cut-through (~3 μs), store-and-forward (minimal delay 6.7 μs; max 124μs).
  – MII/RMII/RGMII internal synchronization.
  – RX and TX FIFOs, start of transmission delay.

• PHY
  – Receive and transmit latency, MII/RMII/RGMII/SGMII dependent.

• Ethernet cable
  – About 500 ns delay per 100 m (CAT5 cable); cable asymmetry is nominally 25-50 ns/100 m.
Industrial Ethernet MAC and frame processing

• Media access controller (MAC)
  – Industrial Ethernet uses 3-port switch: Two physical Ethernet ports and one host port.
  – Specialized MAC is required for following frame handling methods.
  – MAC requirements depend on industrial Ethernet protocol and master/slave.

• Frame processing methods:
  – **On-the-fly**: Frame is forwarded to second Ethernet port; MAC can perform read and write access to the frame while its runs through MAC; CRC is updated to reflect frame modifications by MAC. Examples: EtherCAT, Sercos in RT channel.
  – **Cut-through**: Receives the Ethernet header, performs header analyzes and takes forwarding decision; frame is not modified by MAC. Examples: Profinet, Ethernet/IP, Powerlink, Sercos in UCC channel.
  – **Store and forward**: Legacy mode used by all standard Ethernet MACs; store frame in memory, perform header analyzes first before taking forwarding decision; frame is not modified by MAC.
Clocking technologies

• What subsystem need a clock?
  – MAC as part of the MPU, MCU, ASIC or FPGA.
  – Ethernet PHYs.

• Common source clocking vs. individual clocking
  – Individual clocking
    • Pro: Cheaper BOM when only few clocks are needed in the system.
    • Con: Ethernet PHYs and MAC operate with asynchronous clock source (25 MHz of PHY1 != 25 MHz of PHY2).
  – Common clocking
    • Pro: Cheaper BOM when multiple clocks are needed in the system.
    • Pro: Ethernet PHYs and MAC operate with synchronous clock source.
    – Some Industrial Ethernet protocols specify common clocking approach

• Clocking device solutions
  – Crystal and/or Oscillators
  – Clock Generator
  – Jitter Cleaners
Time synchronization methods used in industrial Ethernet
Why time synchronization in Industrial Ethernet

- Industrial Ethernet guarantees process data exchange between PLC and field devices within a specified cycle time.
- Synchronize tasks, input- and output events, diagnostic messages, motor drives over multiple field devices.
- Examples
  - External: Sync and latch signals.
  - Internal: PWM generation, events, diagnostics.
Synchronization protocols and methods overview

• Standard Ethernet Protocols
  – Network Time Protocol (NTP).
  – Precision Time Protocol (PTP) / IEEE 1588.

• Industrial Ethernet Protocols
  – EtherCAT distributed clocks
  – Profinet PTCP
  – Sercos
  – Ethernet/IP
  – HSR/PRP
  – TSN 802.1as

• Other synchronization protocols
  – SORTE time synchronization
  – Synchronous Ethernet

• Methods
  – Peer-to-peer or port-to-port
  – End-to-end

• MAC bridge delay
  – Cut-through delay and jitter
  – On-the-fly delay and jitter
## Industrial Ethernet Protocol time synchronization table

<table>
<thead>
<tr>
<th>Industrial Ethernet Protocol</th>
<th>Operation modes</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Network Time Protocol (NTP)</td>
<td>End-to-end</td>
<td>Internet</td>
</tr>
<tr>
<td>Precision Time Protocol (PTP) IEEE 1588</td>
<td>End-to-end, port-to-port</td>
<td>Internet and Intranet, adds jitter of forward delay from switches, hubs, …</td>
</tr>
<tr>
<td>EtherCAT Distributed Clock (DC)</td>
<td>End-to-end, cycle time based</td>
<td>1st slave is DC clock master, fixed bridge delay with min jitter</td>
</tr>
<tr>
<td>Sercos master sync telegram (MST)</td>
<td>End-to-end, cycle time based</td>
<td>Sercos master is clock master, fixed bridge delay with min jitter</td>
</tr>
<tr>
<td>PROFINET Precision transparent clock protocol (PTCP)</td>
<td>Port-to-port, 1588 based</td>
<td></td>
</tr>
<tr>
<td>Ethernet/IP CIP Sync</td>
<td>1588 based</td>
<td></td>
</tr>
<tr>
<td>HSR/PRP</td>
<td>1588 based</td>
<td></td>
</tr>
<tr>
<td>Time Sensitive Network (TSN) 802.1as</td>
<td>Port-to-port, 1588 based</td>
<td>Supports one-step-delay operation</td>
</tr>
<tr>
<td>SORTE</td>
<td>Port-to-port, cycle time based</td>
<td></td>
</tr>
<tr>
<td>Synchronous Ethernet</td>
<td>Physical clock distribution over Ethernet recovered clock for clock synchronization, time synchronization over 1588</td>
<td></td>
</tr>
</tbody>
</table>
Summary and Outlook
Customer application question checklist

- System understanding of the customer application that requires synchronization over Ethernet.
- Jitter and accuracy requirements.
- How does the customer specify his jitter and accuracy requirements, e.g. how to measure this?
- Industrial Ethernet protocol.
- Ethernet PHY.
- Ethernet MAC/processor/ASIC.
- Temperature requirements.
- Other subsystems on the board that needs or benefits clocking from a common source.
TI analog and embedded processing highlights

• Clocking devices
  – CDCE913 – clock generator
  – LMK05318 – Clocking generator/jitter cleaner with BAW

• Ethernet PHYs
  – DP83822 – 10/100 Mbit Ethernet PHY
  – DP83867/69 – 10/100/1000 Mbit Ethernet PHY
  – SOF pin for timestamping
  – Output receive clock on pin

• Processors
  – PRU-ICSS enable multi-protocol, cut-through and on-the-fly frame processing
  – Sitara AM335x/AM437x/AM57xx/AM65xx/K2G – PRU-ICSS enabled processors
Summary and outlook

✓ Clocking and time synchronization over industrial Ethernet challenges
  – Time, frequency and phase synchronization.
  – Jitter, delay.

✓ Jitter and drift challenges
  – Oscillator and clocking devices: accuracy, aging, temperature, shock.
  – PHY and cable delay.
  – MAC: path synchronization, FIFOs, frame processing.

✓ Software and hardware protocols
  – NTP, PTP, IEEE1588.
  – Industrial protocol specific methods.
  – Synchronous Ethernet (SyncE).

✓ Collect and share the synchronization and jitter requirements and challenges from your customer applications