Agenda

• FPD-Link Overview
  – General Features
  – In-vehicle Infotainment (IVI)
  – Advanced Driver Assistance Systems (ADAS)

• FPD-Link Features
  • Payload, Line Rate, Unit Interval explanation
  • Adaptive EQ
  • I2C Communication and Alias
  • Link Diagnostic
  • Power-over-coax (PoC)
  • Cable Requirement
  • CMLOUT Monitoring
  • Built-in-self Test (BIST) Mode

• Resources and Collateral

• Fault Analysis
FPD-Link III

Serializer / Deserializer

• Benefits:
  – Reduce cable harness cost and weight
  – Low EMI with differential LVDS
  – Diagnostics features

Replaces multiple interfaces (wires) with one pair

Video Data
Clock
I2C

SER

Forward Channel
(Video Data)

Bidirectional Control
Channel (BCC)

DES

Video Data
Clock
I2C
FPD-Link Application

**IVI:** In-Vehicle Infotainment

**ADAS:** Advanced Driver Assistance Systems

- 3D Surround View
- Rear View Camera
- Rear Cross Traffic
- Blind Spot Detection
- Lane Departure Warning
- Intelligent Headlamp Control
- Traffic Sign Recognition
- Forward Collision Warning
- Intelligent Speed Control
- Pedestrian Detection

**Infotainment Displays**

- **FPD-Link**
  - Automotive Cable
  - Point-to-Point

**ADAS Surround View Cameras**

- **FPD-Link**
  - Automotive Cable
  - Point-to-Point

**High-Speed - 6Gbps+**
**High-Resolution – 2K**
**Low-Latency - nano sec**
**Connections**

**Head-Unit**
FPD-Link Highlights

General
• Video, Bidirectional Control (I²C), GPIO and Power
  – Over single twisted pair or coaxial cable assemblies
• Adaptive equalization compensates for cable type, length, age and condition
• Multiple interface options: RGB, YUV, OpenLDI (LVDS), MIPI CSI-2, HDMI

Infotainment
• Support for 720p and 1080p
• Easy-to-use HDCP content protection
• Dithering, White Balance, and Test Patterns

Driver assist
• Support for 1 and 2 Megapixel image sensors
• Very low latency
• Internal Pattern Generator
• Temperature, PoC voltage Diagnostics
Adaptive Equalization

Automatic adaptation (no need to program EQ)
No EMI impact (because it is at the receiver)
Diagnostic function (can read EQ registers)
Multiple System Interface Options

- **Serializer**
- **Deserializer**
- **Processor**
  - Application Logic

### Interface Options:

1. **RGB Parallel LVCMOS**
   - LCD Module / Processor
     - Timing Controller or Application Logic
2. **HDMI**
3. **“OpenLDI”**
4. **“FPD-Link”**
5. **“LVDS”**
6. **mipi**
7. **CSI-2**
8. **Bridge**

Industry Standard I/Os
FPD-Link
Infotainment Applications

Connecting Head Units to Displays
IVI: In-Vehicle Infotainment
FPD-Link Portfolio by Display Resolution

**DS90UB901/2/3/4**
- QVGA: 320 x 240
- VGA/NTSC: 640 x 480
- PAL: 768 x 576
- SVGA: 800 x 600

**DS90Ux925/6/7/8**
- WVGA: 1024 x 600
- WSVGA: 1280 x 720
- XGA: 1024 x 768
- WXGA: 1280x768

**DS90Ux940/7/8/9**
- 1080p Full HD: 1920 x 1080
- 1080p HD: 1920 x 1080
- WUXGA: 1920 x 1200

High-definition hits the highway
World’s first SerDes chipset for 1080p automotive displays

Learn more at ti.com/pdp-link

Texas Instruments
© 2014 Texas Instruments Incorporated
FPD-Link products for infotainment displays

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- **RGB**
- **openLDI**
- **HDMI**
- **MIPI CSI-2**

Adaptive EQ
Backchannel
Coax support
HDCP Version avail.
I2S Audio
White Balance/Dith.
# FPD-Link IVI Features

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FPD-Link III 1080p60 Infotainment Family
System Interfaces

DS90Ux947
Serializer

DS90Ux948
Deserializer

DS90Ux949
Serializer

DS90Ux940
Bridge

Processor
Application Logic

Display

TCON

DS90Ux948
Deserializer

DS90Ux940
Bridge

Processor
Application Logic

LDI
LVDS

HDMI

mipi

CSI-2

Indstry Standard I/Os


dual Lane
FPD-Link III

†:
Conventional Single Lane FPD-Link III in backward compatible mode
(to and from DS90Ux92x devices)
What you need to know about high-speed cables for FPD-Link III SerDes

By T. K. Chin
Systems Manager, Ethernet and FPD-Link Product Line

Figure 1. Single-end and differential signaling topologies

(a) Differential transmission with unshielded differential cable

(b) Differential transmission with shielded differential cable

(c) Single-ended transmission with coaxial cable

DS90UB947/8A 2K Application

- Supports Pixel Clock up to 200 MHz for 2K
- 2880 x 1080p60
- Dual lane FPD-Link III
- Backward compatible to 720p generation (DS90Ux92x)
- High Speed Bidirectional GPIOs up to 2.5MHz in the back channel, OR
- SPI control interface up to 3.3Mbps in the backchannel
- I²C Control Interface up to 1MHz
FPD-Link ADAS Applications

Connecting High Resolution Cameras
Common Imager Resolutions

Analog Camera (CVBS)

- 800 x 480: WVGA
- 1280 x 720: 720p HD
- 1280 x 960
- 1920 x 1080
- 1920 x 1200: 1080p HD

1.0 - 1.2 - 1.3 Megapixels
2.0 - 2.3 Megapixels
FPD-Link ADAS Portfolio

Serializers
- 1.4 Gbps
  - 1 MP
    - 75 MHz CMOS/DVP
      - 913A

Deserializers
- 1.9 Gbps
  - 1.2 Gbps video
    - 100 MHz CMOS/DVP
      - 933 or
      - 934

- 4 Gbps
  - 2 MP
    - 4 Gbps video
      - 953
    - 3.2 Gbps video
      - 954

Deserializer Hub
- 6.4 Gbps
  - 960
  - 964

Adaptive EQ
Power-over-Coax
Dual Input
Replicate Mode
Synchronous Clocking
CSI-2 Virtual Channels
Advanced Diagnostics
Video Aggregation

Texas Instruments
SER/DES Companion Options for ADAS

FPD-Link III

- 953
- 933
- 913A
- 936
- 934
- 914A

Texas Instruments
SER/DES HUB Solutions for ADAS

FPD-Link III

913A

933

953

954

960

964

100 MHz
CMOS/DVP

75 MHz
CMOS/DVP

mipi CSI-2

CSI-2

mipi CSI-2

6.4 Gbps

6.4 Gbps

6.4 Gbps

6.4 Gbps

mipi CSI-2

mipi CSI-2

mipi CSI-2

mipi CSI-2

2ch

2ch

4ch

4ch
**DS90UB933/934**

**Features**
- Serializes 12 bits up to 100 MHz
- Ultra-low <25 us control channel latency
- On-chip internal oscillator for quick camera start-up
- Adaptive receiver equalization
- 1MP/60fps or 2MP/30fps

**Benefits**
- Supports higher resolution camera imagers
- Allows ISP function to be moved out of the camera to the ECU side, enabling smaller cameras and lowering thermal imager noise
- Cameras are ready quickly after starting car
- Compensates for cable degradation effects due to ageing and bending

**Applications**
- Automotive camera applications
- Satellite RADAR
- Industrial/medical imaging & security & surveillance

**Tools & Resources**
- Cable Characteristics & PoC App Notes
- EVM & Design Files
- ALP EVM Software GUI

**Device Datasheets:**
- DS90UB933-Q1
- DS90UB934-Q1
### DS90UB964

#### Features
- Aggregates up to 4 cameras up to 12 bits@100 MHz
- Dual MIPI CSI-2 output ports
- Virtual channel support tags cameras and exposures
- Ultra-low latency
- Adaptive receiver equalization compensates for cable ageing

#### Benefits
- Delivers video from 4 cameras to a single SoC video port
- Easily creates 2nd copy of video data for use in other video paths such as viewing (display) and data logging
- Separates multiple camera and exposure information so the SoC can easily distinguish this data
- Allows ISP function to be moved out of the camera to the ECU side, enabling smaller cameras and lowering thermal imager noise
- Cameras are ready quickly after starting car
- Compensates for cable degradation effects due to ageing and bending

#### Applications
- Automotive camera applications
- Satellite RADAR
- Industrial/medical imaging & security & surveillance

#### Tools & Resources
- TIDA-00455 Surround View Ref Design
- EVM & Design Files
- ALP EVM Software GUI
- Device Datasheets: DS90UB964-Q1
DS90UB953/954
2MP MIPI CSI-2 Ser/Des

- Supports 2MP image sensors with MIPI CSI-2 interfaces
  - Up to 4 data lanes and clock lane
  - YUV, RAW and RGB data types
  - High Speed, Low Power and Ultra Low Power modes
- Receiver-side clocking ensures all cameras are synchronous
- No 953 register writes if control channel errors present
- Reads Power-over-Coax (PoC) input voltage & internal temp
- Easier PoC support, smaller inductors
- Forward and back channel CRC
- 954 has 2 independent camera “hub” inputs and output replicate mode
- Small footprint (36 QFN) enables compact camera module design
DS90UB953/954 – Flexible Interfaces

Single 2MP camera example

Output replicate mode example

Dual camera example
DS90UB960/964
4:2 Camera Deserializer Hub

- Aggregates up to four 2MP cameras
  - Full 2MP HD & 60fps support
  - Coaxial or single differential pair
- 2x 6.4 Gbps MIPI CSI-2 output ports
  - Flexible mapping of cameras to port(s)
  - Aggregate & replicate modes
- CSI-2 virtual channel support
- (960) had Synchronous clocking mode with 953

- Programmable frame sync generator
- Adaptive Receiver Equalization
- 2x I2C ports up to 1MHz
  - Program 2 cameras using both I2C buses or multiple cameras using I2C broadcast
- 8 GPIOs
- Compatible with 953, 933, & 913A serializers
  - 964 version supports 933/913A only
Clock Source Selection

Figure 9. Clocking System Diagram
Frame Synchronization

1. **Synchronous**: Back Channel Synchronous Clock extracts a clock reference from the bidirectional communications link back channel, and internal PLLs generate the required clocks. This mode locks multiple sensors frequencies to a central clock domain.
   - The DS90UB953-Q1 generates a programmable reference clock for the image sensor.
   - The back channel clock rate is determined by the reference clock that is being provided to the deserializer.

2. Non **Sync** CSI_CLK: CSI Clocking uses the CLK signal at the CSI interface as the clock reference for the FPD output stream.
   - External onboard reference clock to the camera is required
   - 953 uses the CSI-CLK as the clock source for the FPD link data
   - 953 FPD rate is proportional to the CSI clock rate
   - Back channel speed must be below 10-Mbps (Manchester) rate
   - AC Cap of 0.1 μF is required

3. Non **Sync** CLK_IN: External Clock Reference uses an external oscillator as a reference and generates the required clock for the FPD forward channel for that reference.
   - External onboard reference clock is required to provide reference clock to the 953 CLK-IN pin
   - FPD rate is running at constant rate proportional to the external reference clock
   - The CSI rate is independent of the FPD rate
   - Back channel speed must be below 10-Mbps (Manchester) rate
   - AC Cap of 0.1 μF is required
FPDLINK
• Fundamental (payload, line rate, UI, jitter)
• Adaptive EQ
• I2C and Alias
• Link Diagnostics
• Power-over-coax
• Cable Requirement
• CMLOUT Eye Diagram Monitor
• Build-in-self Test (BIST)
ADAS FPD-Link III Payload
91x/93x/95x

28 bit Payload

C1 = Clock bit HIGH
C0 = Clock bit LOW
DCA & DCB = Link Overhead
DIN[n:1] -> DS90UB903/4: 24 Data Bits (18-bit RGB+3 + I2C)
Note: Payload bits are Randomized, Balanced & Scrambled
FPD-Link III Math:
DS90UB903/904 - 43 MHz Example

• 43 MHz Input Clock (pixel clock, PCLK)
  – 23.26 ns period
• 1 UI (Unit Interval) serial data bit is 1/28th of clock period:
  – 23.26 ns / 28
  – 1 UI = 830 ps
• Serial line rate:
  – 43 MHz x 28 bits = 1.20Gbps

Jitter needs to be less than 398.4ps.

Oscilloscope Requirements:
• 50-ohm terminated
• > 2 x Line Rate

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Pin/Freq.</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
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<td>t_{DD}</td>
<td>Deserializer Delay</td>
<td>Default Registers Register 0x03h b[0] (RRFB = 1)</td>
<td>10 MHz–43 MHz</td>
<td>4.571T  + 8</td>
<td>4.571T  + 12</td>
<td>4.571T + 16</td>
<td>ns</td>
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<td>t_{DDEL}</td>
<td>Deserializer Data Lock Time</td>
<td>(Figure 15)²</td>
<td>10 MHz–43 MHz</td>
<td>10</td>
<td></td>
<td></td>
<td>ms</td>
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<td>t_{RJIT}</td>
<td>Receiver Input Jitter Tolerance</td>
<td>(Figure 19, Figure 21)³⁴</td>
<td>43 MHz</td>
<td>0.53</td>
<td></td>
<td></td>
<td>UI</td>
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FPDLINK Adaptive Equalization (EQ)

- Gain curve in Deserializer compensates for cable loss
- Programmable gain setting
- Enhanced ADAPTIVE EQ – automatically selects gain to compensate for cable loss (no programming)
I2C Control Interface Communication

- I2C compatible interface bridged over link – up to 400kHz
  - Multi-master arbitration supported
  - Clock stretching required
- Local and remote I2C access
- Up to 16 unique addresses – configurable via ID[x]
I2C Clock Stretch

SCL Stretching by local Ser/Deser provides necessary time delay for remote device acknowledge across link

- For remote accesses, the “Response Delay” shown is on the order 10 – 15 us for DS90UB901/2/3/4Q and DS90UB913/914Q
- The “Response Delay” includes the latency time of the control channel packing and serialization protocol across the differential link to the remote peripheral
I2C R/W Remote Slave

1. If SER is connected and system is powered up, DES 0x06 register will auto load SER address.
2. Set I2C Pass-through (SER 0x03[1] → 1'b)
3. Set SlaveID0 (SER 0x07 → 0x0A)
4. Set SlaveAlias (SER 0x08 → 0x0A)
5. Read/Write to Slave using address 0x0A
I2C Access Multiple Remote Slaves

- Why SlaveAlias register? → Eliminates remote slave ambiguity
- Set I2C Pass-through (SERA, SERB 0x03[1]→1'b)
- Set SERA Slave ID (SERA 0x07→0x0A)
- Set SERA Slave Alias (SERA 0x08→0x0A)
- Set SERB Slave ID (SERB 0x07→0x0A)
- Set SERB SlaveAlias (SERB 0x08→0x0B)
- Read/Write to Slave A with address 0x0A, Slave B with address 0x0B
I2C over DS90UB913/4 FPD-Link III with Bidirectional Control Channel


Figure 7. I2C Master attached to Serializer

Table 6. Typical I2C bit rates

<table>
<thead>
<tr>
<th>Host I2C Rate</th>
<th>Remote I2C Rate</th>
<th>Master Proxy register settings</th>
<th>Net Bit Rate</th>
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<td>100 kbit/s</td>
<td>77 kbit/s (Default)</td>
<td>&quot;SCL High Time&quot; register 0x82 (Default)</td>
<td>41 kbit/s</td>
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<tr>
<td>100 kbit/s</td>
<td>100 kbit/s</td>
<td>&quot;SCL Low Time&quot; register 0x82 (Default)</td>
<td>47 kbit/s</td>
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<td>400 kbit/s</td>
<td>100 kbit/s</td>
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<td>400 kbit/s</td>
<td>&quot;SCL Low Time&quot; register 0x64</td>
<td>155 kbit/s</td>
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1. **LOCK**: Verifies link established between SER and DES – CDR has “locked” to incoming serial data stream. Monitor LOCK pin.

2. **BIST (Built-in Self Test)**: Verifies data integrity of link between SER and DES. Monitor PASS pin.

3. **CRC**: Integrity of backchannel link. Error reporting via register.

4. **PAT GEN**: Visually validate data path without video source. Test pattern generated by SER or DES.

5. **LINK DETECT**: Remote verification of link between SER and DES. Monitor register in SER.
FPD-Link III for Driver Assist
Power-over-Coax

- PoC Overview
- Inductor Selection Criteria
- Cable requirement
- PoC FPDLINK Performance Test
Overview of FPD-III

- FPD-III has a high speed forward channel, and a lower speed bidirectional backchannel, which is all sent over either a piece of coax cable, or a single pair in a shielded twisted pair cable.
- The forward and back channels are separated in the frequency domain.
Power Over Coaxial Cable Concept

- Same implementation for many years on antenna connections
FPD-link III and Power over Coax
Functional Block diagram

Megapixel Camera Module
- Image sensor SOC
- FDP-Link III Serializer
- LDO
- Power Supply

DS90UB913A
- Coaxial Cable
- POWER
- Braided Shield

ECU
- FDP-Link III Deserializer
- MPU
- Camera Power
- Power Supply

DS90UB914A
Power Over Coaxial Cable Overview

• Power injected on coax cable at Deserializer; drawn from other end of cable
• Power over Coax or Differential Pairs provides power distribution for remote sensors, i.e., cameras
• Typical current range 0.2A to 0.5A, voltage of 5-8V, <4 Watts
• Cable braid used as ground return
• Inductor selected to provide required AC impedance over operating frequency range of the differential signals - Forward & Back-channel
• Ensure inductor saturation and RMS current requirements are met
Coupling Inductor Selection Criteria

• Impedance vs. Frequency ➔ Inductance Value
  – Select component to have high impedance (~1kOhm) at operating frequency of serial communication channel
    • SRF and Q parameters impact this characteristic curve
  – DS90UB913A/914A
    • High Speed Forward channel: 700MHz max
    • Low Speed Backchannel: 2.5MHz, target 1MHz (provides margin)

• Saturation/RMS Current
  – Max current @ minimum voltage delivered at camera
  – Higher Isat & IRMS requires larger footprint
  – IRMS important to limit camera heat!

• Size
  – Optimize selection to meet criteria listed above to achieve smallest footprint
### Power over Coaxial: inductor selection

**Impedance Versus Frequency Plot for a Single Inductor**

<table>
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<tr>
<th>FPD-Link III</th>
<th>Max PCLK (MHz)</th>
<th>Forward Channel Line Rate (Gbps)</th>
<th>Embedded Bidirectional Control Channel</th>
<th>Target Power Feed Inductance</th>
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<td>DS90UB913A/914A</td>
<td>100</td>
<td>1.400</td>
<td>Yes</td>
<td>100uH + 4.7uH</td>
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- Forward channel is 700MHz.
- Back channel is 2.5MHz with 30% frequency variation.
PoC Cable S-parameter Requirements

- Insertion Loss
- Return Loss

What you need to know about high-speed cables for FPD-Link III SerDes (3Q 2017)

S-parameter

S12
Reverse Gain
Insertion Loss,
Transmission Phase

S11,
Input
Refl.
Coeff. $\Gamma_{in}$
Return
Loss,
VSWR

S12

Device Under Test

S22,
Output
Refl.
Coeff. $\Gamma_{out}$
Return
Loss,
VSWR

S21, Forward Gain
Insertion Loss,
Transmission Phase

**Figure 6. Definition of return loss**

\[ R_L = 20 \log \left( \frac{Z_L - Z_{REF}}{Z_L + Z_{REF}} \right) \text{(dB)} \]
Insertion Loss and Return Loss

Figure 8. Insertion loss of a 15-m coaxial cable

Coax

Figure 9. Insertion loss of a 10-m STQ differential cable

STQ
50 Ω Single-ended Coaxial (FAKRA/RTK 031)

Across cable lengths:
- 1m
- 2m
- 5m
- 10m

@1.5GHz

@750MHz
Coaxial Cable/Connector

- Multiple suppliers:
  - Rosenberger/Leoni, AMP, TE Connectivity (Tyco), Molex, Delphi, Pasternack, Flontec, Shikoku
FPD-Link Performance Measurement

- CML Output Eye Diagram
- Build-in-self Test (BIST)
Monitor Output of Equalized Signal

FPD-Link III

D

Cable

R

EQ

CDR

CMLOUT+-/
Measure CMLOUT to See Signal Quality

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O TYPE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>NO.</td>
<td></td>
</tr>
<tr>
<td>DIAGNOSTIC PINS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMLOUTP</td>
<td>38</td>
<td>Channel monitor loop-through (CML) driver differential output. Typically routed to test points and not connected. For monitoring terminate CMLOUT with a 100-Ω differential load.</td>
</tr>
<tr>
<td>CMLOUTN</td>
<td>39</td>
<td></td>
</tr>
</tbody>
</table>
## DS90UB914A-Q1 CML OUTPUT Enable

### 0x3F b4 Set 1

**Hardware pin**

<table>
<thead>
<tr>
<th></th>
<th>7:5</th>
<th>4</th>
<th>3:0</th>
<th>Reserved.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x3F</td>
<td>RSVD</td>
<td>CML OUT Enable</td>
<td>RSVD</td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RW</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

*CML Output Driver Enable is Active-Low. 0: CML Loop-through Driver is powered up. 1: CML Loop-through Driver is powered down.*

**Analog Launchpad GUI**

Set DS90UB914 0x3F b4 to 0 to enable CML.

**Change port if needed.**

<table>
<thead>
<tr>
<th>SEL</th>
<th>Input LVCMOS w/ pulldown</th>
<th>MUX Select Line</th>
</tr>
</thead>
<tbody>
<tr>
<td>46</td>
<td></td>
<td>SEL = L, RIN0+/- input. This selects input A as the active channel on the Deserializer.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SEL = H, RIN1+/- input. This selects input B as the active channel on the Deserializer.</td>
</tr>
</tbody>
</table>
CMLOUT Eye Diagrams
with and without Power Feed (PoC)

Recovered Data Eye Diagram after 10m Coaxial Cable
## DS90UB914A-Q1 CML Output Eye Diagram Calculation

<table>
<thead>
<tr>
<th>CML MONITOR OUTPUT DRIVER SPECIFICATIONS (CMLOUTP, CMLOUTN)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>$E_w$</strong></td>
</tr>
<tr>
<td><strong>$E_H$</strong></td>
</tr>
</tbody>
</table>

Assume use 12-bit low frequency mode:

- Line rate = PCLK $\times$ 28-bit
- Line rate = 1.4Gbps

PCLK = Line rate / 28 = 1.4G / 28 = 50MHz

$E_w = 0.45UI$

$E_{jitter} = 1 - E_w = 0.55UI$

Line rate = 1.4Gbps = 700MHz

$1UI = 1 / (PCLK \times 28\text{-bit}) = 714ps$

Jitter tolerance = $714ps \times 0.55 = 392.7ps$

CML output with PoC Jitter: 127ps

CML output w/o PoC Jitter: 113.8ps

Conclusion: Chipsets with PoC jitter is 127ps which is less than 392.7ps jitter tolerance.

DES is able to lock data.
**Built In Self Test (BIST): Definition**

- **Definition of BIST:**
  - SER outputs continuous stream of a pseudo-random sequence and overrides the BCC.
  - The DES detects the test pattern and monitors it for errors.
  - Tests link independently of CSI data.
  - BIST checks FC and BC:
    - Parity errors = FC errors
    - CRC errors = BC errors
Built In Self Test (BIST): Steps

- Steps for BIST:
  - Digitally reset 953 and 954
  - Confirm Lock between devices
  - Clear any previous errors
  - Enable BIST
    - Force errors if necessary
  - Check for errors
    - Refer to flowchart
FPD-LINK Fault Analysis

Possible root causes for lock not stable problem:
1. No length matching at Layout 1
2. Power ripple at DES
3. Oscillator exceeding jitter
4. Connector impedance insufficient causing return loss too high
5. Cable return loss and insertion loss
6. PoC inductor impedance insufficient causing return loss too high (ADAS product)
7. AC coupling capacitor for line rate
8. Termination resistor
9. Power ripple at SER
10. Pixel clock/CSI clock jitter
FPD-LINK Fault Analysis

- Remove Cable.
  - Enable DES Internal Pattern Generator.

  Yes

- Connect Cable.
  - Enable SER Internal Pattern Generator.
  - Use external timing

  Yes

- Measure Data at SER input
  - Layout impedance matching or impedance discontinuity

  Yes

- OSC jitter
  - PCLK/CLK_CSI jitter

  Yes

- DES Power ripple
  - OSC jitter
  - Layout to display

  No

- Pat Gen with internal timing

  Yes

- Cable return loss
  - PoC inductor return loss
  - SER Power ripple

  No

Image Lock: Yes
Image no lock: No
DS90UB953-Q1 and DS90UB954-Q1 TI Training

https://training.ti.com/ds90ub953954-system-design-operation

1. DS90UB953/954 System Design & Operation: Overview
2. DS90UB953/954 System Design & Operation: Typical Customer Issues
3. DS90UB953/954 System Design & Operation: Basic Design Rules
4. DS90UB953/954 System Design & Operation: 953-954 Link Design
5. DS90UB953/954 System Design & Operation: Sensor-953 Link Design
6. DS90UB953/954 System Design & Operation: 954-ISP/SoC Link Design
7. DS90UB953/954 System Design & Operation: Hardware Design
ADAS FPD-Link Reference Designs

**TDA Ruggedized Video Processor (RVP)**
- Performs CMS, SVS, stereo cam, mono cam+ RADAR fusion, & other applications
- TDA3x or TDA2x +DS90UB960
- Supports Aptina, OVT, & Sony sensors
- Samples NOW

**TIDA-00162 Multi-Camera System**
- Supports up to 6 cameras
- OV10635+DS90UB913A/914A
- FMC connector plugs into FPGA or MCU board for video processing

**PMP10653 Camera Module**
- OV10640+DS90UB913A
- Wide-Vin LM53603Q1 DC/DC
- High PSRR LDO LP5907

**PMP9351 Camera Module**
- OV10635+DS90UB913Q
- LP3990 linear Vreg

**TIDA-00455 SVS Reference Design**
- OV10640+DS90UB964+ OV490
- TDA2xx processor
- Call TI for info

**TIDA-00421 1.3MP Camera**
- OV10640 +DS90UB913A
- TLV702 300 mA LDO
- TPS62170 Buck in 2x2 QFN
- Small 20x20 mm PCB

**TIDA-00262 1MP Camera**
- AR0140AT+DS90UB913A
- TPS3836E18-Q1 220nA Supervisor
- TPS62170-Q1 DC/DC

**TIDA-00098 1MP Camera**
- AP0101AT+DS90UB913A
- LM34919C, TPS62231 buck regulators

**Texas Instruments**
Thank you.

Q&A
Back Up
FPD-LINK Collateral

- What you need to know about high-speed cables for FPD-Link III SerDes (3Q 2017)

- Cable Requirements for the DS90UB913A & DS90UB914A

- How to design remotely-powered cameras for automotive applications (1Q 2017)

- Sending Power Over Coax in DS90UB913A Designs

- Ten tips for successfully designing with automotive EMC/EMI requirements (3Q 2015)

- I2C over DS90UB913/4 FPD-Link III with Bidirectional Control Channel