TI high-speed signal chain update
May 2017

Product Links:
High-Speed ADC (>10MSPS): www.ti.com/highspeedadc
High-Speed DACs (>10MSPS): www.ti.com/highspeeddac

Training Links:
High-Speed Signal Chain University: www.ti.com/hsscu

Reference Designs:
TI Designs: www.ti.com/tidesigns

High-Speed Amps (>=50MHz): www.ti.com/highspeedamp
Clocks and Timing: http://www.ti.com/clocks
Data Converters at Texas Instruments

**Analog to Digital Converters (ADCs)**

- **Precision ADCs**
  - SAR and Delta-sigma ADCs
  - Typically <= 10 MSPS
  - From 4.5 to 32 bits of resolution
  - [www.ti.com/precisionadc](http://www.ti.com/precisionadc)

- **High-Speed ADCs**
  - Pipeline and Folding Interpolating ADCs
  - RF sampling ADCs down to 10 MSPS
  - From 8 to 16 bits of resolution
  - [www.ti.com/highspeedadc](http://www.ti.com/highspeedadc)

- **Isolated ADCs**
  - Up to 7 kV peak of reinforced isolation
  - 16 bits of resolution

**Digital to Analog Converters (DACs)**

- **Precision DACs**
  - Precision 4 – 20mA DACs
  - Integrated ADCs and DACs for PA monitoring
  - High-density DACs with up to 96 channels
  - [www.ti.com/precisiondac](http://www.ti.com/precisiondac)

- **High-Speed DACs**
  - Up to 9 GSPS DACs for wideband systems
  - JESD204B and LVDS options available
  - 1x – 24x interpolation options available
  - [www.ti.com/highspeeddac](http://www.ti.com/highspeeddac)
TI offers the complete high-speed signal chain
High-Speed Data Converters
New Products In Production

ADC16DX370
Dual, 16-Bit
370MSPS, 0.8W/ch.
JESD204B

ADS42LB/JB69
Dual, 16-Bit
250MSPS, 0.8W/ch.
JESD204B

ADS52J90
32-ch, 14-Bit
Up to 100MSPS
25 mW/ch.
JESD204B

ADC344x
Quad, 14-Bit
25-160MSPS
SLVDS/204B

ADC342x
Quad, 12-Bit
25-160MSPS
SLVDS/204B

ADC32x
Quad, 12-Bit
25-160MSPS
SLVDS/204B

ADC322x
Quad, 12-Bit
25-160MSPS
SLVDS/204B

ADC54J69
Dual, 16-Bit
500MSPS, 1.35W/ch.
JESD204B (5G)

ADC31JB68
Single, 16-Bit
500MSPS, 0.9W/ch.
JESD204B (5G)

ADS54J66
Quad, 14-Bit
500MSPS, 0.675W/ch.
JESD204B (10G)

ADC14X250
Single, 14-Bit
250MSPS
JESD204B

ADC54J60
Dual, 16-Bit
1 GSPS, 1.35W/ch.
JESD204B (5G)

ADS54J40
Dual, 14-Bit
1 GSPS, 1.3W/ch.
JESD204B (5G)

ADC54J42
Dual, 14-Bit
625MSPS, 1.3W/ch.
JESD204B (5G)

ADS54J46
Quad, 14-Bit
500MSPS, 0.675W/ch.
JESD204B (10G)

ADC12J1600
Single, 12-Bit
1.6 GSPS, 2W
JESD204B IF

ADC12J6000
Single, 12-Bit
1.6 GSPS, 2W
JESD204B IF

ADS54J20
Dual, 12-Bit
1 GSPS, 1.3W/ch.
JESD204B (5G)

ADC12J1700
Single, 12-Bit
2.7 GSPS, 2W
JESD204B IF

ADC12J4000
Single, 12-Bit
4 GSPS, 2W
JESD204B IF

ADC37J84
Quad, 16-Bit
1.6 GSPS, 1.4W
16x Int, NCO, PLL

ADC38J84
Quad, 16-Bit
1.6 GSPS, 1.4W
16x Int, NCO, PLL

ADC39J84
Quad, 16-Bit
1.6 GSPS, 1.4W
16x Int, NCO, PLL

ADC37J82
Dual, 16-Bit
1.6 GSPS, 0.9W
16x Int, NCO, PLL

ADC38J82
Dual, 16-Bit
1.6 GSPS, 0.9W
16x Int, NCO, PLL

ADC39J82
Dual, 16-Bit
1.6 GSPS, 0.9W
16x Int, NCO, PLL

ADC32RF42
Dual, 14-Bit, 1.5Gsps
DDC optional
JESD204B (12.2Gbps)

ADC32RF45
Dual, 14-Bit, 3Gsps
DDC optional
JESD204B (12.2Gbps)

ADC32RF40
Dual, 14-Bit, 3Gsps
DDC required
JESD204B (12.2Gbps)

ADC32RF44
Single, 14-Bit, 2.6Gsps
DDC required
JESD204B (12.2Gbps)

ADC32RF80
Dual, 14-Bit, 3Gsps
Wideband Input

ADC32RF82
Dual, 14-Bit, 3Gsps
Wideband Input

ADC32RF83
Dual, 14-Bit
9 GSPS, 3W
Int, NCO, PLL

ADC32RF80
Dual, 14-Bit
9 GSPS, 3W
Int, NCO, PLL, +balun

ADC32RF82
Dual, 14-Bit
9 GSPS, 3W
Int, NCO, PLL, +balun

ADC12J66
Quad, 14-Bit
500MSPS, 0.675W/ch.
JESD204B (5G)

ADC12J1600QML
Space Grade, 2-ch, 12-Bit
1.6GSPS, w/LVDS

ADC121600QML-SP
Space Grade, 2-ch, 12-Bit
1.6GSPS, w/LVDS

ADC121600QML-SP
Space Grade, 2-ch, 12-Bit
1.6GSPS, w/LVDS

ADC12J66
Quad, 14-Bit
500MSPS, 0.675W/ch.
JESD204B (5G)

ADC121600QML-SP
Space Grade, 2-ch, 12-Bit
1.6GSPS, w/LVDS

ADC121600QML-SP
Space Grade, 2-ch, 12-Bit
1.6GSPS, w/LVDS

ADC12J66
Quad, 14-Bit
500MSPS, 0.675W/ch.
JESD204B (5G)

ADC121600QML-SP
Space Grade, 2-ch, 12-Bit
1.6GSPS, w/LVDS

ADC121600QML-SP
Space Grade, 2-ch, 12-Bit
1.6GSPS, w/LVDS

ADC12J66
Quad, 14-Bit
500MSPS, 0.675W/ch.
JESD204B (5G)

ADC121600QML-SP
Space Grade, 2-ch, 12-Bit
1.6GSPS, w/LVDS
ADC32RF45: Dual 14-bit 3GSPS RF-Sampling ADC Family with Multiband Digital Down Converter

**Features**

- 14-bit Dual Channel ADC family max sample rate of 3Gsp/s
- Analog input bandwidth: >3GHz
- Aperture Jitter: ~70fs
- Input Fullscale: 1.35Vpp
- RMS and peak power detectors
- Dual-band Digital Down Converter (DDC) with frequency hopping;
  - Down convert two bands of up to 300 MHz bandwidth or one band of up to 600 MHz bandwidth
  - Phase coherent frequency hopping supported by one DDC through use of three independent 16-bit NCOs
  - Fully bypassable
- On Chip Decimation 4, 6, 8, 9, 10, 12, 16, 18, 20, 24, 32
- JESD204B 12Gbps, Subclass 1 support
- Power Consumption: 3.2W/ch @ 3GSPS
- Package: 72QFN (10x10mm)

### Input Frequency

<table>
<thead>
<tr>
<th>Input Frequency</th>
<th>500MHz -1dBFS</th>
<th>2.0 GHz -3dBFS</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNR (dBFS)</td>
<td>62</td>
<td>58.5</td>
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<tr>
<td>NSD (dBFS/Hz)</td>
<td>-154</td>
<td>-150.5</td>
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<tr>
<td>HD2,3 (dBc)</td>
<td>70</td>
<td>65</td>
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<tr>
<td>HD2,3 Image (dBc)*</td>
<td>85</td>
<td>80</td>
</tr>
<tr>
<td>HD4,5 (dBFS)</td>
<td>85</td>
<td>80</td>
</tr>
<tr>
<td>Non HD2-5 (dBFS)</td>
<td>85</td>
<td>80</td>
</tr>
<tr>
<td>Interleaving Spur (dBc)</td>
<td>80</td>
<td>80</td>
</tr>
</tbody>
</table>

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[Diagram of ADC32RF45 block diagram and pinout]

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**Texas Instruments**

[Logo]
ADC32RF4x/8x offers pin compatible RX solutions

<table>
<thead>
<tr>
<th>Part #</th>
<th>Ch’s</th>
<th>ADC Bits</th>
<th>Max Output Rate</th>
<th>Max ADC Sample Rate</th>
<th>Decimation</th>
<th>DDCs/Ch</th>
<th>Released</th>
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</thead>
<tbody>
<tr>
<td>ADC32RF45</td>
<td>2</td>
<td>14-bit</td>
<td>12-bit 3 GSPS 14-bit 2.46 GSPS</td>
<td>3GSPS</td>
<td>0 or 4x-32x</td>
<td>2</td>
<td>Yes</td>
</tr>
<tr>
<td>ADC32RF44</td>
<td>2</td>
<td>14-bit</td>
<td>12-bit 2.6 GSPS 14-bit 2.46 GSPS</td>
<td>2.6GSPS</td>
<td>0 or 4x-32x</td>
<td>2</td>
<td>Yes</td>
</tr>
<tr>
<td>ADC32RF42</td>
<td>2</td>
<td>14-bit</td>
<td>14-bit 1.5GSPS</td>
<td>1.5 GSPS</td>
<td>0 or 4x-32x</td>
<td>2</td>
<td>5/25/17</td>
</tr>
<tr>
<td>ADC32RF40</td>
<td>2</td>
<td>14-bit</td>
<td>14-bit 750 MSPS complex</td>
<td>3 GSPS</td>
<td>4x-32x</td>
<td>2</td>
<td>Yes</td>
</tr>
<tr>
<td>ADC32RF83</td>
<td>2</td>
<td>14-bit</td>
<td>14-bit 750 MSPS complex</td>
<td>3 GSPS</td>
<td>4x-32x</td>
<td>1</td>
<td>Yes</td>
</tr>
</tbody>
</table>

DDC REQUIRED (removes bypass mode)
DAC38RF8x: Dual 9GSPS RF DAC
Monolithically integrated Tx Bits-to-RF solution

Features

- Dual/Single channel 14-bit DAC
- DAC MAX sample rate: 9 GSPS
- Output Frequency Range:
  - 0 – 4.5 GHz 1st Nyquist
  - up to 6 GHz supported in 2nd Nyquist
- Input Interface:
  - Up to 8 lane JESD204B @ 12.5 Gbps
  - Up to 1.23 GSPPS Complex
  - License free export
  - Supporting WCDMA, LTE & MC-GSM
- Digital Processing & Options:
  - 2x Dual-band DUC
  - Interpolation: 6, 8, 10, 12, 16, 18, 20, 24x
  - Complex Mixer with NCO
- RF Output Options:
  - Balun: Single-ended output with 3 dBm full scale, ~700 MHz to > 4 GHz
  - Differential (DC coupled) output with 7 dBm full scale output power (tone)
  - Multi-DAC synchronization (subclass 1)
- Optional internal PLL/VCO to generate high-rate sampling clock
  - 130 dBc/Hz at 2.1 GHz output/2 MHz offset (supports 3G/4G BTS)
  - 138 dBc/Hz at 1.8 GHz output/1.8 MHz offset (supports GSM/3G/4G BTS)
- Divided output clock for feedback ADC
- Package: 10x10mm BGA, 0.8mm pitch
- Total Power @ 9GSPS:
  - 1 DUC mode: 1.35W/ch
  - 2 DUC mode: 1.55W/ch
DAC38RFxx offers pin-compatible TX solutions

<table>
<thead>
<tr>
<th>Part #</th>
<th>Ch’s</th>
<th>Max Input Rate Complex</th>
<th>RF Output</th>
<th>Max Output Rate</th>
<th>DUCs/Ch</th>
<th>Bypassable Internal VCO/PLL</th>
<th>Interpolation</th>
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<tbody>
<tr>
<td>DAC38RF82</td>
<td>2</td>
<td>2.5 GSPS 16-bit 3.3 GSPS 12-bit 9 GSPS 8-bit real</td>
<td>Differential DC-4.5GHz</td>
<td>9.0 GSPS</td>
<td>2</td>
<td>6, 9 GHz</td>
<td>1x-24x</td>
</tr>
<tr>
<td>DAC38RF89</td>
<td>2</td>
<td>2.5 GSPS 16-bit 3.3 GSPS 12-bit 9 GSPS 8-bit real</td>
<td>Differential DC-4.5GHz</td>
<td>9.0 GSPS</td>
<td>2</td>
<td>5, 7.5 GHz</td>
<td>1x-24x</td>
</tr>
<tr>
<td>DAC38RF83</td>
<td>1</td>
<td>1.25 GSPS</td>
<td>Differential DC-4.5GHz</td>
<td>9.0 GSPS</td>
<td>2</td>
<td>6, 9 GHz</td>
<td>6x-24x</td>
</tr>
<tr>
<td>DAC38RF80</td>
<td>1</td>
<td>1.25 GSPS</td>
<td>SE balun 700M-4GHz</td>
<td>9.0 GSPS</td>
<td>2</td>
<td>6, 9 GHz</td>
<td>6x-24x</td>
</tr>
<tr>
<td>DAC38RF86</td>
<td>1</td>
<td>1.25 GSPS</td>
<td>SE balun 700M-4GHz</td>
<td>9.0 GSPS</td>
<td>2</td>
<td>9 GHz low noise</td>
<td>6x-24x</td>
</tr>
<tr>
<td>DAC38RF87</td>
<td>1</td>
<td>1.25 GSPS</td>
<td>SE balun 700M-4GHz</td>
<td>9.0 GSPS</td>
<td>2</td>
<td>6 GHz low noise</td>
<td>6x-24x</td>
</tr>
<tr>
<td>DAC38RF93</td>
<td>1</td>
<td>750 MSPS</td>
<td>Differential DC-4.5GHz</td>
<td>9.0 GSPS</td>
<td>1</td>
<td>6, 9 GHz</td>
<td>12x-24x</td>
</tr>
<tr>
<td>DAC38RF90</td>
<td>1</td>
<td>750 MSPS</td>
<td>SE balun 700M-4GHz</td>
<td>9.0 GSPS</td>
<td>1</td>
<td>6, 9 GHz</td>
<td>12x-24x</td>
</tr>
<tr>
<td>DAC38RF96</td>
<td>1</td>
<td>750 MSPS</td>
<td>SE balun 700M-4GHz</td>
<td>9.0 GSPS</td>
<td>1</td>
<td>9 GHz low noise</td>
<td>12x-24x</td>
</tr>
<tr>
<td>DAC38RF97</td>
<td>1</td>
<td>750 MSPS</td>
<td>SE balun 700M-4GHz</td>
<td>9.0 GSPS</td>
<td>1</td>
<td>6 GHz low noise</td>
<td>12x-24x</td>
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<tr>
<td>DAC38RF85</td>
<td>1</td>
<td>1.25 GSPS</td>
<td>Differential DC-4.5GHz</td>
<td>9.0 GSPS</td>
<td>2</td>
<td>6, 9 GHz</td>
<td>6x-24x</td>
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<tr>
<td>DAC38RF84</td>
<td>1</td>
<td>1.25 GSPS</td>
<td>SE balun 700M-4GHz</td>
<td>9.0 GSPS</td>
<td>2</td>
<td>6, 9 GHz</td>
<td>6x-24x</td>
</tr>
</tbody>
</table>
LMX2592: Industry’s lowest noise 9.8-GHz RF Synthesizer
Supports wide frequency range from 0.02 – 9.8GHz

Features

• Wide frequency output range 20 MHz – 9.8GHz
• Supports wide input reference range of 5 MHz – 1.4GHz
• -134.5 dBc/Hz VCO Phase Noise @ 1 MHz offset for 6 GHz Carrier
• Innovative technique to remove Integer Boundary Spurs (IBS)
• Low noise frequency synthesizer
  • Normalized phase noise - 231 dBc/Hz
  • 50 fs typical RMS jitter (12KHz – 20MHz)
• Phase Adjust feature for beam forming and clocking high speed Data Converters
• 3.3V single supply voltage
• Dual Differential Outputs

Benefits

• Lowest noise Frac-N Synthesizer in the market
  • Improves performance for T&M applications
  • Enables high sensitivity radio receivers
• Generates wide frequency range to cover L / C / S - Band applications
  • Reduce the system complexity and cost
  • Allows flexibility to use same hardware across different RF bands.

See this clocking solution implemented in:
1. 1-GHz Signal Bandwidth RF Sampling Receiver Reference Design

<table>
<thead>
<tr>
<th>LMX2592 Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device Count</td>
</tr>
<tr>
<td>DEVCLK</td>
</tr>
</tbody>
</table>

Texas INSTRUMENTS
High-speed signal chain solutions available today

**LMH5401**
8 GHz GBW Fully Differential Amp, Usable bandwidth from DC to 2 GHz
DC or AC coupled operation
HD2: -80 dBc @ 500 MHz

**ADC32RF45**
Dual, 14-bit, 3 GSPS ADC
Noise Floor: -155 dBFS/Hz
SNR: 58.0 dBFS @ fIN = 1.78 GHz
JESD204B subclass 1
Ch. Isolation: 95 dB @ fIN = 1.8 GHz

**LMK04828**
Clock distribution and jitter cleaner
< 100 fs RMS jitter, JESD204B support

**TPS54116-Q1**
DDR Power Solution with 4-A, 2-MHz, VDDQ DC/DC Converter, 1-A VTT LDO and VTTREF

**66AK2L06**
Multicore DSP+ARM KeyStone II System-on-Chip (SoC)
Support up to 4x Lane JESD204A/B.

**TMP461**
1.8 V remote & local temp sensor, Programmable non-ideality factor I2C/Smbus

**LMH3404**
7 GHz GBW, Dual Channel FDA
Usable bandwidth from DC to 2 GHz
20dB fixed gain
HD2: -64 dBc @ 500 MHz

**DAC38RF93**
Dual, 14-bit, 9 GSPS DAC
Differential output
6x-24x Interpolating
Internal 6 & 9 GHz PLL
JESD204B subclass 1

**LMZ31530**
3V to 14.5V, 30A Power Module
Low-noise power solution for ADC32RF4x

- 1-GHz Signal Bandwidth RF Sampling Receiver Reference Design
- Multi-band RF Sampling Receiver Reference Design
- RF Sampling S-Band Radar Receiver Reference Design

NEW white paper discussing: Minimum power specifications for high-performance ADC
Low-noise power solution for DAC38RF8x

- **Power Supply Reference Design for Optimizing Spur and Phase Noise in RF-sampling DACs**
Complete power solution for FPGA/Processors

- **Sequencing**
  - LM3881 Simple Power Sequencer with Programmable Time Delay

- **FPGA**
  - $V_{CORE}$
  - $V_{IO}$ Rail (1.8V)
  - $V_{IO}$ Rail (2.8V)
  - $V_{IO}$ Rail (3.3V)
  - $V_{AUX}$
  - $V_{REF}$

- **PMIC**
  - 5 VDC Supply
  - DDR Power Solution with 4-A, 2-MHz, VDDQ DC/DC Converter, 1-A VTT LDO and VTTREF

- **TPS54116-Q1**
  - DDR Power Solution with 4-A, 2-MHz, VDDQ DC/DC Converter, 1-A VTT LDO and VTTREF

- **LMZ31530**
  - 3V to 14.5V, 30A Power Module

- **TPS53318**
  - High-Efficiency 8-A Synchronous Buck Converter with Eco-mode™

- **TPS7A89**
  - Dual, 2-A, Low Noise (3.8-μVRMS), LDO Voltage Regulator

- **TPS65086**
  - Configurable Multirail PMU for Multicore Processors/FPGAs

- **TPS65086**
  - Configurable Multirail PMU for Multicore Processors/FPGAs

- **TPS65086**
  - Configurable Multirail PMU for Multicore Processors/FPGAs

See our NEW landing page for FPGA power solutions at [www.ti.com/fpgapower](http://www.ti.com/fpgapower)
**Find the right online resource for your application**

High-Speed Signal Chain University is your portal to relevant training material on high-speed data converters, high-speed amplifiers, and clocking techniques. This includes topics such as:

| Extending JESD204B Link on Low Cost Substrates | Introduction to the RF Sampling Architecture | Advanced JESD204B topics, part 3 of 3: Multi-device synchronization |

### JES204B Link / Quality

- Serial Lane Interface
  - AC or DC Coupling
  - 100Ω differential channel
- Routing signal integrity is MOST critical of all JESD204B interface signals

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**RF Sampling Receiver**

- Simplified Architecture with more feasibility
- Eliminate
  - Quadrature Demodulator
  - RF Synthesizer
- Replace: Dual ADC with one RF sampling ADC
- Supports:
  - Higher Signal Bandwidths
  - Direct sampling of RF bands

**Clock Delays to Adjust Device Clock Skew**

![Clock Delays to Adjust Device Clock Skew Diagram](image)

At 3 GHz, 333.3 ps period of VCO. Half Step = 166.65 ps. Delaying green by 166.65 ps will reduce system skew.
Find the right product for your application

Visit our high-speed product landing pages below for more information:

High-Speed ADC (>10MSPS): [www.ti.com/highspeedadc](http://www.ti.com/highspeedadc)

High-Speed DACs (>10MSPS): [www.ti.com/highspeeddac](http://www.ti.com/highspeeddac)

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Clocks and Timing: [www.ti.com/clocks](http://www.ti.com/clocks)

High-Speed Signal Chain University: [www.ti.com/hsscu](http://www.ti.com/hsscu)
Thanks for watching!
Visit the links below for more information

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Reference Designs:
TI Designs: [www.ti.com/tidesigns](http://www.ti.com/tidesigns)
## Power Devices for Noise-Sensitive Applications

<table>
<thead>
<tr>
<th>Power Device</th>
<th>Description</th>
<th>VIN (V)</th>
<th>VOUT (V)</th>
<th>IOUT (mA)</th>
<th>Vnoise* (μVRMS)</th>
<th>PSRR** (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS7A89</td>
<td>Dual, 2-A, Low Noise (3.8-μVRMS), LDO Voltage Regulator - NEW</td>
<td>1.4 - 6.5</td>
<td>0.8 - 5.2</td>
<td>2</td>
<td>3.8 μVRMS</td>
<td>40</td>
</tr>
<tr>
<td>TPS7A88</td>
<td>Dual, 1A, Low Noise (3.8-μVRMS), LDO Voltage Regulator - NEW</td>
<td>1.4 - 6.5</td>
<td>0.8 - 5.2</td>
<td>1</td>
<td>3.8 μVRMS</td>
<td>40</td>
</tr>
<tr>
<td>TPS7A87</td>
<td>Dual, 500mA, Low Noise (3.8-μVRMS), LDO Voltage Regulator - NEW</td>
<td>1.4 - 6.5</td>
<td>0.8 - 5.2</td>
<td>500mA</td>
<td>3.8 μVRMS</td>
<td>40</td>
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<tr>
<td>TPS7A84</td>
<td>3 A, High-Accuracy (1%), Low-Noise (4.4 μVRMS), LDO</td>
<td>1.1 - 6.5</td>
<td>0.8 - 5V</td>
<td>3</td>
<td>4.4 μVRMS</td>
<td>40</td>
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<tr>
<td>TPS7A85</td>
<td>4 A, High-Accuracy (1%), Low-Noise (4.4 μVRMS), LDO</td>
<td>1.1 - 6.5</td>
<td>0.8 - 4V</td>
<td>4</td>
<td>4.4 μVRMS</td>
<td>40</td>
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<tr>
<td>TPS54122</td>
<td>Dual Output, High Efficiency 3A Switcher + 3A Low Noise LDO</td>
<td>2.95 - 5.5</td>
<td>0.8 - 3.6V</td>
<td>3</td>
<td>17 μVRMS</td>
<td>53</td>
</tr>
<tr>
<td>TPS7A47</td>
<td>36V, 1A, RF Low Noise LDO</td>
<td>3 - 36</td>
<td>1.4 - 34V</td>
<td>1</td>
<td>4.17 μVRMS</td>
<td>59</td>
</tr>
</tbody>
</table>

*BW = 10 Hz to 100 kHz, Vout min, Iout @ ~70%

**Iout max, f = 1 MHz

### TI Designs featuring these companion devices

- **TIDA-01161**: 1-GHz Signal Bandwidth RF Sampling Receiver Reference Design → uses the TPS7A47
- **TIDA-01084**: Continuous Wave Phase-aligned Multitone Generator Reference Design → uses TPS7A85
- **TIDA-00388**: Low noise linear regulator + DC/DC solution with excellent transient response → uses TPS54122