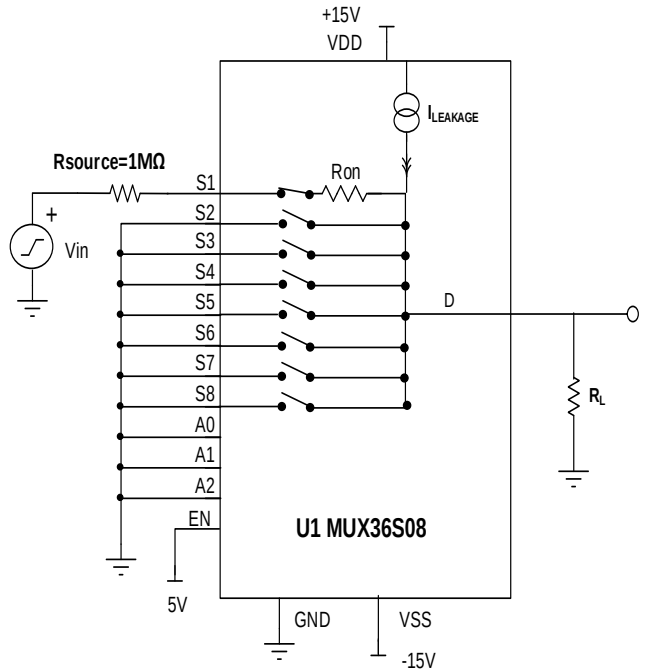
Basics of Analog Multiplexers – 2

Exercises

TI Precision Labs – Op Amps

1. In the circuit below, the MUX36S08 input channel is interfaced with a high input impedance source (1MΩ). The MUX has an on leakage current specification of 8pA to 100pA over 25^0C to 85^0C temperature range. This multiplexer is used in a 18 bit data acquisition system referenced to 4.5V. It is required that offset error introduced due to MUX leakage should not exceed a 10 LSB specification. Does this multiplexer meet this condition?

Assume Rsource >> Ron



2. There is an option to select one of the two multiplexers (MUX1 and MUX2) for a given DAQ system. MUX1 and MUX2 have charge injection figures of 1pC and 4.7pC respectively. MUX1 has an output load capacitance of 47pF while MUX2 has a load capacitance of 100pF. Which multiplexer will have minimum voltage error due to charge injection at the output?

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Solution

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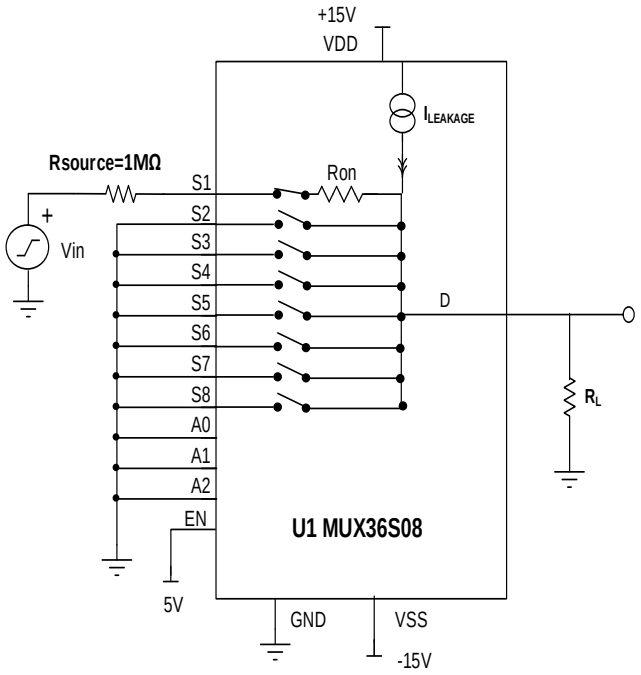
1. In the circuit below, the MUX36S08 input channel is interfaced with a high input impedance source (1MΩ). The MUX has an on leakage current specification of 8pA/100pA over 25^0C to 85^0C temperature range. This multiplexer is used in a 18 bit data acquisition system referenced to 4.5V. It is required that offset error introduced due to MUX leakage should not exceed a 10 LSB specification. Does this multiplexer meet this condition?



18-bit System Calculation

$$V_{ref} = 4.5V$$

$$V_{LSB} = \frac{4.5V}{2^{18}} = 17.16\mu V$$

$$\text{OffsetError}(V)_{25C} = I_{LEAKAGE} \cdot R_{SOURCE} = (8pA) * (1M\Omega) = 8\mu V$$

$$\text{OffsetError}(\text{Bits})_{25C} = \frac{\text{OffsetError}(V)}{V_{LSB}} = \frac{8\mu V}{17.16\mu V} = 0.46\ LSB$$

$$\text{OffsetError}(V)_{85C} = I_{LEAKAGE} \cdot R_{SOURCE} = (100pA) * (1M\Omega) = 100\mu V$$

$$\text{OffsetError}(\text{Bits})_{85C} = \frac{\text{OffsetError}(V)}{V_{LSB}} = \frac{100\mu V}{17.16\mu V} = 5.82\ LSB$$

1. In below circuit MUX36S08 input channel is interfaced with high input impedance source (1MΩ). MUX has on leakage current specification of 8pA/100pA over 25^0C to 85^0C temperature range. This multiplexer is used in 18 bit data acquisition system referenced to 4.5V. It is required that offset error introduced due to MUX leakage should not exceed 10 LSB specification. Does this multiplexer meet this condition?

Answer: From calculations shown in previous slide, we can see that the offset error introduced by the MUX36S08 across 25^0C to 85^0C is 0.46 LSBs to 5.82 LSBs which is less than the system offset requirement (10 LSBs). Thus, the MUX36S08 is suitable for this application.

2. There is an option to select one of the two multiplexers (MUX1 and MUX2) for a given DAQ system. MUX1 and MUX2 have charge injection figures of 1pC and 4.7pC respectively. MUX1 has an output load capacitance of 47pF while MUX2 has a load capacitance of 100pF. Which multiplexer will have minimum voltage error due to charge injection at the output?

Answer:

Output Error due to Charge Injection is given by

$$\text{Voltage Error} = Q_{INJ} / C_L$$

Where C_L is output load capacitance of MUX

2. There is an option to select one of the two multiplexers (MUX1 and MUX2) for a given DAQ system. MUX1 and MUX2 have charge injection figures of 1pC and 4.7pC respectively. MUX1 has an output load capacitance of 47pF while MUX2 has a load capacitance of 100pF. Which multiplexer will have minimum voltage error due to charge injection at the output?

Answer:

Output Error due to MUX1

$$\text{Voltage Error}_{\_MUX1} = Q_{INJ\_1} / C_{L1}$$
$$= 1pC / 47pF$$
$$= 21.27\ mV$$

Output Error due to MUX2

$$\text{Voltage Error}_{\_MUX2} = Q_{INJ\_2} / C_{L2}$$
$$= 4.7\ pC / 100\ pF$$
$$= 47\ mV$$

Thus, MUX1 will have less error due to charge injection at the output than MUX2.