Buck Regulator Architectures

4.6 Voltage Mode Buck Regulators
Voltage-Mode Regulator

Modulator

Output Filter

Error Amplifier
Advantages and Disadvantages

• Advantages
  – Stable modulation/less sensitive to noise
  – Single feedback path
  – Can work over a wide range of duty cycles

• Disadvantages
  – Loop gain proportional to $V_{IN}$
  – LC double pole often drives Type III compensation
  – CCM and DCM differences - a compensation challenge
  – Slow response to input voltage changes
  – Current limiting must be done separately
Modulator Gain

\[ A_M = \frac{V_{IN}}{V_P} \]
Output Filter

\[ \frac{V_{\text{OUT}}}{V_{\text{SW}}} = \frac{Z_B}{Z_A + Z_B} \]

* (Rx, Cy) indicate the components that drive the locations of the pole and the zero, detailed equations are in the notes.
The easiest place to compensate the entire loop is to adjust the compensation around the error amplifier. Several different approaches are possible.

\[
\frac{V_C}{V_{OUT}} = -\frac{Z_F}{Z_I}
\]
Type II Compensation

\[
\frac{V_C}{V_{OUT}} = -\frac{Z_F}{Z_I}
\]

* (\(R_x, C_y\)) indicate the components that drive the locations of the pole and the zero (and \(k\)), detailed equations are in the notes
Design Guidelines for Type II Compensation

• Choose a large value for $R_{FB2}$, between 2-200 kΩ
• Set the mid-band gain $k$ to give desired bandwidth
• Set $\omega_p$ equal to half the switching frequency:
  $\omega_p = \frac{2\pi F_{sw}}{2}$
• Set $\omega_z$ equal to the output filter double pole $\omega_O$
• Use the following equations to solve for the remaining variables

\[
R_C = kR_{FB2} \quad C_{C1} = \frac{1}{\omega_z R_C} \quad C_{C2} = \frac{1}{\omega_p R_C}
\]
Type III Compensation

\[ \frac{V_C}{V_{OUT}} = -\frac{Z_F}{Z_I} \]

* \((R_x, C_y)\) indicate the components that drive the locations of the poles and zeros, detailed equations are in the notes.
Design Guidelines for Type III Compensation

- Choose a large value for \( R_{FB2} \), between 2-200 kW
- Set the mid-band gain \( k \) to shift the open-loop gain up to give desired bandwidth
- Set \( \omega_{P1} \) equal to half the switching frequency:
  \[ \omega_{P1} = 2\pi * F_{sw}/2 \]
- Set \( \omega_{P2} \) equal to the output filter zero, \( \omega_{ESR} \)
- Set \( \omega_{Z1} \) and \( \omega_{Z2} \) equal to cancel out the output filter double pole
- Use the following equations to solve for the remaining variables

\[
\begin{align*}
R_{C2} &= \frac{1}{\omega_{P2}C_{C3}} \\
C_{C3} &= \frac{1}{\omega_{Z2}R_{FB2}} \\
C_{C1} &= \frac{\omega_{Z2}R_{FB2}}{\omega_{Z1}R_{C1}}C_{c3} \\
R_{C1} &= kR_{FB2} \\
C_{C2} &= \frac{1}{\omega_{P1}R_{C1}}
\end{align*}
\]

Texas Instruments
Internal Type III Voltage Mode Compensation (LM367x)

Internal Block Diagram

Typical Application Circuit
Internal Type III Voltage Mode Compensation (LM285x)

Internal Block Diagram

Typical Application Circuit

- PVIN
- AVIN
- EN
- SS
- SGND
- PGND
- SNS
- SW
- LM2852/3

V_{IN} = 3.3V

\text{Current Limit}

Z_{c1}

Z_{c2}

20 \text{ pF}

200 \text{ k}\Omega

400 \text{ k}\Omega

V_{OUT} = 2.5V
Thank you!