

# **Choosing the Best ADC Architecture for your Application**

## **Part 2:**

Hello, my name is Luis Chioye. I am an Applications Engineer with Texas Instruments Precision Data Converter team.

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Today we are going to give you an overview on how a Successive Approximation Register or SAR ADC works.

The typical topology of a successive approximation ADC consists of a sample and hold structure, an analog comparator, a Successive Approximation Register and N-Bit Search Digital-to-Analog Converter or (DAC).

A typical SAR conversion cycle consists of two phases: a sampling phase or acquisition period and a conversion phase. The accuracy of the conversion result is dependent on several factors. From the extrinsic point of view, the quality of the source signal and SAR driving circuitry play a significant role as well as the accuracy and stability of the reference voltage. From the ADC intrinsic point of view, the performance of the device is dependent on the accuracy of the internal DAC and comparator.

The conversion process starts with the acquisition phase or sampling period. During the sampling period, switch S2 is open, and Switch S1 closes and the analog input signal is allowed to charge the ADC's sample-and-hold

capacitor (Csh) to the voltage level of the analog input.

The voltage across the sampling capacitor charges with a single-pole response. During the acquisition time, the voltage on the sampling capacitor needs to charge from an initial voltage (VSH0) to the final target input signal level of VIN. By the end of the acquisition time, prior the conversion phase, the voltage in the sample capacitor must be settled to the required resolution and the voltage difference between the sampling capacitor and input voltage should be less than 1/2LSB. This is a fundamental requirement to obtain accurate conversion results.

If you consider the ADC sample and hold structure exclusively, this settling time depends on the internal sampling capacitor, CSH, and the switch resistance, RS1. From the time constant,  $\tau = RS1 \times CSH$ , we can derive the settling time of this single pole system. The minimum acquisition time for the SAR converter is the time required for the sampling mechanism to capture the input voltage and settle.

The required settling time for the ADC equivalent input network can be calculated with the above set of equations. In this first order system, the user needs to allow a minimum number of RC time constants for the input voltage to settle within  $\frac{1}{2}$  LSB. For example, a 12 bit resolution ADC, requires 9 time constants to settle from an initial VSH0 voltage of zero volts to full-scale within  $\frac{1}{2}$  LSB. Similarly, the settling requirements for a 16 bit resolution ADC will be more stringent and the user will need to allow at least 12 time constants to ensure the sample-and-hold voltage settles within  $\frac{1}{2}$  LSB.

At the end of acquisition phase, Switch S1 opens, and the sample and hold is disconnected from the external circuit. Switch S2 connects the sample capacitor to the internal comparator and the conversion phase starts, where the sampled voltage is compared against the output of the N-bit search DAC. The N-bit search DAC produces binary weighted analog voltages proportional to a reference as each bit decision is made in the binary weighted search.

The binary search starts with the Most Significant Bit decision, and the tests are repeated for each binary weighted bit until the Least Significant bit decision is made. The value of each binary weighted bit is based on whether the analog input signal is higher or lower than the DAC voltage. The successive approximation register provides the digital code to the internal DAC during each conversion clock cycle.

The conversion time is a function of the conversion clock frequency and the resolution of the ADC. In the simplified 5-bit SAR ADC example above, 5 conversion clock cycles are required to reach the end of conversion.

In most SAR ADC devices, after the device reaches the end of conversion, the device returns to the acquisition mode. Depending on the specific SAR ADC circuit, the initial voltage on the sample-and-hold capacitor during the next sampling phase may be reset to a mid-point voltage or it may keep a value on the last sampled voltage. The device will trigger the next conversion after the next START conversion signal is received.

In summary, the SAR ADC's is a very popular topology used in many general purpose acquisition systems.

They provide a good trade-off between speed, resolution and power; providing data rates up to 4MSPS and resolutions up to 18 bits.

A key advantage of the SAR ADC is the precise control of the point in time sampling; and virtually zero latency. These characteristics may be beneficial in control systems and applications that require fast response.

For more information about precision ADCs, or to order a development kit, visit the TI Precision ADC web page at [ti.com/precisionadc](http://ti.com/precisionadc).

There are a number of resources available to help you evaluate and develop a system based on these ADCs. The TI Designs – Precision page features several reference designs that can help to speed the development of a system.

We hope that you have found this overview useful. Thank you for watching.

#### **Useful Links:**



<http://www.ti.com/precisionadc>



<http://www.ti.com/precisionadcsupport>