Choosing the Best ADC Architecture for Your Application

Part 3:

Hello, my name is Luis Chioye, I am an Applications Engineer with the Texas Instruments Precision Data Converters team.

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In the next two sessions, we will provide an overview on how the Delta-Sigma converter works.

The typical topology of the Delta-Sigma Converter consists primarily of two blocks: a Delta-Sigma Modulator and a Digital Decimating Filter. In today's session we will discuss the Delta-Sigma

The Delta Sigma Modulator samples the analog signal at a high data rate and modulates the analog input into a coarse, 1-bit, high frequency, Pulse Code Modulated Stream or PCM.

Following the modulator is the digital decimation filter. This digital filter stage accumulates a number of samples from the low-resolution modulator stream over a period of time, averages between a number of samples, and produces a lower speed, very high resolution output conversion result.

A key difference between the Delta-Sigma topology when compared with other ADC topologies, is that the device performs oversampling of the input signal. Conventional Analog–to-digital converters sample the input signal at a frequency close to the Nyquist Rate. The Delta-Sigma converter involves two

data rates: it samples the input signal at frequencies much higher than the Nyquist rate and produces high resolution conversion results at a slower data rate.

Oversampling converters can use simple and relative high tolerance analog components to achieve high resolution, but they require a digital signal processing stage.

Before explaining how the delta-sigma converter works, it is important to understand the concept of oversampling.

When sampling a signal at discrete intervals, the Nyquist-Shanon sampling theorem states that the sampling frequency (Fs) must be greater than twice the highest frequency of the input signal in order to be able to reconstruct the original signal from the sampled version.

Most ADC's sample at frequencies close to the Nyquist rate. The quantization noise for a N-Bit resolution ADC is evenly distributed over the sampled bandwidth between DC to the Nyquist rate of Fs/2. The signal-to-noise ratio (or SNR) for an ideal ADC is given by the equation shown, where N is the number of bits.

The Oversampling FFT plot, shown on the right, shows the effects of oversampling. The input signal frequency is the same, but the sampling frequency has been increased by an oversampling ratio k. Oversampling increases the bandwidth considerably, therefore, oversampling spreads the quantization noise over a wider bandwidth. The quantization noise power remains constant, but the quantization noise is now spread over a higher sampled bandwidth from DC to K times Fs/2. It is important to realize

that the total amount of noise power remains the same, but the noise has been spread over a wider frequency range, and the noise level at each frequency bin in the FFT has been reduced.

A digital low-pass filter can be used to eliminate the high frequency noise, while keeping the input frequency signals of interest. In this manner, oversampling can be used to increase resolution. After filtering the high frequency components, the improvement in SNR can be calculated by the above equation, where OSR is the oversampling ratio.

A typical first order delta-sigma modulator samples the analog input at a fast data rate, producing a single-bit modulated pulse wave. The delta-sigma modulator also performs the function of a noise shaping filter, pushing the noise spectrum components to higher frequencies and reducing the noise at the lower frequencies.

In order to understand the function of the delta-sigma modulator, it makes sense to build a linear model in the frequency domain. This analysis can help a great deal in understanding the concept of Noise Shaping.

A first-order delta sigma modulator consists of an integrator, a comparator that acts as a 1-Bit ADC, and a 1-bit DAC.

The modulator can be model as a two-input, one-output linear system. To achieve noise shaping, the output signal Y is fed back and summed with the analog input signal X. The result is fed through an integrator block that behaves as an analog low-pass function A(f).

Using this linear model, the resulting output Y can be represented by equation (1).

After re-arranging terms, equation (2) shows two components: the input signal transfer function and the noise transfer function in the frequency domain. The low frequency elements of the input signal are preserved with a low-pass filter function, while the lower frequency elements of the quantization noise are filtered with a high-pass filter function

The noise power is preserved in the conversion; therefore, the lower frequency noise is “shaped” to the higher frequencies.

Noise shaping is why the delta sigma is able to provide a high resolution conversion result.

This plot shows the modulator stream output in the time domain. The output of the modulator is a 1 bit PCM train, where the ‘ones’ density data is a function of the input signal applied. When the input signal is close to positive full-scale, the ‘ones’ density is at its highest. When the signal is close to the negative full scale, the ‘ones’ density is at its lowest.

The modulator stream in this plot example represents a sine wave.

Analyzing the output signal of the modulator in the frequency domain shows the signal spectrum and the resulting shaped noise. The noise term is the key to the modulator’s operation. Most of the quantization energy is shifted to the higher frequencies so the in-band noise is reduced significantly. The quantization noise for a first-order modulator starts at zero, rises rapidly, and then levels off at a

maximum value at the modulator frequency.

This diagram shows the spectral noise densities for 1^{st}, 2^{nd}, and 3^{rd} order modulators with a sampling frequency of F_S. Multi-order modulators shape the quantization noise to higher frequencies, while keeping the in-band noise at low frequencies. The higher the order of the modulator, the more quantization noise energy is suppressed at low frequencies. The highest line in this plot shows the third-order modulator response. At low frequencies, near our signal of interest, the 3^{rd} order modulator has very low noise. It gradually becomes noisier at higher frequencies.

In the magnified plot at the left, the quantization noise for the higher-order modulator starts lower than the other modulators. The noise rises more rapidly and levels off at the modulator frequency.

The high frequency modulator noise can be filtered by a digital filter. Higher order modulators can be used to obtain high resolution at low data rates.

The delta-sigma modulator over samples the input signal, and performs the function of a noise shaping filter, pushing the noise spectrum components to higher frequencies and reducing the noise at the lower frequency noise during the conversion process.

The modulator is followed by a digital/decimation low pass filter which filters this high frequency noise in the modulator stream of data.

On our next session we will review o block in the Delta-Sigma Topology: The digital Filter.

There are a number of resources available to help you evaluate and develop a system based on these ADCs.

The TI Designs – Precision page features several reference designs that can help to speed the development of a system.

For more information about precision ADCs, or to order a development kit, visit the TI Precision ADC web page at ti.com/precisionadc.

I hope that you have found this overview useful. Thank you for watching.

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