Designing a 99% Efficient Totem Pole PFC with GaN

Serkan Dusmez, Systems and applications engineer
What will I get out of this session?

• Purpose:
  - Why GaN Based Totem-pole PFC?
  - Design guidelines for getting 99% efficiency at 1kW / 100kHz including:
    - Thermal management,
    - PCB design,
    - intelligent control algorithms,
    - passive component selections
  - Loss breakdown of HB GaN power stage and 1kW PFC

• Part numbers mentioned:
  - LMG3410
  - UCD3138
  - UCC27714

• Reference designs mentioned:
  - PMP20873

• Relevant End Equipment:
  - Industrial/Telecom/Server
Agenda

• CCM PFC Topologies
  - Topology Comparison
  - Why GaN based TP PFC?

• Path to 99% Efficiency with GaN
  - GaN Based 1kW TP PFC Specs
  - Thermal Management Considerations
  - PCB Design Considerations
  - Half Bridge GaN Power Stage Losses
  - Control Tips
  - Power Inductor, EMI and DC Capacitor Selections

• Results
  - Total Loss Breakdown
  - Efficiency, Power Factor, THD, Current Waveforms
CCM PFC Topologies

- **Diode-bridge PFC**
  - Low cost
  - Good EMI performance
  - Moderate power density
  - Low efficiency
  - Heat not distributed

- **Dual boost PFC**
  - Good EMI performance
  - Distributed heat
  - Moderate efficiency
  - Moderate cost
  - Low power density

- **Totem-pole PFC**
  - High power density
  - High efficiency
  - Distributed heat
  - Moderate cost
  - EMI performance
## Why GaN Totem-pole PFC?

### Switching Losses

- **I-V Overlap Losses:** \( (I_{\text{RMS}} \times V_{\text{DC}} \times t_{\text{SW}} \times f_{\text{PWM}})/2 \)
- **Output Charge Losses:** \( (V_{\text{DC}} \times Q_{\text{OSS}} \times f_{\text{PWM}}) \)
- **Reverse Recovery Losses:** \( (V_{\text{DC}} \times Q_{\text{rr}} \times f_{\text{PWM}}) \)

### Loss Mechanism

<table>
<thead>
<tr>
<th>Loss Mechanism</th>
<th>Diode-bridge Boost PFC w/ Sj</th>
<th>Dual Boost PFC w/ Sj</th>
<th>Dual Boost w/ GaN</th>
<th>TP PFC w/ GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching FET Cond.</td>
<td>0.6 W</td>
<td>0.6 W</td>
<td>0.6 W</td>
<td>2.06 W</td>
</tr>
<tr>
<td>SiC Diode Cond.</td>
<td>2.75W</td>
<td>2.75W</td>
<td>2.75W</td>
<td>-</td>
</tr>
<tr>
<td>Rect. Diodes / FETs</td>
<td>8.19 W (Diode)</td>
<td>0.45 W (FET)</td>
<td>0.45 W (FET)</td>
<td>0.45 W (FET)</td>
</tr>
<tr>
<td>FET ( E_{\text{oss}} )/ SiC Diode ( Q_{\text{oss}} )</td>
<td>3.9 W</td>
<td>3.9 W</td>
<td>3.36W</td>
<td>2.4W</td>
</tr>
<tr>
<td>I-V Overlap</td>
<td>1.47 W</td>
<td>1.47 W</td>
<td>0.95W</td>
<td>0.95W</td>
</tr>
<tr>
<td>Total Power Losses</td>
<td><strong>16.9W</strong></td>
<td><strong>9.17W</strong></td>
<td><strong>8.11W</strong></td>
<td><strong>5.86W</strong></td>
</tr>
</tbody>
</table>

- **Same heat sinking is considered for Si (70mΩ) and GaN (70mΩ).**
- **Switching frequency is 100 kHz.** \( V_o=400V, P_o=1kW \).
- **Sj denotes super-junction FETs.**
- **\( Q_{\text{oss}} \) of Sj=360nC; \( E_{\text{oss}} \) of Sj=13µJ**
- **\( Q_{\text{oss}} \) of TI GaN=60nC; \( E_{\text{oss}} \) of TI GaN=7.6µJ**
- **\( Q_{\text{oss}} \) of SiC diode=83nC; \( E_{\text{oss}} \) of SiC Diode=7µJ**
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### 1kW GaN-based Totem-Pole CCM PFC

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>85 – 265 V(_{\text{AC}})</td>
</tr>
<tr>
<td>Input Frequency</td>
<td>50 – 60 Hz</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>385 V(_{\text{DC}})</td>
</tr>
<tr>
<td>Output Power</td>
<td>1 kW</td>
</tr>
<tr>
<td>Input Inductance</td>
<td>481 (\mu)H</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>100 kHz / 140 kHz</td>
</tr>
</tbody>
</table>

- **GaN FET Daughter Card** LMG3410-HB-EVM
- **Switching Stage and Inductor**
- **156 W/in\(^3\) 2X power density**
- **PMP20873**
Path to 99% Efficiency with GaN: **Thermal Management**

- **Thermal interface material (TIM) selection:**

| Thermal Resistances in Various Heatsinking Approaches |
|---------------------------------|-----------------|-----------------|-----------------|
| Rth (°C/W) | Bondply-100 | HF-300P | Direct Soldering |
| $R_{jb}$ | 0.5 | 0.5 | 0.5 |
| $R_{pcb}$ | 1.95 | 1.95 | 1.95 |
| $R_{TIM}$ | 5.5 | 3 | 0.2 |
| $R_{hs}$ | **6.4** | **6.4** | ***6*** |
| $R_{ja}$ | 14.3 | 11.8 | 8.65 |

*At 400 LFM

**Heat sink size 25x25x15mm shared by HB GaN FETs

***20x10x15mm for each GaN FET
Thermal board design

- Cu layer should cover thermal pad
- Copper thickness ≥ 2 oz copper
- Reduced PCB thickness (32 mils)
- Plated thermal vias for better thermal conduction (dia 8-12 mils)
- Thermal vias numbers and optimized pattern (tradeoff with power loop inductance)
  - 39 vias → 76.2 °C/W each
  - $R_{\text{pcb}}$ → 1.95 °C/W total
Path to 99% Efficiency with GaN: PCB Design

- Minimize power loop return
- Minimize SW node capacitance

\[ V = L_{lk} \frac{di}{dt} \]
Path to 99% Efficiency with GaN: GaN FET LMG3410

- 600V/70mΩ tailored for 1-1.5kW hard-switching.
- HB loss breakdown for 1kW / 387V / 100kHz.

Conduction losses: \( P_{\text{COND}} = I_{\text{RMS}}^2 \times R_{\text{DS(ON)}} \)

Dead time losses: \( P_{\text{DB}} \sim I_{\text{RMS}} \times V_{3Q} \times t_{\text{ON}} \times f_{\text{PWM}} \)

Switching losses: \( P_{\text{SW}} \sim \left( I_{\text{RMS}} \times V_{\text{DC}} \times t_{\text{R}} \times f_{\text{PWM}} \right)/2 + (V_{\text{DC}} \times Q_{\text{OSS}} \times f_{\text{PWM}}) + (V_{\text{DC}} \times Q_{rr} \times f_{\text{PWM}}) \)

- Direct soldering: 1.52W
  - Bond-plied-100: 1.78W

50V/ns - 100V/ns

Discrete GaN (1.9W)  TI GaN (0.95W)

2.3W at 387V  0W
Path to 99% Efficiency with GaN: Control

- Advance digital power control (UCD3138)
  - Highly integrated digital solution offering superior performance
  - Advanced control algorithm
  - Excellent THD and PF

- Adaptive dead-time
  - Different dead-times for HS and SS edges
  - Dead-time calculated based on operating condition

- Negative current conduction
  - Helps reducing switching losses

\[ T_d = \frac{C_{SW} \times V_o}{I_{L\_peak}} \]

*C_{SW} = top and bottom device C_{oss\_tr} + PCB, heatsink, inductor coupling capacitance
Path to 99% Efficiency with GaN: Passive Components

- Inductor Design

2 layer winding

Partial single layer winding

Single layer flat winding

Loss/EMI:
- 2 layer winding > Partial single layer winding > Single layer flat winding

Cost:
- 2 layer winding < Partial single layer winding < Single layer flat winding

Graphs showing waveform comparison.
Path to 99% Efficiency with GaN: Passive Components

- **Inductor Design**
  - High flux density and low loss Amorphous core
  - 80 turns
  - 480μH zero bias inductance
  - Core loss ~ 1.65W
  - Copper loss ~ 1.2W

- **EMI Inductor Design**
  - Low DCR
  - 16 AWG
  - 10x2 turns
  - 1.2mH
  - copper loss 0.2W x 2

- **DC Capacitor**
  - Low ESR at 120Hz
  - Cap > hold up time constraint
  - Cap > voltage ripple constraint
  - 560μF
  - Typical form factor 30-35 x 45-50

<table>
<thead>
<tr>
<th>Type</th>
<th>Cap [μF]</th>
<th>ESR [mΩ]</th>
<th>Dia [mm]</th>
<th>Height [mm]</th>
<th>Power Loss [W]</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>680</td>
<td>90</td>
<td>30</td>
<td>52</td>
<td>0.61</td>
</tr>
<tr>
<td>A</td>
<td>560</td>
<td>112</td>
<td>30</td>
<td>47</td>
<td>0.76</td>
</tr>
<tr>
<td>B</td>
<td>560</td>
<td>200</td>
<td>30</td>
<td>45</td>
<td>1.35</td>
</tr>
<tr>
<td>B</td>
<td>560</td>
<td>80</td>
<td>35</td>
<td>50</td>
<td>0.54</td>
</tr>
<tr>
<td>C</td>
<td>560</td>
<td>137</td>
<td>35</td>
<td>47</td>
<td>0.93</td>
</tr>
</tbody>
</table>

Partial single layer winding | 18AWG 13x2 1.68mH | 16AWG 10x2 1.2mH
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Loss breakdown of 1kW PFC / 387V / 100kHz

- 99% efficiency 60% to 100% load

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<th>Loss Mechanism</th>
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</tr>
</thead>
<tbody>
<tr>
<td>EMI Inductor Loss</td>
<td>0.4W</td>
</tr>
<tr>
<td>PFC Inductor Copper Loss</td>
<td>1.2W</td>
</tr>
<tr>
<td>PFC Inductor Core Loss</td>
<td>1.64W</td>
</tr>
<tr>
<td>DC Capacitor</td>
<td>0.54W</td>
</tr>
<tr>
<td>GaN Conduction + 3\textsuperscript{rd} Quadrant Loss</td>
<td>1.76W</td>
</tr>
<tr>
<td>GaN $Q_{\text{loss}}$ + Switch Node Cap Loss</td>
<td>2.54W</td>
</tr>
<tr>
<td>GaN I-V Overlap Loss</td>
<td>0.95W</td>
</tr>
<tr>
<td>Relay + Si FET + PCB + Fuse Losses</td>
<td>0.95W</td>
</tr>
<tr>
<td>Total Power Losses</td>
<td>9.98W</td>
</tr>
</tbody>
</table>

*Note: Excludes bias losses

\[ T_{\text{amb}} = 25^\circ \text{C} \]
Good power factor and THD

- Energy Star Server (1kW+)
- Inductor: 480uH
- Lead OEM Spec

![Graph showing power factor and THD vs. output power for different voltages and frequencies.](chart.png)
AC Current Waveforms at Full Load

- **115Vac**: 100KHz
- **230Vac**: 100KHz
- **115Vac**: 140KHz
- **230Vac**: 140KHz
Thank you for your attention!

References for more information:

1) Texas Instruments, Gallium Nitride (GaN) Solutions, www.ti.com/gan
4) Texas Instruments, Using the LMG3410-HB-EVM Half-Bridge and LMG34XXBB-EVM Breakout Board EVM, User Guide (SNOU140A)
5) Texas Instruments, Optimizing GaN Performance with an Integrated Driver, White Paper (SLYY085)
6) Texas Instruments, GaN FET Module Performance Advantage over Silicon, White Paper (SLYY071)
7) Texas Instruments, 99% Efficient 1kW GaN-based CCM Totem-pole Power Factor Correction (PFC) Converter Reference Design, TI design (PMP20873)