Hysteresis loss in high voltage MOSFETs:
Findings and effects for high frequency AC-DC converters

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What will I get out of this session?

Purpose:

• Highlight Coss hysteresis loss
  • Occurs for all SJ MOSFETs, from ALL manufacturers, but to greater/lesser extent
• Illustrate how it can be measured
• Show how it impacts MOSFET choice for ZVS topologies

• Part numbers mentioned:
  • UCC24612 SR driver
  • UCC27712 600-V half-bridge driver

• Reference designs mentioned:
  • TI high-efficiency active-clamp Flyback EVM (under development)

• Relevant End Equipments:
  • High-density adapters
  • High-efficiency PSUs
Introduction

- Industry trend → high efficiency & small size adapters & PSUs
  - Standard 65-W adapter → 8 W/in³
  - Zolt 70-W → 14 W/in³
  - Finsix Dart → 17 W/in³

- Higher power density
  - Higher frequency → smaller magnetics
  - Small size → less surface area to dissipate heat
    → need higher efficiency with less dissipation

- Need soft-switching or zero-voltage-switching (ZVS) topologies to enable high Fsw

- ZVS – eliminate switching loss
  - Allows higher Fsw → smaller magnetics (still limited by HF core loss, AC resistance)
  - Allows larger switching devices with lower conduction loss – no capacitive losses, right?
Example ZVS topology – Active-Clamp Flyback

- QR Flyback only achieves partial ZVS
- Add active-clamp switch to achieve full ZVS
- Also recycle transformer leakage inductance energy

ZVS criteria: \[ \frac{1}{2} L_m i_m^2 - \frac{1}{2} C_{sw} V_{sw}^2 \geq 0 \]
Zero-voltage-switching (ZVS) trade-offs

- ZVS – eliminate switching loss
  - Allows higher $F_{sw} \rightarrow$ smaller magnetics
  - Push $F_{sw}$ higher – how high can or should you go?
  - Magnetics still limited by HF core loss, AC resistance loss
  - Allows larger switching devices with lower conduction loss
  - No capacitive losses, right?
  - Can push the capacitance way up, right?

- Not quite!
Superjunction high-voltage MOSFET

• **Brief history:**
  • Superjunction concept patents date from 1978-1990s
  • First commercialized 1998/9 by Infineon (CoolMOS), 2000 by ST (MDMesh)
  • Breaks the theoretical Si limit of Rds(on) at high voltage
  • Uses vertical pillars of P/N to for more uniform field distribution
  • Allows much higher N-doping level (10x to 100x) vs std. MOSFET
  • Gives higher breakdown (uniform field) at very low Rds(on) (N-doping)

• **Many Superjunction vendors:**
  • Infineon/IR, ST, Toshiba, AOS, Fairchild/On, Vishay, Fuji, Rohm, NXP, EPC, Fujitsu, & others

• **Non-linear Coss vs VDS**
  • More pronounced with newer gen lower Rds(on), smaller feature size

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Eoss loss – background

• What is Eoss?
  • Energy-related loss due to charge stored in Coss
  • Depends on the bus voltage & device

• Eoss completely dissipated in hard-switching topologies

• Eoss partly recovered in quasi-resonant topologies

• ZVS topologies ideally avoid all Eoss loss
  • Can switch at very high frequency
  • Lower Eoss ⇒ less circulating energy to achieve ZVS

• Big variation in Eoss loss for different devices
  • New generations continually achieve lower Eoss
  • Curves show latest gen C7/P7/G7 close to WBG

• However MOSFET Coss charge and discharge has hysteresis

Fig. 13 reproduced with permission from “Superjunction Power Devices, History, Development and Future Prospects”, Florin Udrea, Gerald Deboy, Tatsuhiko Fujihira, IEEE Transaction on Electron Devices, Vol. 64, No. 3, March 2017, © IEEE; Fig. 1 reproduced with permission from “Coss Hysteresis in Advanced Superjunction MOSFETs”, J. B. Fedison, M. J. Harrison, Enphase Energy Inc., APEC 2016, © IEEE
Coss hysteresis loss – the discovery

- Phenomenon first reported APEC 2014 by Enphase*
- Measured Coss to help choose best devices for HF ZVS
- Observed asymmetric charge/discharge waveforms
- Significant temperature rise for expected lossless charge & discharge of Coss
- Waveforms & losses did not match models & simulation
- Big variation in Coss loss for different devices A-E
- Proposed new ZVS Figure of Merit

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**Table 2. Characteristics of the superjunction MOSFETs measured.**

<table>
<thead>
<tr>
<th>Device</th>
<th>$V_{DS}$ at 25°C (V)</th>
<th>$R_{DSS}$ max at 25°C (Ω)</th>
<th>$C_{iss}$ at $V_{DS}=0$ (nF)</th>
<th>$E_{inert}$ a (μJ)</th>
<th>$E_{dissipated}$ b (μJ)</th>
<th>Area Specific On-Resistance typ at 25°C (mΩ cm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device A</td>
<td>650</td>
<td>0.148</td>
<td>2.0</td>
<td>1.47</td>
<td>4.050</td>
<td>19</td>
</tr>
<tr>
<td>Device B</td>
<td>600</td>
<td>0.160</td>
<td>2.1</td>
<td>2.75</td>
<td>0.5664</td>
<td>27</td>
</tr>
<tr>
<td>Device C</td>
<td>600</td>
<td>0.178</td>
<td>2.0</td>
<td>2.46</td>
<td>0.242</td>
<td>26</td>
</tr>
<tr>
<td>Device D</td>
<td>600</td>
<td>0.188</td>
<td>3.3</td>
<td>4.06</td>
<td>0.140</td>
<td>30</td>
</tr>
<tr>
<td>Device E</td>
<td>600</td>
<td>0.160</td>
<td>1.9</td>
<td>2.67</td>
<td>0.079</td>
<td>33</td>
</tr>
</tbody>
</table>

*aV_{GS}=0, V_{DS}=200V.  bCalculated from small-signal Ciss versus V_{DS}.  cMeasured energy dissipation of Ciss per ZVS cycle.

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* Authors now with ST
Coss hysteresis loss – other published results

- What causes hysteresis in Coss charge/discharge? Why are some devices better?
- Jaume Roig & Filip Bauwens proposed cause due to “stranded charges”, much worse in MEMI (multi-implant multiepitaxy) technology vs. TFEG (trench-filling epitaxial growth)
- Possibly explains why different devices show grossly varying hysteresis loss?
- How can hysteresis loss be measured? Fedison et al (Enphase) used Sawyer-Tower method (detailed in the paper) for same FETS A-E:
TI investigation of Coss loss – test circuit

• Connect 2 identical DUTs back-to-back in series
  • Back-to-back body diodes ⇒ no diode conduction
  • G-S short => FET off ⇒ no channel conduction
• Connect to driving high-freq high-voltage square-wave
  • Driving square-wave generated by half-bridge circuit
• Observe Vds of low-side DUT & inductor current
• Measure low-side DUT temperature rise to assess level of Coss hysteresis loss.
• Measure low-side DUT temperature rise ΔT
• Calibrate result
  • Same environmental setup (same thermal conditions)
  • Current I though body diode Vf to get same ΔT
  • $P_{\text{diss}} = I \times V_f$
  • $E_{\text{oss}(\text{hyst})} = \frac{P_{\text{diss}}}{F_{\text{sw}}}$
TI investigation of Coss loss – test setup

1. DUTs socketed with thermocouples glued to plastic body (not metal tab)
2. Styrofoam box to isolate DUTs from external HB FETs & inductor
3. Plastic safety enclosure over entire setup to block ambient air-conditioning airflow

Four K-type thermocouples measured – #1 Low DUT, #2 High DUT, #3 Ambient inside styrofoam, #4 DUT PCB
Devices tested – Infineon CoolMOS 600-V, 650-V & 700-V rated

- Note that Coss hysteresis loss is observed for ALL SJ MOSFETs – regardless of manufacturer
  - Actual loss varies, depending on internal design specifics
- Results summarised here – all Infineon
  - *Not intended to single out Infineon, just take one manufacturers broad portfolio as an example*
  - *To show comparative performance across families for a single manufacturer*
- CoolMOS 700-V:
  - P7 – IPA70R360P7, IPA70R600P7, IPS70R900P7, IPS70R1K4P7
- CoolMOS 650-V:
  - C7 – IPP65R225C7, IPA65R190C7, IPP65R125C7, IPP65R045C7
  - G7 – IPT65R195G7
- CoolMOS 600-V:
  - C3 – SPP20N60C3
  - C6 – IPP60R190C6, IPP60R380C6, IPP60R600C6, IPP60R950C6
  - C7 – IPP60R180C7
  - G7 – IPT60R150G7
Key test results – C6 series

<table>
<thead>
<tr>
<th>DUT</th>
<th>Vds</th>
<th>Series</th>
<th>Rdson</th>
<th>Eoss @ 450 V (uJ)</th>
<th>Eoss hyst (uJ)</th>
<th>Eoss Hyst %</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPP20N60C3XKSA1</td>
<td>600</td>
<td>C3</td>
<td>190</td>
<td>8.7</td>
<td>0.833</td>
<td>9.6%</td>
</tr>
<tr>
<td>IPP60R190C6</td>
<td>600</td>
<td>C6</td>
<td>190</td>
<td>5.9</td>
<td>0.636</td>
<td>10.8%</td>
</tr>
<tr>
<td>IPP60R380C6</td>
<td>600</td>
<td>C6</td>
<td>380</td>
<td>3.2</td>
<td>0.298</td>
<td>9.3%</td>
</tr>
<tr>
<td>IPP60R600C6</td>
<td>600</td>
<td>C6</td>
<td>600</td>
<td>2.1</td>
<td>0.288</td>
<td>13.7%</td>
</tr>
<tr>
<td>IPP60R950C6</td>
<td>600</td>
<td>C6</td>
<td>950</td>
<td>1.5</td>
<td>0.138</td>
<td>9.2%</td>
</tr>
</tbody>
</table>

- Good Eoss reduction (-33%) vs old C3/CP generations
- 600-V C6 family shows low hysteresis loss <10%
- Good choice for ZVS compared to older gen devices
- E.g. – 0.636 uJ @ 500 kHz = 0.32 W – not negligible! Significant temp rise
- E.g. – 50 W @ 93% eff –> extra 0.32 W loss –> ~0.55% eff drop
Key test results – C7 series

<table>
<thead>
<tr>
<th>DUT</th>
<th>Vds</th>
<th>Series</th>
<th>Rdson</th>
<th>Eoss @ 450 V (uJ)</th>
<th>Eoss hyst (uJ)</th>
<th>Eoss Hyst %</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPP65R225C7</td>
<td>650</td>
<td>C7</td>
<td>225</td>
<td>2.6</td>
<td>1.478</td>
<td>56.8%</td>
</tr>
<tr>
<td>IPA65R190C7</td>
<td>650</td>
<td>C7</td>
<td>190</td>
<td>3.1</td>
<td>1.390</td>
<td>44.8%</td>
</tr>
<tr>
<td>IPP65R125C7</td>
<td>650</td>
<td>C7</td>
<td>125</td>
<td>4.7</td>
<td>1.766</td>
<td>37.6%</td>
</tr>
<tr>
<td>IPP65R045C7</td>
<td>650</td>
<td>C7</td>
<td>45</td>
<td>13</td>
<td>4.656</td>
<td>35.8%</td>
</tr>
<tr>
<td>IPP60R180C7</td>
<td>600</td>
<td>C7</td>
<td>180</td>
<td>3</td>
<td>0.264</td>
<td>8.8%</td>
</tr>
</tbody>
</table>

- Significant Eoss reduction vs older C6 generation
- 600-V C7 shows low hysteresis loss <9%, but also lower Eoss to begin with
  - 600-V C6 vs C7 – 0.636 uJ vs 0.264 uJ – 60% reduction
- 650-V C7 shows significantly higher hysteresis loss
  - Compare 180/190 mR 600/650-V devices – 8.8% vs 45%! 
### Key test results – P7 series

<table>
<thead>
<tr>
<th>DUT</th>
<th>Vds</th>
<th>Series</th>
<th>Rdson</th>
<th>Eoss @ 450 V (uJ)</th>
<th>Eoss hyst (uJ)</th>
<th>Eoss Hyst %</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPA70R360P7</td>
<td>700</td>
<td>P7</td>
<td>360</td>
<td>2</td>
<td>0.603</td>
<td>30.1%</td>
</tr>
<tr>
<td>IPA70R600P7</td>
<td>700</td>
<td>P7</td>
<td>600</td>
<td>1.23</td>
<td>0.374</td>
<td>30.4%</td>
</tr>
<tr>
<td>IPS70R900P7</td>
<td>700</td>
<td>P7</td>
<td>900</td>
<td>0.97</td>
<td>0.235</td>
<td>24.2%</td>
</tr>
<tr>
<td>IPS70R1K4P7</td>
<td>700</td>
<td>P7</td>
<td>1400</td>
<td>0.64</td>
<td>0.196</td>
<td>30.6%</td>
</tr>
</tbody>
</table>

- Comparable Eoss values vs C7 650-V generation
- Achieves same Eoss at higher VDS 700 V
- 700-V P7 shows reduced higher hysteresis loss vs 650-V C7
  - Compare 225-mR 650-V C7 (57%) vs 360-mR 700-V P7 (30%)
Key test results – G7 series

<table>
<thead>
<tr>
<th>DUT</th>
<th>Vds</th>
<th>Series</th>
<th>Rdson</th>
<th>Eoss @ 450 V (uJ)</th>
<th>Eoss hyst (uJ)</th>
<th>Eoss Hyst %</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPT60R150G7</td>
<td>600</td>
<td>G7</td>
<td>150</td>
<td>3.15</td>
<td>0.170</td>
<td>5.4%</td>
</tr>
<tr>
<td>IPT65R195G7</td>
<td>650</td>
<td>G7</td>
<td>195</td>
<td>2.6</td>
<td>0.889</td>
<td>34.2%</td>
</tr>
</tbody>
</table>

- Initially marketed as “P7 Gold”, later converted to G7
- Best-in-class Eoss (lower than C6/C7/P7)
- Comparable Eoss – 600-V G7 vs 600-V C7, but at lower Rds(on) (-17%)
- Comparable Eoss – 650-V G7 vs 650-V C7, but at lower Rds(on) (-14%)
- Again – observe a penalty at higher voltage – 650-V vs 600-V 34% vs 5%
Results summary

Eoss Loss vs. Hysteresis Loss Portion

- C7-650V
- C7-600V
- C6-600V
- G7-650V
- G7-600V
- P7-700V

Energy (uJ) vs. Rds(on) (m-ohm)
Conclusions & key take-aways

- Coss hysteresis is REAL and can be very apparent in ZVS topologies
- MOSFET datasheets do not include Coss hysteresis loss data; it cannot be predicted from other data
- Industry must encourage MOSFET vendors to test for and publish this data – and to reduce the loss!
- Different MOSFET generations are better suited to various hard-switched, QR & ZVS topologies
- Newer generation devices are improving – lower Rds(on), lower Eoss & lower hysteresis loss
- Specific observation – Coss Hysteresis Loss vs VDS Rating:
  - Similar Rds(on), similar Eoss curves – observe higher loss for 650-V vs 600-V rated device
  - Depends on internal design and process, cannot be related to VDS rating alone
- Advantage of Active-Clamp Flyback (ACF) ZVS topology –
  - “Clean” waveforms allow use of 600-V MOSFETs with lowest Eoss and lowest hysteresis loss
  - EVM (under development) using 600-V FETs, UCC27712 HB driver, UCC24612 SR driver