High Density DC-DC Power Module Design with Embedded Planar Transformer

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What will I get out of this session?

• Purpose:
  1. Understand state of the art & market trend for telecom power brick module industry
  2. Gain insights into the key considerations to optimizing a power module design
  3. Learn how to design a embedded planar transformer

• Part numbers mentioned:
  • LM5045, LM5035, UCC28251/0
  • UCC21225A, CSD19537Q3

• Reference designs mentioned:
  • PMP8878, LM5045EVM

• Relevant End Equipments:
  • Telecom Base Station, Enterprise Switching/Networking
## Power Brick Module - State of Art

<table>
<thead>
<tr>
<th>Form Factor</th>
<th>Power Level</th>
<th>Topology</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/32 brick</td>
<td>&lt;30W</td>
<td>Active clamp forward</td>
</tr>
<tr>
<td>1/16 brick</td>
<td>30W-100W</td>
<td>Active clamp forward</td>
</tr>
<tr>
<td>1/8 brick</td>
<td>100W-300W/300W-500W</td>
<td>Half/full bridge</td>
</tr>
<tr>
<td>Quarter brick</td>
<td>500W-800W</td>
<td>Full bridge</td>
</tr>
</tbody>
</table>

**Images:**
- Half brick
- Quarter brick
- 1/8 brick
Question #1: What form factors are the growing trend in the power brick module industry

- A) 1/32 brick
- B) 1/16 brick
- C) 1/8 brick
- D) Quarter brick
Power Brick Module - Market Trend

- Smaller form factors (8th and 16th brick) gaining more traction
- Push 16th brick power level above 200W
- Half bridge preferred for 16th brick due to higher efficiency
- 48V-POL gaining traction in higher current output (>100A) applications
Question #2: What are the key considerations to achieving a high-density power module design

- A) Integration of control functionalities
- B) Magnetic design
- C) Integrated gate drivers
- D) Smaller packages
Key Design Considerations for High-Density Power Module

- Power density (deliver highest power in least footprint)
  - Higher level of controller integration
  - Embedded planar magnetics
  - Isolated gate driver
  - Small package FETs
  - System Integration

- Pre-biased startup
- Optimized PWM scheme
- Enhanced fault protection (e.g. CBC)
High level of Integration

- Integration of control functions
  - Compensation, PWM, drivers, pre-biased soft start, etc
- Integrated bridge gate drivers
- Integrated startup regulator
- Integrated bias supply
- Isolated gate driver (UCC21225A)
  - replace digital isolator + gate driver
- Small footprint components (CSD19537Q3)
  - e.g. MOSFETs (3.3mm*3.3mm)
- Embedded planar magnetics
Embedded Planar Magnetics

- **Pros:**
  - ✓ Low profile
  - ✓ High power density
  - ✓ Ease mass production with min. manufacturing tolerance
  - ✓ Lower cost

- **Cons:**
  - ▪ Reduced core window utilization (due to dielectric layers of PCB)
  - ▪ Hard to iterate/debug during prototyping phase
Embedded Planar Transformer – Core Selection

- **Key Steps:**
  1. Determine the turn ratio $N$ based on the operation range of $V_{in}$ & $V_{o}$
  2. Calculate the RMS current of pri & sec windings and applied pri volt-secs
  3. Select the core material based on the power loss density requirement vs. temp
  4. Calculate the geometric constant to determine the core size

$$K_{gf} \geq \frac{\rho \lambda_1^2 I_{tot}^2 K_{fe}^{(2/\beta)} 10^8}{4K_u P_{tot}^{((\beta+2)/\beta)}}$$

Where $K_{gf}$ is the geometric constant, $\rho$ is the wire effective resistivity, $I_{tot}$ is the total rms winding current referenced to primary, $\lambda_1$ is applied primary volt-sec, $P_{tot}$ is allowed total power dissipation, $K_u$ is winding fill factor, $K_{fe}$ is core loss coefficient, $\beta$ is core loss exponent, $A_c$ is core cross-sectional area, $W_A$ is core window area, $MLT$ is magnetic path length per turn, $l_m$ is magnetic path length, $A_{wn}$ is wire area, and $\Delta B$ is peak ac flux density.
5. Determine the optimal peak flux density yielding the minimum power loss

\[ \Delta B = \left[ \frac{10^8 \rho \lambda_1^2 l_{tot}^2}{2 K_u} \cdot \frac{MLT}{W_A A_c^3 l_m} \cdot \frac{1}{\beta K_f e} \right]^{\frac{1}{\beta + 2}} \]

6. Determine the number of turns of each winding \( n_1 \) and \( n_2 \)

\[ n_1 \geq \frac{\lambda_1 10^4}{2 \Delta B A_c} \]

7. Determine the PCB winding sizes

\[ A_{w1} \geq \frac{\alpha_1 K_u W_A}{n_1} \quad A_{w2} \geq \frac{\alpha_2 K_u W_A}{n_2} \quad \ldots \]
Winding Interleaving (Reduce AC winding loss)
Winding Interleaving (MMF Diagram) – Power Transfer Phase I

Power Transfer Phase I
(high-side FET & SR2 on)
Winding Interleaving (MMF Diagram) – Power Transfer Phase II

Power Transfer Phase II (low-side FET & SR1 on)
Winding Interleaving (MMF diagram) – Freewheeling Phase

Freewheeling Phase
(both SRs on and primary FETs off)
Pre-Biased Startup Phase I – Primary FETs Soft-Start

1. SS start to ramp up as UVLO is passed and SS controls duty
2. Secondary bias comes up when SS passes 1V
3. Secondary REF soft starts followed by COMP voltage
4. SSSR cap is released once COMP voltage controls the duty and SS hits 2V

LM5045
5. Until SSSR cap voltage hits 1V, SR pulses are synchronized to respective primary FET pulse (reduced rectification loss)
6. After SSSR cap hits 1V, the pulse width of SR freewheeling gradually increases
7. The SR pulse eventually becomes complementary to the respective primary FET
Optimized Cycle-By-Cycle Current Limiting

Voltage balance of the cap divider for half-bridge converter

Subharmonic oscillation when $d > 0.25$ in HB

Voltage balance of the cap divider

Non-uniform current limit level at different input voltages
Optimized Cycle-By-Cycle Current Limiting

\[ I_{\text{sense}} = (V_{cs} + I_{\text{ramp}} R_1 + \frac{V_{in} R_1}{R_2}) \]

X axis: input voltage
Y axis: current limit

positive current limit

reverse current limit
Optimized PWM Scheme

\[ D_{MAX} = \frac{1}{f_{osc}} - \frac{T_1}{2f_{osc}} \]

\[ D_{MAX} = \frac{1}{f_{osc}} - \frac{T_{pw}}{2f_{osc}} \]
Conclusion

- An overview of the state-of-art and market trend of the power module industry is given
- Key considerations to achieving an optimized power module design are discussed
- A step-by-step design guide for an embedded transformer is reviewed
- The pre-biased startup, and optimized CBC and PWM schemes are discussed
- Several TI parts are introduced including LM5045 (full bridge controller), LM5035 (half bridge controller), UCC28250/1 (half bridge controller), UCC21225A (isolated gate driver) and CSD19537Q3 (100V MOSFET)
References

• Robert W. Erickson and Dragan Maksimovic, Fundamentals of Power Electronics
• LM5045 datasheet
• LM5045 EVM user guide
• LM5035 datasheet
• UCC28251/0
• UCC21225A datasheet
• CSD19537Q3 datasheet