Closed-loop Delfino Control Systems: Multiple Industrial Protocol Support using the AMIC110 Sitara Processor

Part 3: Industrial software and multiprotocol support
Training series overview

AMIC110 Multiprotocol Industrial Interface for Closed-loop Delfino Control Systems:
• Part 1: Product solutions supported by the AMIC110 and Delfino system architecture
• Part 2: Implementation of multiprotocol industrial communications solutions
• Part 3: Industrial software and multiprotocol support
Training agenda

• Part 1: Product solutions supported by the AMIC110 and Delfino system architecture:
  – Solution space
  – The capabilities and advantages of this system solution
  – Applications of this systems solution

• Part 2: Implementation of multiprotocol industrial communications solutions:
  – AMIC110 architecture
  – (TIDA-00299) AMIC110 ICE integration with dual-core MS320F2837x Delfino MCUs LaunchPad

• Part 3: Industrial software and multi-protocol support:
  – Software architecture
  – Multi-protocol support
  – Simple Open Real-Time Ethernet (SORTE)
Industrial software and multiprotocol support

Software architecture
AMIC110 software

• AMIC110 software will be delivered as PRU-ICSS Industrial packages based upon Processor SDK.

• The AMIC110 Processor SDK is included in the Processor SDK for AM335x Processors http://www.ti.com/tool/processor-sdk-am335x

• AMIC110 PRU-ICSS EtherCAT available on mysecuresoftware

• Standard release PRU-ICSS Industrial with AMIC110 support - 2Q 2017

• More AMIC110 details: http://www.ti.com/tool/tmdxice110
The AMIC110 provides a complete EtherCAT slave interface.

- The AMIC110 emulates an ET1100 slave controller.
- The EtherCAT slave stack runs on the C2000 Delfino.
**EtherCAT slave architecture**

- **Auto-Forwarder**
  Receives frames, performs frame checking, affixes time stamps, and forwards it to the loop-back function.

- **Loop-back Function**
  Forwards Ethernet frames to the next logical port.

- **Fieldbus Memory Management Unit (FMMU)**
  Supports bitwise mapping of logical addresses to physical addresses of the ESC.

- **EtherCAT Processing Unit**
  Coordinate access to the internal registers and the memory space of the ESC, from the EtherCAT master and from the local application.

- **SyncManager**
  - Manages register, data exchange and mailbox communication between EtherCAT master and slaves.
  - Read or write transactions may generate events for the EtherCAT master and the attached Delfino/Sitara ARM controller respectively.

- **Memory**
  - The first block of 4 Kbyte (0x0000-0x0FFF) is used for registers and user memory.
  - The memory space from address 0x1000 onwards is used as the process memory (8 Kbyte).
  - The ESC address range is addressable by the EtherCAT master and the attached Delfino/Sitara ARM.

- **Monitoring Unit**
  Contains error counters and watchdogs.

- **Distributed Clock (DC)**
  Allow for precisely synchronized generation of output signals, input sampling, and time stamp events.

- **SII EEPROM**
  Non-volatile memory for EtherCAT Slave Information (ESI) storage.

- **Status / LEDs**
  - Provides ESC and application status information.
  - Controls external RUN LED/ERR LED and port Link/Activity LEDs.
## EtherCAT slave features

<table>
<thead>
<tr>
<th>Feature</th>
<th>AMIC110</th>
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</thead>
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<tr>
<td>Ports</td>
<td>2 MII</td>
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<tr>
<td>FMMUs</td>
<td>8</td>
</tr>
<tr>
<td>SyncManagers</td>
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<tr>
<td>Process Data RAM (Kbyte)</td>
<td>8</td>
</tr>
<tr>
<td>ESC Register (Kbyte)</td>
<td>4</td>
</tr>
<tr>
<td>Distributed Clocks</td>
<td>64-bit</td>
</tr>
<tr>
<td>Process Data Interface (PDI)</td>
<td>SPI slave</td>
</tr>
</tbody>
</table>
AMIC110 processing model when stack is on Delfino

Layer 7 - Application

Layer 2 – Data Link

Layer 1 – Physical

C2000 SPI Slave I/F to C2000

API

ESC Registers

SPI API

Protocol Driver

Protocol Firmware

ARM

PRUSS

Layer 7 - Application

Layer 2 – Data Link

Layer 1 – Physical

SPI

Ethernet Phy

TI Source

TI Binary

Texas Instruments
AMIC110 processing model when stack is on AMIC110

Layer 7 - Application
- Industrial Application
  - SPI Master I/F to C2000
  - API
  - Protocol Stack
  - Processor SDK
    - TI-RTOS
    - Bootloader
    - Tools
    - Peripheral Drivers

Layer 2 – Data Link
- Protocol Firmware
  - SPI API
  - Protocol Driver

Layer 1 – Physical
- SPI
- Ethernet Phy

TI Example - Customer
- Third Party or Customer
- TI Source
- TI Binary

ARM

PRUSS
Industrial software and multiprotocol support
Certified industrial communication protocols

Faster time to market!
### Industrial protocols: 3P engagement model

<table>
<thead>
<tr>
<th>Protocol</th>
<th>3P</th>
<th>Initial Engagement</th>
<th>Production</th>
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<tbody>
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<td>PROFIBUS</td>
<td>TMG: <a href="mailto:info@tmgte.de">info@tmgte.de</a></td>
<td>Evaluation license included in TI SDK</td>
<td>Production license: 1-time fee of 5000€ plus maintenance</td>
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<td>Evaluation license included in TI SDK</td>
<td>Available for free with ETG membership which is also free. Support from ETG</td>
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<td>Ethernet/IP</td>
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<td>SERCOS III</td>
<td>Automata: Christoph Melzer <a href="mailto:chmelzer@automata.de">chmelzer@automata.de</a></td>
<td>Limited evaluation is free; Full license based on Time/IO/Vendor</td>
<td>Contact automata</td>
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<td>EtherCAT Master</td>
<td>Acontis: Stefan Zintgraf <a href="mailto:s.zintgraf@acontis.com">s.zintgraf@acontis.com</a></td>
<td>Evaluation images found on TI designs (TIDEP0043, TIDEP0079) &amp; on Acontis landing page</td>
<td>Production license: NRE for stack, plus fee per unit shipped. Contact Acontis for details.</td>
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<td>PLC SW</td>
<td>3S: CodeSys PLC Framework</td>
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<td>KW-Soft: Boris Waldeck <a href="mailto:bwaldeck@kw-software.com">bwaldeck@kw-software.com</a></td>
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<tr>
<td>IEC61850</td>
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<td>Contact Triangle Microworks</td>
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<tr>
<td>Powerlink</td>
<td>Port: Christian Bornschein <a href="mailto:cb@port.de">cb@port.de</a></td>
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Industrial software and multiprotocol support

Simple Open Real-Time Ethernet (SORTE)
SORTE summary

• Simple Open Real-Time Ethernet (SORTÉ) is a process data efficient and fast real-time Ethernet protocol leveraging PRU-ICSS and MII_RT.

• Delivered as PRU firmware source code:
  – Enables customer differentiated products
  – Fully customizable PRU Firmware

• Real-time Ethernet programming example for PRU-ICSS and MII_RT (“build your own” protocol)

• Currently available in Processor SDK for AM335x and AM437x
Fast and efficient real-time Ethernet protocol implementation on PRU-ICSS:
- Master and device(s) network line topology
- 4µs cycle time for process data exchange with one master and four devices
- 100Mbit, full duplex

Removes external ASIC or FPGA support and integrates industrial Ethernet.

Training and programming example for real-time Ethernet on PRU-ICSS:
- Fully customizable PRU firmware
- PRU firmware provided in source code
- Reference PRU firmware with user guide, PRU firmware, and ARM driver software
For more information


- TI Designs:

- AMIC110 Industrial Communications Engine (ICE): http://www.ti.com/tool/tmdxice110

- Sitara Industrial FAQ: http://processors.wiki.ti.com/index.php/FAQ_Sitara_Industrial

- For questions about this training, refer to the TI E2E Community Sitara Processor Forum: https://e2e.ti.com/support/arm/sitara_arm/f/791