What? nanoWatt?

Acquiring sensor data in wireless products with nanowatts of power consumption

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Agenda

Objective:
Discuss methods for optimizing the electronic design of low-power sensor data acquisition systems

Topics:
1. Overview of Low-power Sensor Data Acquisition Systems
2. Common system-level design challenges
3. Designing a low-power sensor data acquisition system
4. Low-power signal chain devices
5. Links for more information
Low-Power Sensor Data Acquisition

Wearable Electronics

Building Automation Sensors

Implantable Medical Devices

Surveillance Equipment

Industrial and Wireless Sensor Nodes

Portable Electronics
Goals of Low-Power Sensor Data Acquisition

- Improve overall battery life
- Increase the number of data collection nodes
- Reduce size and cost of the battery
- Improve the quality of data measurements
Basic Data Acquisition System

POWER SUPPLY
- LDO / REF

SENSOR
- INPUT DRIVER
- FILTER
- SAR ADC
- ADS7042
Common System Design Challenges

• Power consumption
  – Battery-powered with a need for long battery life
  – Each component should consume as little power as possible
  – Often trade-off between low power and high-performance

• Size
  – Component selection must meet package size requirements
  – Sometimes a trade-off with power consumption or performance

• Performance
  – Dictates the quality of measurements taken by the system
  – Mandates the resolution and/or data rate of the system
Three Optimizations

**High-Bandwidth**: 12 bit, 1Msps optimized for hard disk drives, motor control, motor encoders, and optical encoders.

**Mid-Range**: 12 bit, 500ksps optimized for current monitoring, battery monitoring, electromyography (EMG), and skin impedance.

**Low-Power**: 12 bit, < 1ksps optimized for tilt, gyro, pressure, temperature, gas, chemical, blood glucose, low voltage, and DC sensor measurements.
System Power Consumption

High-Bandwidth
Optimized for maximum ADC data rate
1 Msps
2.5 mW

Mid-Range
Optimized for balance between power and data rate
< 500 ksp
1 mW

Low-Power
Optimized for lowest power by eliminating the drive buffer
< 1 kps
< 1 µW

Key power consumption areas:
- Input Driver
- Data Sampling Rate
- Power Supply
- Digital Interface
- Microcontroller

Note: This data is only provided as an example.
High-Bandwidth Design

Features:

• Highest throughput
  \[ 500\text{ksps} < f_{\text{throughput}} < 1\text{Msps} \]
• Widest input bandwidth \( (f_{\text{max}} = \frac{1}{2} \times f_{\text{throughput}}) \)
  \[ 250\text{kHz} < f_{\text{max}} < 500\text{kHz} \]
• Fastest transient response time \( (t_{\text{min}} = \frac{1}{f_{\text{max}}}) \)
  \[ 2\mu\text{s} < t_{\text{min}} < 4\mu\text{s} \]

Limitations:

• Requires a high-bandwidth amplifier
  – High-bandwidth = more power
  – High-bandwidth = more difficult to get good dc accuracy (i.e. low offset, drift)
  – May be more costly to get a good bandwidth and dc accuracy
  – Layout and parasitic are more critical than low bandwidth designs
Mid-Range Design

Features:

• Moderate throughput
  \[ 100 \text{ksp} < f_{\text{throughput}} < 500 \text{ksp} \]

• Reduced input bandwidth \( (f_{\text{max}} = \frac{1}{2} * f_{\text{throughput}}) \)
  \[ 50 \text{kHz} < f_{\text{max}} < 250 \text{kHz} \]

• Reduced transient response time \( (t_{\text{min}} = 1/f_{\text{max}}) \)
  \[ 4 \mu s < t_{\text{min}} < 20 \mu s \]

Limitations:

• Can use a lower-bandwidth amplifier
  – Lower-bandwidth = less power
  – Lower-bandwidth = many options with good dc accuracy (i.e. low offset, drift)
  – Less expensive to get a good bandwidth and dc accuracy
  – Easier to design than wide bandwidth: layout and parasitics less critical

Mid-Range

Optimized for balance between power and data rate

\(< 500 \text{ ksp} \)

1 mW
Low-Power Design

Features:

• Minimal throughput
  \[ f_{\text{throughput}} < 1 \text{ksps} \]
• Very low bandwidth \( (f_{\text{max}} = \frac{1}{2} \times f_{\text{throughput}}) \)
  \[ 250 \text{ Hz} < f_{\text{max}} < 500 \text{ Hz} \]
• Slow transient response time \( (t_{\text{min}} = \frac{1}{f_{\text{max}}}) \)
  \[ t_{\text{min}} < 3 \text{ms} \]

Limitations:

• Lower system performance when driver is removed
  – Lowest cost, board area, and power
  – Best performance with low sensor output impedance

Low-Power
Optimized for lowest power by eliminating the drive buffer

\[ < 1 \text{ksps} \]
\[ < 1 \mu\text{W} \]
Basic Data Acquisition System
Design Procedure

1. Select Sensor Type
   - Output frequency determines the sampling rate of the ADC
   - Output range needs to be scaled to match the input range of the ADC

```
+--------------------+       +--------------------+
|                   |       |                   |
| INPUT DRIVER       |       | SAR ADC            |
|                   |       | ADS7042            |
|                   |       | 3V                 |
|                   |       | 1V                 |
|                   |       | -1V                |
|                   |       | 0V                 |
|                   | Level-shifted, amplified, and/or attenuated |
```
Design Procedure

1. Select Sensor Type
2. Select Analog-to-Digital Converter
   - Power consumption scales with sampling rate

![Graph showing power consumption vs. sampling rate](chart.png)

- **ADS7042**
- **SAR ADC**
SAR ADC Optimized Power Consumption

**ADS7042 Typical Analog Power Consumption**

<table>
<thead>
<tr>
<th></th>
<th>1 MSPS</th>
<th>1 kSPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVDD = 3V</td>
<td>690 µWatts</td>
<td>690 nWatts</td>
</tr>
<tr>
<td>AVDD = 1.8V</td>
<td>234 µWatts</td>
<td>234 nWatts</td>
</tr>
</tbody>
</table>

To optimize the power consumption of a SAR ADC:
- Use the lowest permissible sampling rate/throughput
- Use the lowest permissible analog supply voltage
- Use the lowest permissible digital supply voltage
- Reduce the capacitance on each digital interface line
Ultra-Low Power ADC Core Technology
ADS704x Family

Industry’s First 12-bit SAR ADC with NanoWatt power consumption

- Typical Power: **234 nW @ 1 ksps**
- Power consumption scales directly with sampling rate
- 8 pin QFN package measuring only **1.5 x 1.5 mm**
- Can be mounted extremely close to or directly to sensors
- Multiple devices can be used to create a small multi-channel system

Optimize power consumption at the system-level

- Increase battery life and lifetime replacement
- Reduce battery size and cost

The ADS7042 can run for an estimated **6 days longer** at 1ksps off of a 1000mAh CR2477 3V Lithium battery when used in place of the internal ADC of MCU 1.

ADC Power @ 1 ksps

- **Typical Power:** 234 nW @ 1 ksps
- **Power consumption scales directly with sampling rate**
- **8 pin QFN package measuring only 1.5 x 1.5 mm**
- **Can be mounted extremely close to or directly to sensors**
- **Multiple devices can be used to create a small multi-channel system**
Selecting a Reference for the ADC

Most precision analog-to-digital converters require an external voltage reference:

- Large initial inrush current at the start of conversion and **large current transients** at bit conversions
- ADCs with **higher than 14-bit precision** require voltage reference + buffer
- REF6xxx devices are the first voltage references in the industry that **integrate the ADC drive buffer**
- TI Design TIPD173 walks through selecting the R and C for the reference pin
# Voltage Reference Options

<table>
<thead>
<tr>
<th>Voltage Reference Option</th>
<th>Use-cases / Limitations</th>
</tr>
</thead>
<tbody>
<tr>
<td>LDO as the reference</td>
<td>Least accurate</td>
</tr>
<tr>
<td>Reference as the LDO</td>
<td>More accurate, but limited by output current</td>
</tr>
<tr>
<td>LDO + Reference without buffer</td>
<td>10- and 12-bit ADCs</td>
</tr>
<tr>
<td>LDO + Reference with buffer</td>
<td>≥14-bit ADCs, but highest power</td>
</tr>
</tbody>
</table>

![Diagram](image)

**POWER SUPPLY**
- LDO / REF

**SENSORS**
- INPUT DRIVER
- FILTER
- SAR ADC
- ADS7042

*Texas Instruments*
Design Procedure

1. Select Sensor Type
2. Select Analog-to-Digital Converter
3. Select Amplifier
   - Bandwidth & slew rate for proper ADC settling, and sensor frequency range
   - Choose lowest bandwidth for best current
   - Set gain and level shift to maximize input voltage range for ADC
The power consumed by a SAR ADC during sampling (acquisition) phase is negligible compared to power consumed by ADC during conversion phase.
Acquisition Cycle

• S1 closed during acquisition cycle (200ns)
• $C_{sh}$, Sample-hold capacitor, must charge to $\frac{1}{2}$ LSB
• Charge bucket capacitor, $C_F$, provides transient current at start of acquisition ($V_{sh} = V_{SH0}$)
• Amplifier must drive $V_{sh}$ to $\frac{1}{2}$ LSB by end of $t_{aq}$

Sampling Rate = 1 Msps

$t_{throughput} = t_{acq} + t_{conv} = 1\mu s$
$t_{acq} = 200\text{ns}$
$t_{conv} = 800\text{ns}$
Selecting Charge Bucket Filter & Amplifier

- \( C_F >> C_{SH} \) forces \( C_{SH} \) close to \( V_{in} \) when \( S_1 \) closes
- \( R_F \) is required for stability
- Amplifier bandwidth set by acquisition time (charge \( C_{SH} \) to \( \frac{1}{2} \) LSB)
  - Wide bandwidth amplifier needed for short acquisition time (high \( I_Q \))
  - Lower bandwidth amplifier needed for longer acquisition time (low \( I_Q \))
  - For very long acquisition time, and low source \( Z \), amp not required

Sampling Rate = 1 Msps

- \( t_{throughput} = t_{acq} + t_{conv} = 1\mu s \)
- \( t_{acq} = 200\text{ns} \)
- \( t_{conv} = 800\text{ns} \)
If the input signal bandwidth is low enough a long ADC acquisition time is permissible a SAR ADC may not need an input amplifier/driver.
Design Procedure

1. Select Sensor Type
2. Select Analog-to-Digital Converter
3. Select Amplifier
4. Select Power Supply
   - Typically an LDO or low current output precision voltage reference
   - Needs good load regulation for proper settling between conversions
   - Should consume as little quiescent current as possible
   - External stability resistor will dissipate additional power

POWER SUPPLY

LDO
Design Procedure

1. Select Sensor Type
2. Select Analog-to-Digital Converter
3. Select Amplifier
4. Select Power Supply
Summary

• Common low-power system design challenges
  – Power Consumption
  – Size
  – Performance

• Reference design specifics
  – Trade-offs are optimized in TI Design TIPD168
  – R and C selection is highlighted in TI Design TIPD173

• Low-power signal chain devices
  – ADS7042: Industry’s First 12-bit SAR ADC with Nanowatt Power Consumption
  – REF3330: Low-power (5 uA) voltage reference available in a small package
  – OPA333: Low quiescent current (17 µA) operational amplifier for driving the ADS7042

• Link for more information
  
ti.com/precisionadc
# Hands-on Experiment

### Circuit Diagram

- **OPA316**
  - $I_{Q316} = 400\mu A$
  - $V_{in} = 3.3V$

- **RF68**

- **CF1.5n**

- **100k**

- **1u**

- **10k**

- **MSP430FR4133**
  - **AVdd**
  - **3.3V**

- **RF 68**

- **CF 1.5n**

- **RSH**

- **CSH**

- **15p**

- **Comp**

- **N-Bit Register**

- **ADS7042**

- **System Current Sense**

## Table: Sampling Rate vs Power Consumption

<table>
<thead>
<tr>
<th>Sampling Rate</th>
<th>ADC Power</th>
<th>REF Power</th>
<th>Combined Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 ksps</td>
<td>0.69 µW</td>
<td>12.87 µW</td>
<td>13.56 µW</td>
</tr>
<tr>
<td>63 ksps</td>
<td>44.85 µW</td>
<td>12.87 µW</td>
<td>57.72 µW</td>
</tr>
<tr>
<td>125 ksps</td>
<td>86.25 µW</td>
<td>12.87 µW</td>
<td>99.12 µW</td>
</tr>
</tbody>
</table>
S1 – Changes LCD from power to HEX data

S1 – Reduces ADC sampling rate (down to 1 ksp/s)

S2 – Increases ADC sampling rate (up to 125 ksp/s)