Power loss and thermal consideration in gate drivers

[Ritesh Oza]
What will I get out of this session?

• Purpose:
This presentation will discuss power losses, distribution of power losses, thermal impedance, and impact of various parameters on thermal performance of the gate drivers. Presentation will also show methodology and examples of thermal measurements in gate drivers.

• Part numbers mentioned:
  • UCC21520
  • UCC27714, UCC27712

• Reference designs mentioned:
  • TIDM-1000
  • PMP20873

• Relevant End Equipments:
  • Telecom Power Supplies
  • Automotive On Board Charger
  • Motor Drives, and more
General Classification of Gate Driver ICs

• A) Low Side Gate Driver - UCC27524, UCC27531
• B) High-Side Low-side Gate Driver or Half-Bridge Gate Driver – UCC27712, LM510x
• C) High Side Only Gate Driver
• D) Isolated Gate Driver – UCC21520
Where does power dissipate?
Estimating Power Loss in a Gate Driver IC

- **Static Power Loss**
  \[ P_{QC} = V_{DD} \times I_{DD} + (V_{DD} - V_{DH}) \times I_{HB} \]

- **Static Level Shifter Loss**
  \[ P_{IHBS} = V_{HB} \times I_{HBS} \times D \]

- **Dynamic Level Shifter Loss**
  \[ P_{LS} = V_{HB} \times Q_p \times f_{SW} \]

- **Switching Loss**
  \[ P_{QG1&2} = 2 \times V_{DD} \times Q_g \times f_{SW} \times \frac{R_{GD-R}}{R_{GD-R} + R_{Gate} + R_{GFET_int}} \]

- **Bootstrap Diode Loss**
  \[ P_{Diode} = V_f \times I_f \] + Reverse Recovery Losses
Influence of Lead-Frame/Substrate on Thermal Performance

- Identical Layout
- Purely Capacitive Load
- Supply Voltage and current monitored
- Switching frequency varied
- Case temperature measured using type K thermocouple at package top/center
Does Package Size Influence Thermal Performance

![Diagram showing two IC packages: SOIC-14 and SOIC-8, with labels UCC27714 and UCC27712.]
Does Package Size Influence Thermal Performance

**Thermal Performance of UCC27712, UCC27714**

**Est. Junction Temp. Increase vs. Power Dissipation**
Bootstrap Diode Peak Power Dissipation

- During start up, first few cycles high peak current flow through bootstrap diode
- Need to make sure that bond wire, die, and other metal layers can handle this peak current
Bootstrap Diode Peak Power Dissipation

- If bootstrap diode is reverse biased when high forward current is flowing, then the power dissipation in the bootstrap diode could be very high and could damage the diode.
What information one would need for IC Thermal Analysis?

- A) Maximum Allowed Junction Temperature
- B) IC Thermal Model
- C) IC Power Dissipation
- D) Operating Conditions
Thermal Model of a Gate Driver IC

- Based on JEDEC standards
- Many vendors do not provide all the thermal parameters
- Thermal performance comparison must be done on the same board and under the exact same operating conditions

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>UCC21520 DW-16 (SOIC)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JA}$</td>
<td>78.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JC(top)}$</td>
<td>11.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JB}$</td>
<td>48.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JT}$</td>
<td>12.5</td>
<td>°C/W</td>
</tr>
<tr>
<td>$\psi_{JB}$</td>
<td>48.4</td>
<td>°C/W</td>
</tr>
</tbody>
</table>
Comparing Thermal Performance of Two Parts

- Case temperature can be compared under the same operating conditions.
- But junction temperature cannot be estimated accurately or compared reliably without a full thermal model.

What is the test condition? And are they the same?
Thermal Performance Analysis

- TI’s Simplified Circuit

- Conservative estimate
- Capacitive load can be estimated based on $Q=CV$
- $Q$ can be lower for soft switching topologies
- Diode losses are ignored
Thermal Performance Analysis

• Estimating junction temperature is always possible when:
  - $\Psi_{JT}$ is provided on the datasheet ($T_J = \Psi_{JT} \times P_D + T_C$)
  - Application layout is available for testing
  - Case temperature can be measured
  - IC power dissipation is known

• Predicting thermal performance in three steps:
  1. Measure $T_C$ with known voltages/currents and purely capacitive load
  2. Calculate $T_J$ for the test cases with $\Psi_{JT}$
  3. Characterize $\Theta_{JA(Effective)}$ for application layout
  4. Use $\Theta_{JA(Effective)}$ to estimate junction temperature for any system configuration
Thermal Performance Analysis

**UCC21520 Case Temp. vs. Switching Frequency**

![Graph showing UCC21520 Case Temp. vs. Switching Frequency](image)

**Junction Temp vs. Power Dissipation**

![Graph showing Junction Temp vs. Power Dissipation](image)

\[ T_J = \Psi_{JT} \times P_D + T_C \]

Plot \( T_J \) vs. \( P_D \)

\[ \Theta_{JA(Effective)} = \frac{dT_J}{dP_D} = 45.8^\circ C/W \]

Characterization from UCC21520 vs Si8233

Compare this \( \Theta_{JA} \) with 78°C/W shown in thermal model. Why?
Thermal Performance Analysis

• Accuracy
  • When system parameters such as power MOSFET and gate resistor changes, one cannot directly compare junction temperature.
  • Need to estimate case temperature based on previously calculated $\Theta_{JA(Effective)}$
  • $\Theta_{JA(Effective)}$ more dependent on board layout and airflow through the board than absolute ambient temperature
  • Temperature coefficient of various resistances such as power MOSFET internal gate resistor, driver IC driver stage pull-up/pull-down resistor, and gate resistor is important for very accurate prediction/estimation
  • Equal thermal settling time should be allowed before taking thermal measurement
  • Proper thermocouple and it’s connection is necessary to achieve accurate results
Thermal Performance Analysis

Predicted vs. Measured Case Temperature

Junction Temp. vs. Switching Frequency

- Measured Case Temperature
- Predicted Case Temperature
- Changed Power MOSFET and Gate Resistor

- 5.10 + Diode, 22°C Ambient (Measured)
- 5.10 + Diode, 80°C Ambient (Prediction)
- 5.10 + Diode + 2Ω FET Internal Resistance, 80°C Ambient (Prediction)
Prominent Influencers and Best Practices

• Board Layout
  • More copper, cooler junction
  • Large pour on $V_{DDA}$, $V_{SSB}$ minimizes switch node size, maximizes thermal performance
• Soft switching reduces $Q_G$, power consumption
• Temperature coefficients
  • Driver on/off resistance can vary >10% over temperature
  • MOSFET internal gate resistance varies with MOSFET temperature
• Radiation (proportional to $T^4$, performance improves with temperature)
• MOSFET internal gate resistance, diode loss, and frequency-related capacitance changes tend to reduce driver IC internal power dissipation
• Can use $T_{C,Predicted} = \left(\Theta_{JA} - \Psi_{JT}\right)(P_{SW} + P_{STATIC}) + T_A$ to verify vs. measured $T_C$
Key Take Aways

• Lot of parameters influence thermal performance of the gate driver IC

• Complete thermal model is essential to do detailed thermal analysis and comparison

• Detailed functional block diagram and power dissipation distribution within IC need to be understood to evaluate thermal reliability of the part

• Estimating thermal performance based on thermal model could save lot of development time
Thank You

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