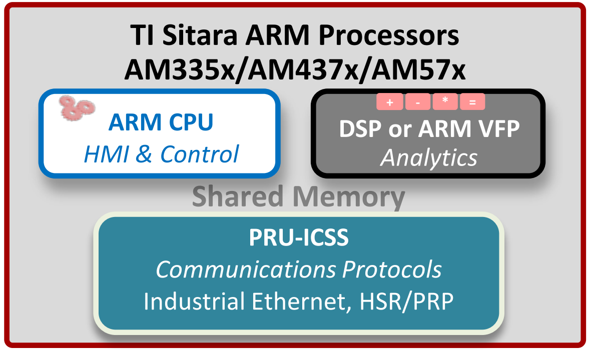
Sitara Processors Encoder Interfaces

PRU-ICSS: Programmable Real-Time Industrial Control and Communications Subsystem

TI Sitara Processors simplify development for industrial applications through the PRU-ICSS:

- **Deterministic RISC cores with dedicated I/O and memory**
- **Hard real-time performance, fully deterministic**
- **Assembly & C Programmability**



Benefits of the TI PRU-ICSS solution:

- Integrated solutions provide **BOM**, **power**, **size**, **cost** savings.

- Software-based:
  - Support for **multiple real-time protocols** with the same hardware
  - Able to support **customer specific** solution development

- **Scalable solutions** supporting commercial and industrial Ethernets, encoder interfaces, data acquisition, and more.

Protocols Supported

EnDat 2.2
- ISDK full source reference design

BiSS INTERFACE
- Full source reference design (AM437x)

HIPERFACE DSL

Position Feedback Solutions

SoC	AM335x • 1x A8, 1 GHz • GbE Switch, SGX • 16 bit DDR3 • 15x15mm ICSS_M	AM437x • 1x A9, 1 GHz • GbE Switch, SGX • 32 bit DDR3, QSPI • 17x17mm ICSS_M+L	AM57x • 1x/2x A15, 1.5 GHz • 1x C66x, 750 MHz • 32 bit DDR3, QSPI, PCIe, USB3 • 23x23mm 2 x ICSS_M
PRUs	**2**	**4**	**4**
EnDAT2.2	**-**	**3 ch / PRU**	**3 ch / PRU**
Hiperface DSL	**-**	**1 ch / PRU**	**1 ch / PRU**
BiSS	**-**	**1 ch / PRU**	**1 ch / PRU**
Custom	**Yes**	**Yes**	**Yes**
Industrial Ethernet	1 protocol with two phy ports	1 protocol with two phy ports	2 protocols
Profibus DP	1	2	2

TIDEP0050 & TIDA-00172
EnDat 2.2 System Reference Design

TIDesigns

EnDat 2.2

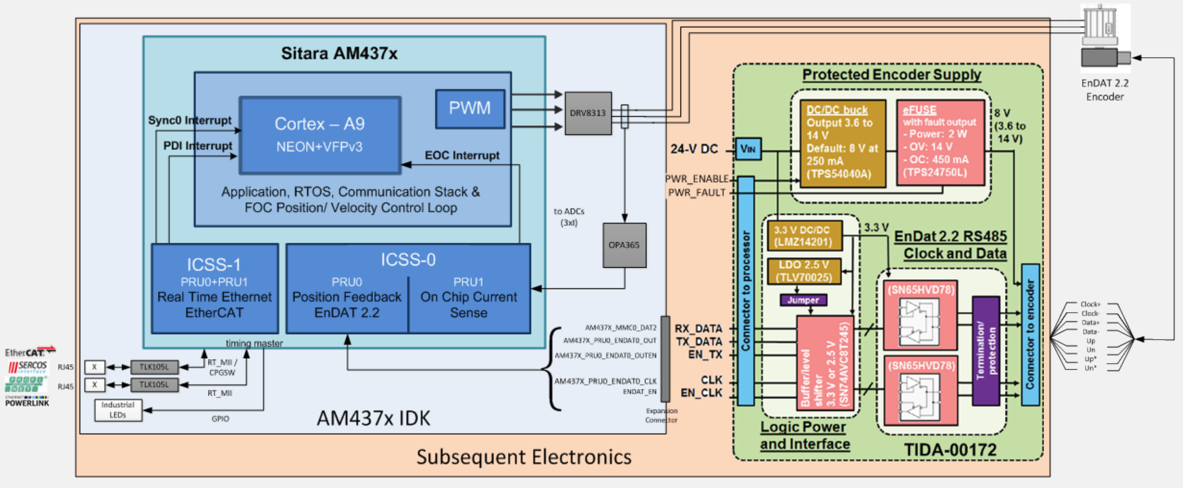
Solution Features

- EnDAT 2.2 Master protocol running on ICSS
- Interface speed of 300 KHz – 8/16 MHz
- 8x oversampled input capture
- Line delay compensation with filtered sample point
- Command interface
- Supports up to 100 m cable (150 m at lower speed)
- Runs on AM437x with ICSS
- Examples and Sources in ISDK

Solution Benefits

- Integrated with scalable ARM MPU devices
- Firmware implementation with maximum flexibility for customization
- Full performance with at 8/16 MHz
- Low power consumption on 40nm low power process technology

Tools & Resources



Cable Length	Frequency
Up to 20m	16MHz
Up to 100m	8MHz
Up to 150m	300KHz

TIDEP0022

ARM MPU with Integrated BiSS C Master Interface

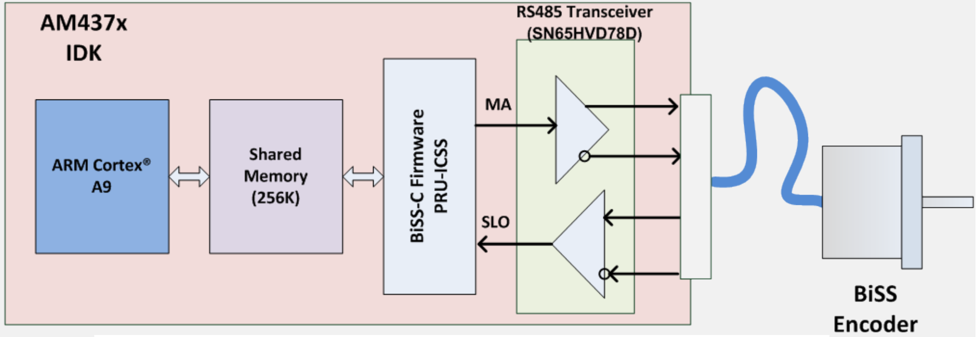
Solution Features

- BiSS C Master protocol running on ICSS
- Interface speed of 1, 2, 5 and 10 MHz
- 8x oversampled input capture
- Line delay compensation with filtered sample point
- Debouncing filter on oversampled input
- Variable frame format with CRC check
- Command (CDS/CDM) interface
- Supports up to 100 m cable
- Runs on AM437x with ICSS

Solution Benefits

- Integrated with scalable ARM MPU devices
- Firmware implementation with maximum flexibility for customization
- Full performance with 8x oversampling at 10 MHz
- Low power consumption on 40nm low power process technology
- Maximum reach with up to 100 meter cable length
- Auto adjust of data rate according to line delay measurement

Tools & Resources



Cable Length	Frequency
Up to 10m	10MHz
Up to 25m	5MHz
Up to 60m	2MHz
Up to 100m	1MHz

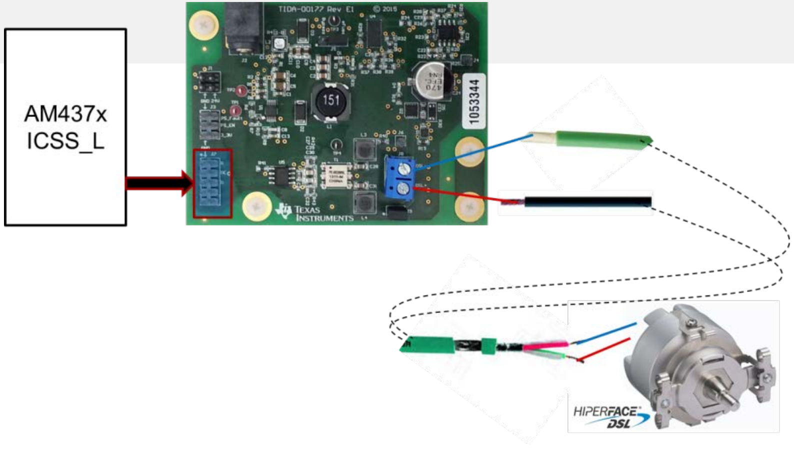
TIDEP0035 + TIDA-00177
Hiperface DSL Master Protocol on AM437x IDK

Solution Features

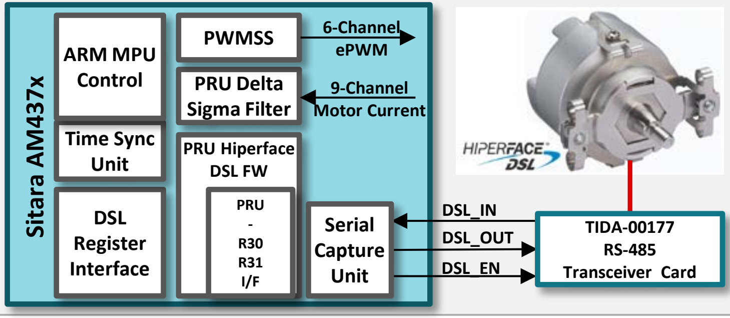
- HIPERFACE DSL master protocol with register compatible interface to existing FPGA IP core
- Design is able to be combined with a Delta Sigma filter and Industrial Ethernet (Single Chip Drive)
- Support for internal and external sync pulse sources
- Supports cable length of up to 100 meter
- Line delay compensation
- 8x oversampling with sample edge detection
- Line diagnostics – quality monitor

Solution Benefits

- Hiperface DSL allows to remove motor feedback cable
- Integrated with Single Chip Drive solution
- Replaces external FPGA
- On-chip time synchronization with motor application
- 225 MHz design supports minimum-sync pulse jitter



Tools & Resources



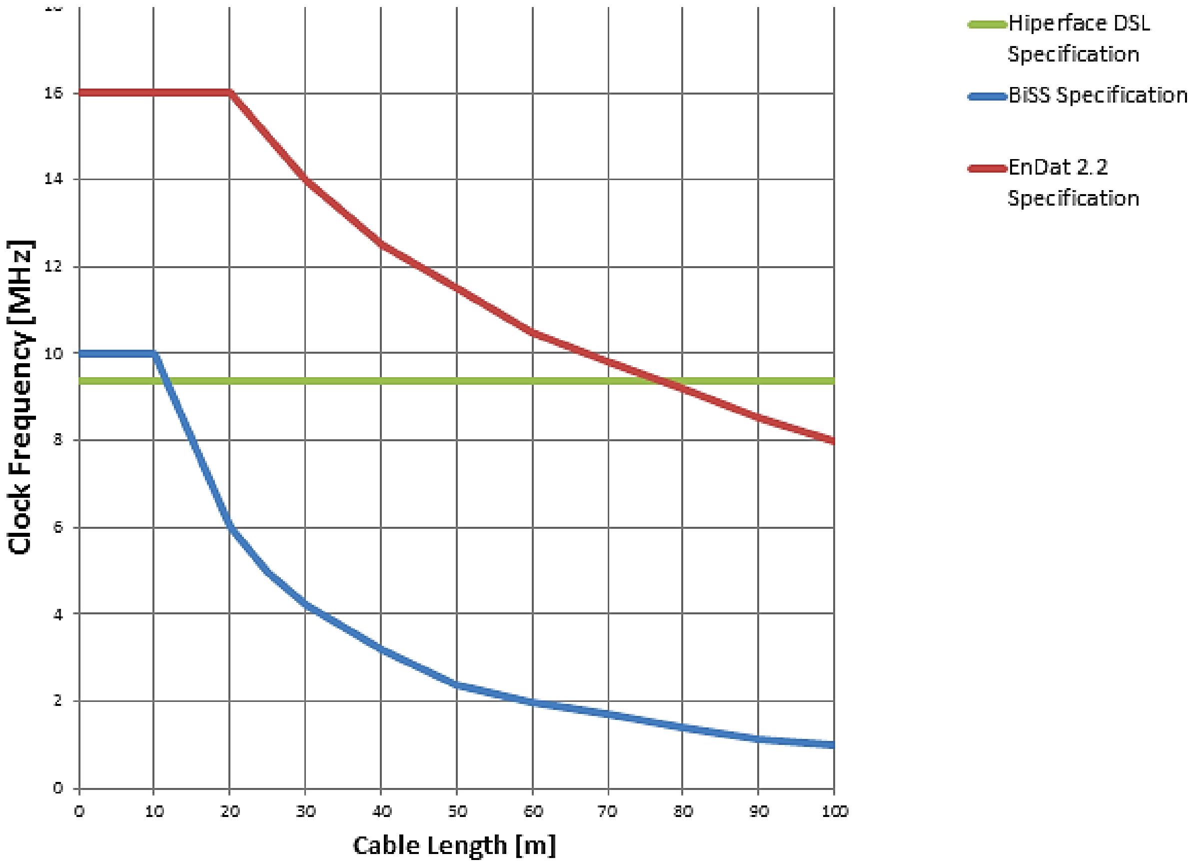
Encoder Technology

Sitara Processors Encoder Interfaces

Digital Encoder Interfaces

Protocol	EnDAT 2.2	Hiperface DSL	BiSS C
Owner	Heidenhain (Germany)	Sick (Germany)	iC Haus (Germany)
License /specification	Free / NDA	Free / NDA	Free / Open Source
Phy Interface	RS-485	RS-485	RS-422/485
Speed	100kbit - 8/16 Mbit	9.375 Mbit	1/2/5/10 Mbit
Reach	100 meter, 150m at lower speed	100 meter	100 meter
Cable	4 wire	2 wire, motor integrated	4 wire
Max frame length	~ 31+116 bit	continuous frame 117 bit	64 bit / frame
Delay compensation	yes	yes	yes
Oversampling	8x	8x	8x
Overhead channels	Two additional	8 V frames	1 bit per frame
Synchronization	Start pulse – bit time	Async Pulse (13 ns)	Start pulse – bit time
Host interface	Own API function compatible	register compatible	register compatible
Functional Safety	Yes	No	Yes
Sitara - ICSS	ICSS_L / M_v2 1-3 chan per PRU	ICSS_L / M_v2, (225MHz),1 chan per PRU	ICSS v1 1 channel per PRU

Encoder Cable Length vs Speed



For More Information

- Sitara™ Processors

- Industrial Communications Overview

- TI Designs:
  - TIDEP0050: EnDat 2.2 System Reference Design
  - TIDA-00172: Reference Design for an Interface to a Position Encoder with EnDat 2.2
  - TIDEP0022: ARM MPU with Integrated BiSS C Master Interface Reference Design
  - TIDEP0035: ARM MPU with Integrated HIPERFACE DSL Master Interface Reference Design
  - TIDA-00177: Two-Wire Interface to a HIPERFACE DSL Encoder Reference Design

- For questions regarding topics covered in this training, visit the support forums at the TI E2E Community website: http://e2e.ti.com