Sitara Processors Encoder Interfaces
PRU-ICSS: Programmable Real-Time Industrial Control and Communications Subsystem

TI Sitara Processors simplify development for industrial applications through the PRU-ICSS:

- Deterministic RISC cores with dedicated I/O and memory
- Hard real-time performance, fully deterministic
- Assembly & C Programmability

Benefits of the TI PRU-ICSS solution:

- Integrated solutions provide BOM, power, size, cost savings.
- Software-based:
  - Support for multiple real-time protocols with the same hardware
  - Able to support customer specific solution development
- Scalable solutions supporting commercial and industrial Ethernets, encoder interfaces, data acquisition, and more.

Protocols Supported:

- EnDat 2.2
- BiSS Interface
- HiPERFACE DSL
- ISDK full source reference design
- Full source reference design (AM437x)
# Position Feedback Solutions

## SoC

<table>
<thead>
<tr>
<th>PRUs</th>
<th>AM335x</th>
<th>AM437x</th>
<th>AM57x</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1x A8, 1 GHz</td>
<td>1x A9, 1 GHz</td>
<td>1x/2x A15, 1.5 GHz</td>
</tr>
<tr>
<td></td>
<td>GbE Switch, SGX</td>
<td>GbE Switch, SGX</td>
<td>1x C66x, 750 MHz</td>
</tr>
<tr>
<td></td>
<td>16 bit DDR3</td>
<td>32 bit DDR3, QSPI</td>
<td>32 bit DDR3, QSPI, PCIe, USB3</td>
</tr>
<tr>
<td></td>
<td>15x15mm</td>
<td>17x17mm</td>
<td>23x23mm</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PRUs</th>
<th>2</th>
<th>4</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>EnDAT2.2</td>
<td>-</td>
<td>3 ch / PRU</td>
<td>3 ch / PRU</td>
</tr>
<tr>
<td>Hiperface DSL</td>
<td>-</td>
<td>1 ch / PRU</td>
<td>1 ch / PRU</td>
</tr>
<tr>
<td>BiSS</td>
<td>-</td>
<td>1 ch / PRU</td>
<td>1 ch / PRU</td>
</tr>
<tr>
<td>Custom</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Industrial Ethernet</td>
<td>1 protocol with two phy ports</td>
<td>1 protocol with two phy ports</td>
<td>2 protocols</td>
</tr>
<tr>
<td>Profibus DP</td>
<td>1</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>
EnDat 2.2 System Reference Design

Solution Features
- EnDat 2.2 Master protocol running on ICSS
- Interface speed of 300 KHz – 8/16 MHz
- 8x oversampled input capture
- Line delay compensation with filtered sample point
- Command interface
- Supports up to 100 m cable (150 m at lower speed)
- Runs on AM437x with ICSS
- Examples and Sources in ISDK

Solution Benefits
- Integrated with scalable ARM MPU devices
- Firmware implementation with maximum flexibility for customization
- Full performance with at 8/16 MHz
- Low power consumption on 40nm low power process technology

Tools & Resources
- Examples and Sources in ISDK

Cable Length | Frequency
--- | ---
Up to 20m | 16MHz
Up to 100m | 8MHz
Up to 150m | 300KHz
TIDEP0022
ARM MPU with Integrated BiSS C Master Interface

Solution Features
- BiSS C Master protocol running on ICSS
- Interface speed of 1, 2, 5 and 10 MHz
- 8x oversampled input capture
- Line delay compensation with filtered sample point
- Debouncing filter on oversampled input
- Variable frame format with CRC check
- Command (CDS/CDM) interface
- Supports up to 100 m cable
- Runs on AM437x with ICSS

Solution Benefits
- Integrated with scalable ARM MPU devices
- Firmware implementation with maximum flexibility for customization
- Full performance with 8x oversampling at 10 MHz
- Low power consumption on 40nm low power process technology
- Maximum reach with up to 100 meter cable length
- Auto adjust of data rate according to line delay measurement

Tools & Resources

Cable Length | Frequency
---|---
Up to 10m | 10MHz
Up to 25m | 5MHz
Up to 60m | 2MHz
Up to 100m | 1MHz
Solution Features

- HIPERFACE DSL master protocol with register compatible interface to existing FPGA IP core
- Design is able to be combined with a Delta Sigma filter and Industrial Ethernet (Single Chip Drive)
- Support for internal and external sync pulse sources
- Supports cable length of up to 100 meter
- Line delay compensation
- 8x oversampling with sample edge detection
- Line diagnostics – quality monitor

Solution Benefits

- Hiperface DSL allows to remove motor feedback cable
- Integrated with Single Chip Drive solution
- Replaces external FPGA
- On-chip time synchronization with motor application
- 225 MHz design supports minimum-sync pulse jitter
Encoder Technology

Sitara Processors Encoder Interfaces
# Digital Encoder Interfaces

<table>
<thead>
<tr>
<th>Protocol</th>
<th>EnDAT 2.2</th>
<th>Hiperface DSL</th>
<th>BiSS C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Owner</td>
<td>Heidenhain (Germany)</td>
<td>Sick (Germany)</td>
<td>iC Haus (Germany)</td>
</tr>
<tr>
<td>License /specification</td>
<td>Free / NDA</td>
<td>Free / NDA</td>
<td>Free / Open Source</td>
</tr>
<tr>
<td>Phy Interface</td>
<td>RS-485</td>
<td>RS-485</td>
<td>RS-422/485</td>
</tr>
<tr>
<td>Speed</td>
<td>100kbit - 8/16 Mbit</td>
<td>9.375 Mbit</td>
<td>1/2/5/10 Mbit</td>
</tr>
<tr>
<td>Reach</td>
<td>100 meter, 150m at lower speed</td>
<td>100 meter</td>
<td>100 meter</td>
</tr>
<tr>
<td>Cable</td>
<td>4 wire</td>
<td>2 wire, motor integrated</td>
<td>4 wire</td>
</tr>
<tr>
<td>Max frame length</td>
<td>~ 31+116 bit</td>
<td>continuous frame 117 bit</td>
<td>64 bit / frame</td>
</tr>
<tr>
<td>Delay compensation</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Oversampling</td>
<td>8x</td>
<td>8x</td>
<td>8x</td>
</tr>
<tr>
<td>Overhead channels</td>
<td>Two additional</td>
<td>8 V frames</td>
<td>1 bit per frame</td>
</tr>
<tr>
<td>Synchronization</td>
<td>Start pulse – bit time</td>
<td>Async Pulse (13 ns)</td>
<td>Start pulse – bit time</td>
</tr>
<tr>
<td>Host interface</td>
<td>Own API function compatible</td>
<td>register compatible</td>
<td>register compatible</td>
</tr>
<tr>
<td>Functional Safety</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Sitara - ICSS</td>
<td>ICSS_L / M_v2 1-3 chan per PRU</td>
<td>ICSS_L / M_v2, (225MHz),1 chan per PRU</td>
<td>ICSS v1 1 channel per PRU</td>
</tr>
</tbody>
</table>
For More Information

- **Sitara™ Processors**

- **Industrial Communications Overview**

- **TI Designs:**
  - [TIDEPO050](#): EnDat 2.2 System Reference Design
  - [TIDA-00172](#): Reference Design for an Interface to a Position Encoder with EnDat 2.2
  - [TIDEPO022](#): ARM MPU with Integrated BiSS C Master Interface Reference Design
  - [TIDEPO035](#): ARM MPU with Integrated HIPERFACE DSL Master Interface Reference Design
  - [TIDA-00177](#): Two-Wire Interface to a HIPERFACE DSL Encoder Reference Design

- For questions regarding topics covered in this training, visit the support forums at the [TI E2E Community](http://e2e.ti.com) website: [http://e2e.ti.com](http://e2e.ti.com)