Texas Instruments

TI Solutions for Clock & Timing
Pushing the boundaries on your clock & timing designs

Dean Banerjee
Systems Engineer // Clock & Timing Solutions

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Most Popular Clock & Timing Links:

- Best PLL for your solution
- PLL performance, simulation & design
- RF PLLs & synthesizers: support & training
TI offers the complete high-speed signal chain

PLL / Synthesizer

Clock Distribution

ADC

Temp Sense

SYSREF

DEVCLK

FPGA

SYSREF

DEVCLK

DSP+ARM Processor

DDR

DAC

Temp Sense

Optional DDC

JESD204B Link

DAC

Optional DUC

JESD204B Link

Temp Sense

DAC

DDR Term

Memory Power

Low Noise LDOs

Integrated Switcher + LDO

FPGA/Processor Power

High Power Density Modules

Signal Chain Power

FPGA

Temp Sense

Low Noise LDOs

Integrated Switcher + LDO

FPGA/Processor Power

High Power Density Modules

Texas Instruments
Wideband, high performance synthesizers

**Highest performance**

Industry’s best PLL

+ 

1st 15GHz wideband integrated VCO

**Unique Features**

Phase align multiple devices

Generate frequency ramps

Clock for High speed Data converters
LMX2594/5 wideband synthesizer overview

**High Performance**
- High Frequency up to 19 GHz
- Low Jitter < 50 fs (100 Hz -100 MHz)

**Leading Edge Features**
- Phase Synchronization
- SysRef
- Fast Calibration Time
- Ramping

**Product Offering**
- Tools
- Recently Released Products
LMX2594/95 wideband synthesizer

- Industry’s best PLL Figure of Merit for Noise: -236 dBC/Hz
- Highest PFD frequency for a fractional mode: 300 MHz
- 45 fsec integrated jitter (100 Hz to 100 MHz) at 8.8 GHz
- Output up to 15 GHz directly from VCO
- LMX2595 Adds a doubler to reach frequencies from 15-19 GHz

Download datasheet, click here
LMX2594/5 wideband synthesizer overview

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Product Offering
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Align phase across multiple devices
Phase adjustment

• Phase Adjustment is done using the fractional engine and can be done with a fraction of zero.
  
  \[ \text{Phase shift} = \frac{1}{F_{pd}} \times \frac{\text{MASH SEED}}{F_{den}} \times \frac{1}{\text{channel divider}} \]

• Phase Adjustment can be made very fine resolution
  
  – For 100 MHz Phase detector, it can be made as small as \( \frac{1}{100 \text{ MHz}} \times \frac{1}{2^{32}-1} = 0.002 \text{ ps} \)

• Phase Adjust is available in the following devices
  
  – LMX2582/92 (but no phase sync), LMX2594/95, LMX2572
Phase synchronization reference diagram
TIDA-01410
LMX2594 multiple PLL reference design
TIDA-01346

View reference design, click here
~25 fs jitter with combination of four LMX2594/95

100 MHz

~25 fs Jitter
(100Hz – 100 MHz)
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JESD204B SYSREF support

- RFoutA can go up to 19 GHz
- RFoutB can be reconfigured as SYSREF
  - Max output frequency 85MHz
  - Fine delay adjustment available (<9 ps)
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Fast calibration time

- Some devices allow the user to speed up the VCO calibration by giving it an initial starting point.
Frequency ramping with integrated VCOs

- LMX2594 is the first device in industry to include frequency ramping with internal VCOs
- Also supported in LMX2595 and LMX2572
- Ramping can be automatic (2 segments can be stored) or manual
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Tools

**TICSPro**
- Programs RF EVMs
- Easy to Use
- Can also be used to validate registers

**PLLatinum Sim**
- Easy loop filter design
- Detailed simulation for spurs, lock time, phase noise, bode plot
PLLatinum Sim matches measured data well

- PLL Phase Noise trace shows sources that contribute to the phase noise
- Comparison trace is the actual measured data

- VCO Calibration Simulation shows switching through VCO Cores
- Comparison Trace is the actual measured data
Key resources

SOFTWARE TOOLS:
• PLLatinum Sim Design/Simulation Tool
• TICSPro Device Programming Tool

TI DESIGNS:
• TIDA-01410 Phase Synchronization Reference Design
• TIDA-0121 Multi-Channel JESD204B 15 GHz Clocking Reference Design
• TIDA-00626 9.8GHz RF CW Signal Generator Using Integrated Synthesizer With Spur Reduction Reference Design
• TIDA-00885 6 9.8GHz RF CW Signal Generator Using Integrated Synthesizer With Spur Reduction Reference Design

REFERENCES:
• PLL Performance, Simulation, and Design Book
• JESD204B Multi-Device Synchronization: Breaking Down the Requirements
• Clocking Optimization for RF Sampling Analog-to-Digital Converters
• High-frequency synchronization with multiple devices

NEW DEVICES:
• LMX2594 Datasheet AND EVM
• LMX2595 Datasheet AND EVM
• LMX2572 Datasheet AND EVM
• LMK04832 Product Page AND EVM
LMX2594/5 wideband synthesizer overview

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Product Offering
- Tools
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LMX2572 low power/high performance synthesizer
13MHz – 6.4GHz RF

Features

- Generates any frequency from 13MHz to 6.4GHz
- Excellent Phase noise and spurious performance
  - -127 dBc/Hz at 1MHz offset @ 6.4GHz carrier frequency open loop VCO performance
  - Normalized noise floor of -231dBc/Hz
  - 1/f better than -124 dBc/Hz
  - Spurious better than – 75 dBc/Hz
- Low current consumption 75 mA
- Novel scheme to remove Integer Boundary Spurs (IBS)
- Ability to synchronize output phase across multiple PLLs
- FSK modulation
- Fast calibration time (< 25 us)
- JESD204B support
- Frequency ramping support
- 2 differential outputs
- Pin/Software compatible with LMX2594

Benefits

- Lowest power solution for high performance PLL applications.
- Pin compatibility with LMX2592 and LMX2594 allows flexibility to re-use same board across applications that require different power, performance trade-offs.
- Provide high performance, low power clock source for high speed Data Converters

Download datasheet, click here
LMX2572 comparison with ADF4351

LMX2572 has 40% less power consumption than ADF4351
Oscillator family key highlights

- Available in standard footprint 7x5 and 5x3.2
- Short lead times for custom frequencies
- LMK61K2-322M26 and LMK62K2-156M25 being qualified with Intel
- Programmable LMK61E0 supported by Broadcom firmware
- Total stability of 25 and 50 ppm
**LMK04832: JESD204B Clock Cleaner**

Industry’s Highest Performance & Most Feature-Rich Clock Source

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### Features

- Supports 7 JESD204B targets (7 device clocks & 7 SYSREF) or 14 clocking targets conventional systems!
- Dual Loop PLLatinum PLL Architecture
- <50 fs RMS jitter at 245.76 MHz, 12 kHz to 20 MHz
- Noise Floor -155 dBC/Hz @ 3200 MHz
- 2 Integrated VCO to support 2 different freq
  - VCO0 = 2495 to 2705 MHz
  - VCO1 = 2945 to 3205 MHz
- Extended ambient temperature: -40 C to +85 C
- SYSREF analog delay 25 ps step resolution
- Dual/Single Loop with 0-delay
- JESD204B distribution / generation mode
- 300 MHz PLL2 phase detector frequency
- CML Swing: 1.4 Vpp differential @ 3.2 GHz
- Holdover mode when input clock is lost
- Package 9 mm x 9 mm QFN-64
- Pin to pin compatible with LMK0482x

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### Applications

- Low Jitter with JEDEC JESD204B
- JESD204B and Traditional Clocking Systems
- Military, Aerospace, radar systems
- Medical, Test and Measurement

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**Download datasheet, click here**
LMK04832 Jitter is <50 fs

RMS Jitter: 46.393 fs
Clock & Timing Design Support on E2E.com

TI E2E™ Community

Ask questions, share knowledge, solve problems with fellow engineers. Get in conversation today >>>