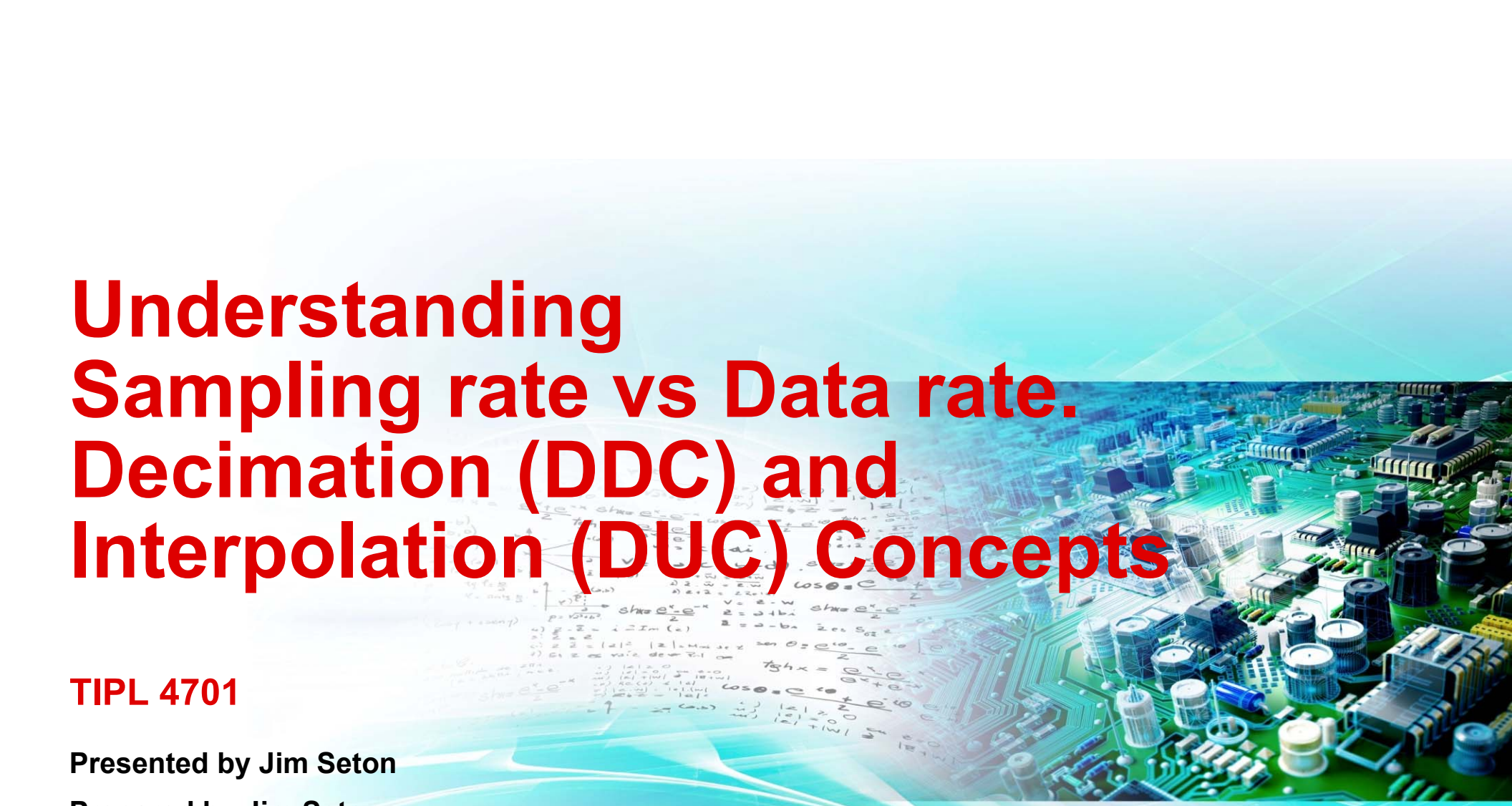
Understanding Sampling rate vs Data rate. Decimation (DDC) and Interpolation (DUC) Concepts



TIPL 4701

Presented by Jim Seton

Prepared by Jim Seton

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Sample Rate vs Data Rate

- Sampling rate (Fs) is the speed at which the data converter (ADC) is sampling an analog input or sending out (DAC) an analog output
- Data rate is the rate of the digital output data from an ADC or digital input data rate to a DAC
- In many cases, these are **NOT** the same rate.
- For instance, ADS54J60
  - 16 bit, dual ADC with sample rate = 1Gsps
  - Decimate by 2 mode, data output rate = sample rate / 2 = 500Msps
  - Decimate by 4 mode, data output rate = sample rate / 4 = 250Msps

Input Data Rates

- Higher sampling rates are required for sampling at RF and for frequency planning around spurious areas
- Data rates can not operate at those speeds
  - Limited by processor or FPGA rate
  - Limited by available I/O on the device
- Implement
  - Interpolation/Decimation in order to keep data rates reasonable
- Rule of thumb:
  - Select data rate to support bandwidth of the signal
  - Select sampling rate to support spectral purity

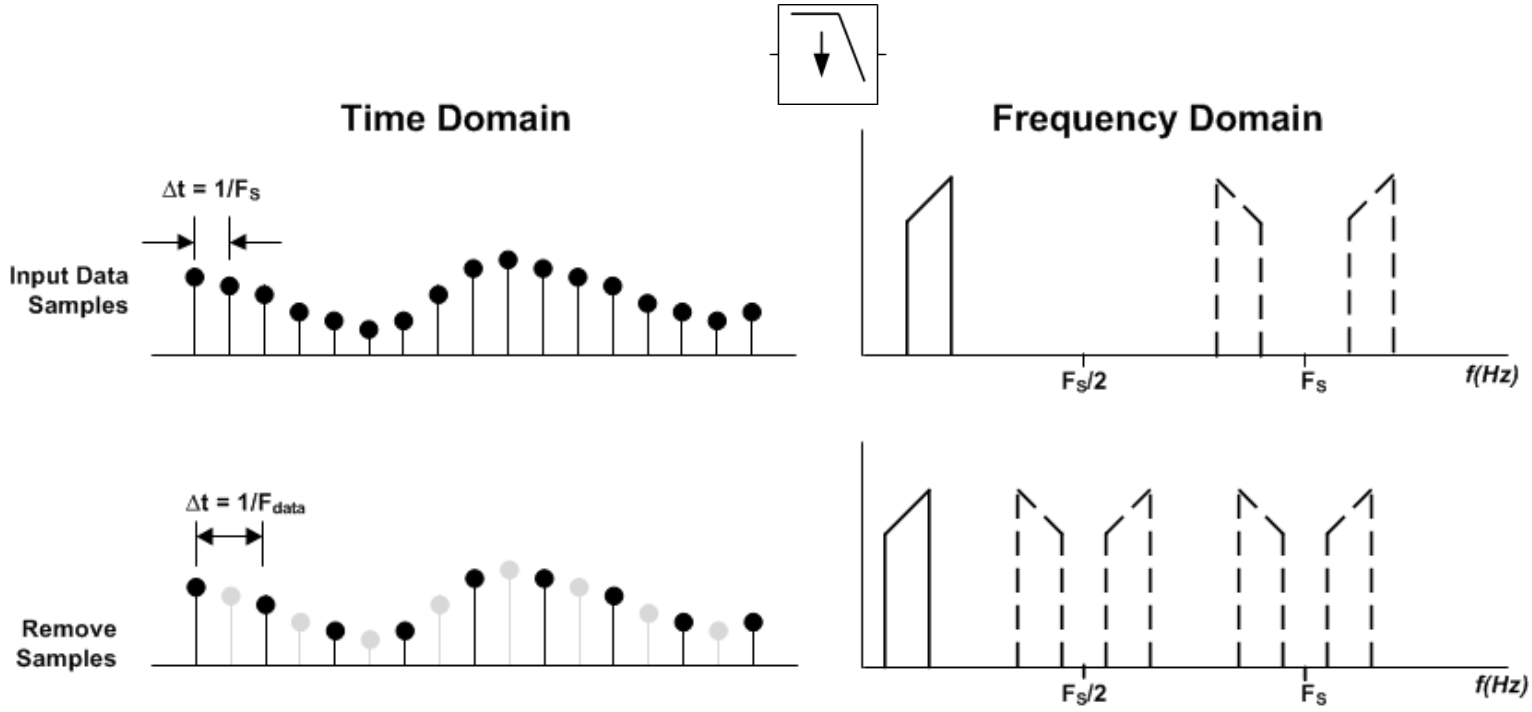
DECIMATION CONCEPTS

What is Decimation?

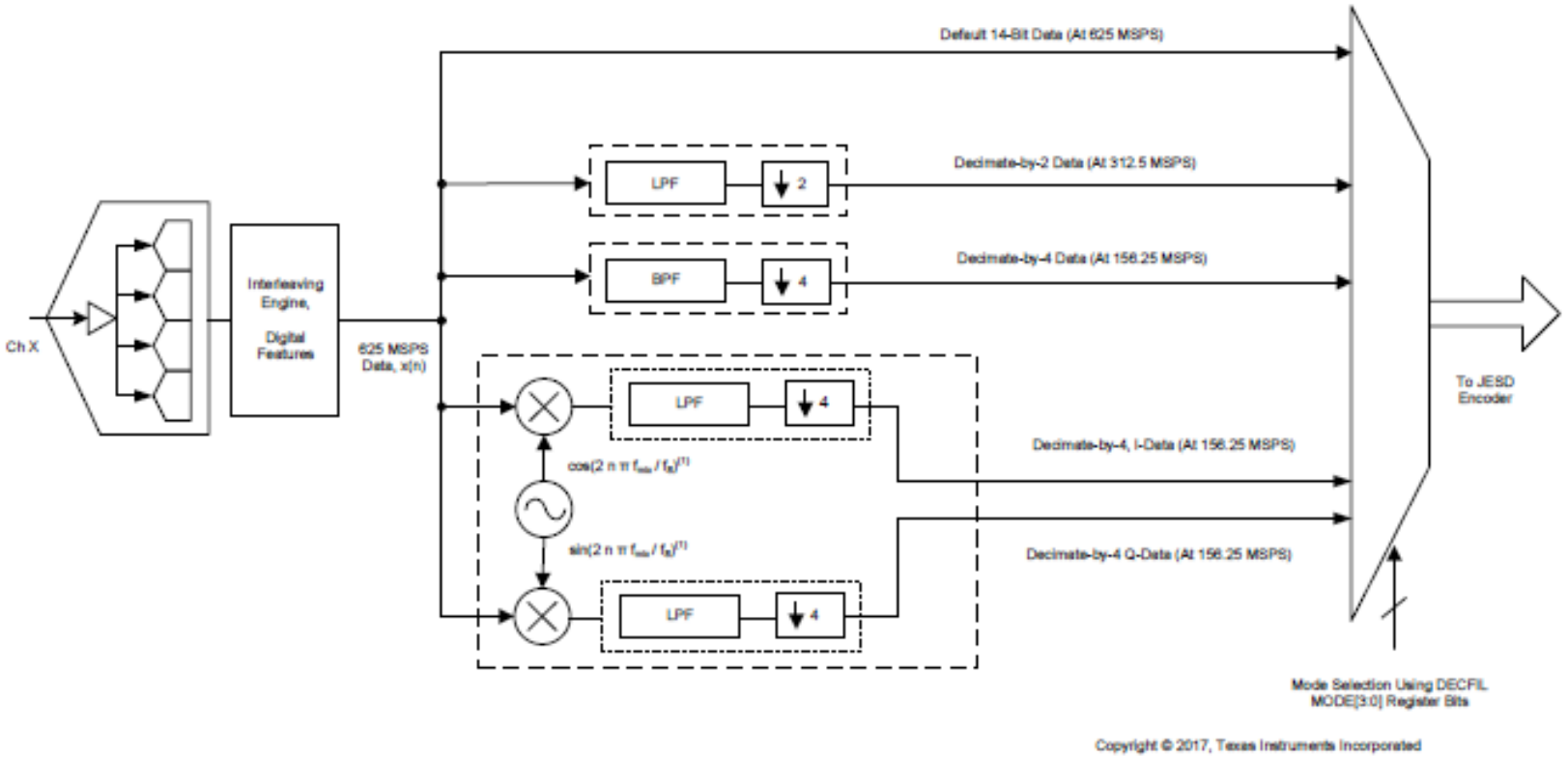
- Decimation decreases the sample rate of a signal by removing samples from the data stream
- Decimation includes digital low pass (anti-aliasing) filter followed by a decimator
  - The operation is equivalent to utilizing an analog anti-aliasing filter at fc = F_S /2M and sampling a converter at F_d = F_S /M, where M = decimation count (i.e. 2)
- Decimation is used to:
  1. Decrease the ADC data rate to reasonable levels for data capture
  2. Maintain high output sampling rate for more flexible frequency planning
  3. Take advantage of decimation filtering for improved spectral performance

Time/Freq Domain View of Decimation

- Images created with each decimation
- Low Pass filter provides anti-aliasing protection
- Data rate reduced for easier processing



Typical DDC Block Diagram (ADS54J60 Data Sheet)



(1) In IQ decimate-by-4 mode, the mixer frequency is fixed at $f_{mix} = f_S / 4$. For f_S = 1 GSPS and f_{mix} = 250 MHz.

Figure 60. DDC Block

Advantages and Disadvantages

Key Decimation Advantage

- Decimation provides SNR processing gain
- Frequency Domain View Signal remains constant
- Noise power is reduced by decimation filter
- Improved SNR performance
- Time Domain View Form over averaging samples to reduce overall noise

Decimation “Penalty”

- Increased digital power consumption
- More digital logic required
- Reduced signal bandwidth capability

ADC's with DDC

- **ADC32RF45/80 Family**
  - ADC32RF45 Dual-channel, 14-bit, 3GSPS Supports DDC (decimation /4 to /32) modes and bypass DDC mode.
  - ADC32RF80 Dual-channel, 14-bit, 3 GSPS Supports only DDC modes (decimation /4 to /32)
- **ADC12J4000/2700/1600 Family**
  - Single-channel 12-bit, 1.6 / 2.7 / 4GSPS, support DDC (decimation /4 to /32)
- **ADS54J20/40/42/60/69 Family**
  - Dual-channel 16,14,12-bit, 625MHz / 1GSPS, support DDC (decimation /2 and /4)

INTEROLATION CONCEPTS

Interpolation increases the sample rate of a signal without affecting the signal itself

The steps for 2x interpolation are as follows:

1. Insert a 0 between each sample (zero stuffing / up sampling)
2. Filter the resulting images from the up sample process
3. Repeat another 2x interpolation to get 4x, and again for 8x

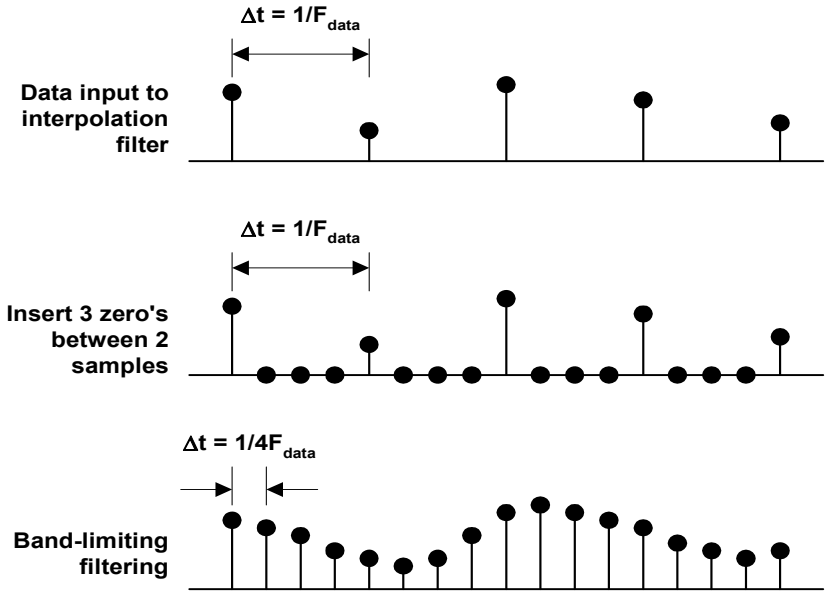
Cascading multiple 2x stages to increase interpolation is best due to efficient half-band filters.

Interpolation is used to:

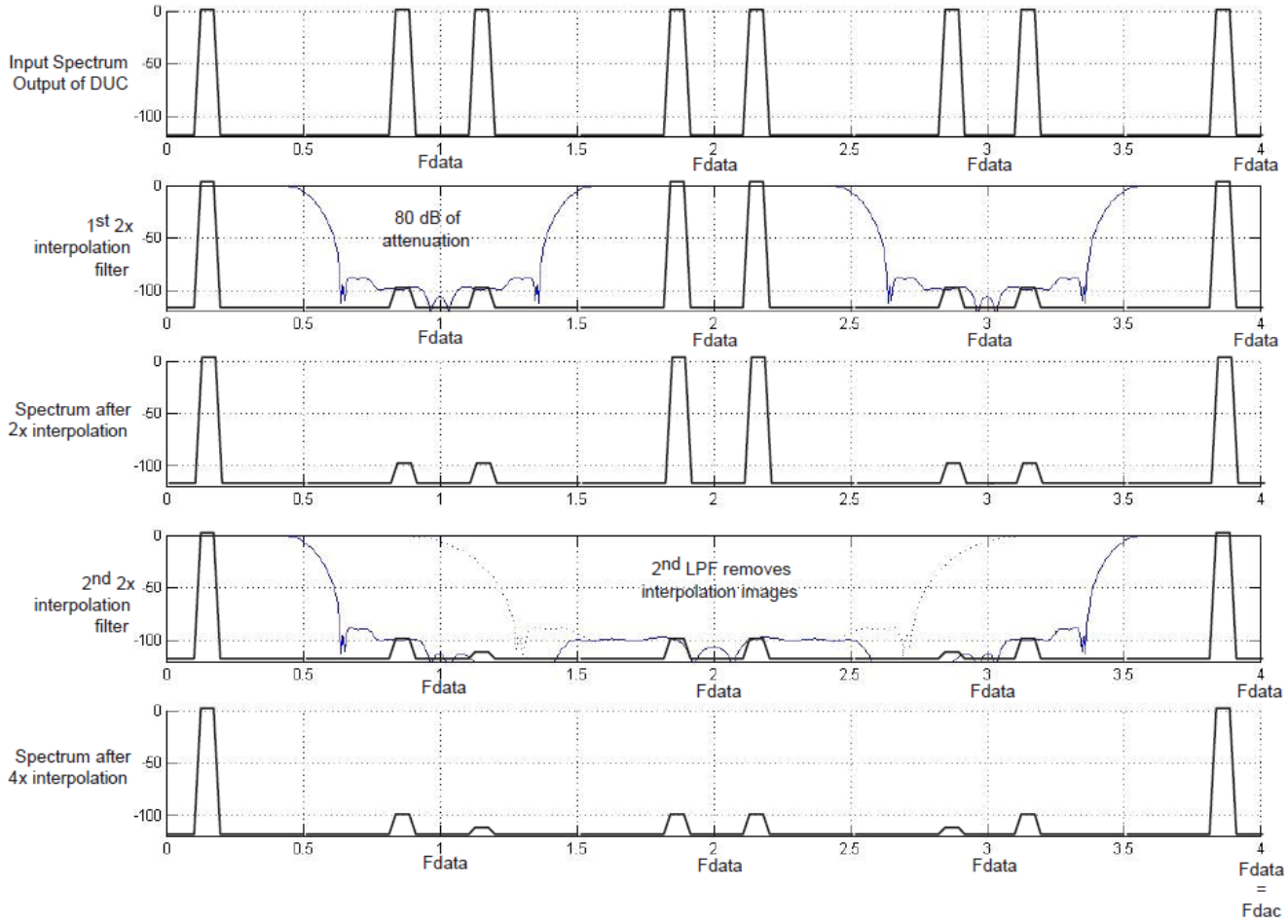
1. Increase the DAC output rate to allow for higher DAC output frequencies
2. Shift the DAC images further from the desired band of interest
3. Allow for a wider Nyquist zone for more flexible frequency planning
4. Maintain reasonable input data rates

Time Domain View of Interpolation

- 0's are inserted between the original samples
  - Adding a 0 does not change the spectral content, just sampling frequency
  - Widens the unique BW of the signal
- Low-pass (band-limiting) filtering fills in the missing levels between the original samples



Frequency Domain View of Interpolation



Typical DUC Filter response (DAC38J84 Data Sheet)

The filter taps for all digital filters are listed in Table 14. Note that the loss of signal amplitude may result in lower SNR due to decrease in signal amplitude.

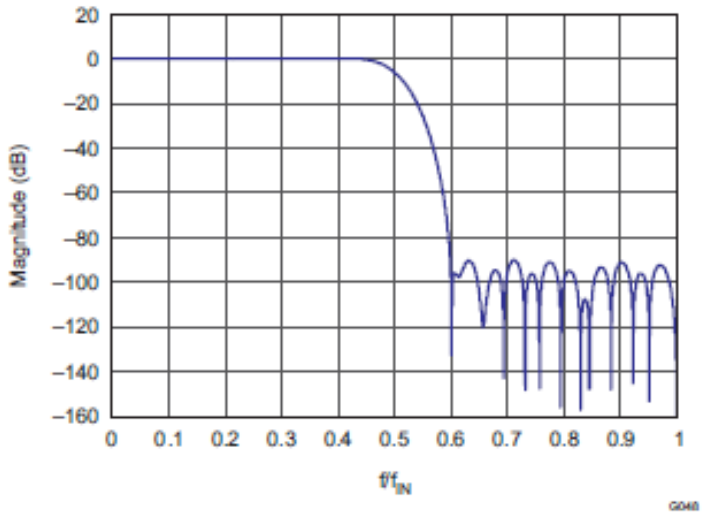


Figure 60. Magnitude Spectrum for FIR0

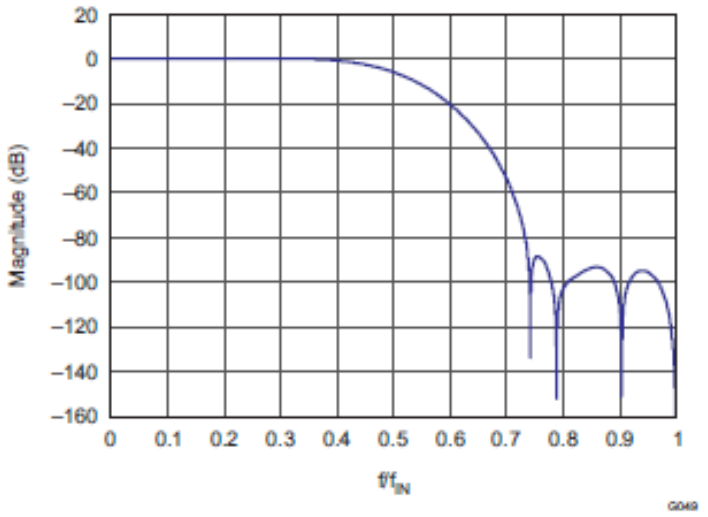


Figure 61. Magnitude Spectrum for FIR1

Advantages and Disadvantages

Key Interpolation Advantage

- Shift the DAC images further from the band of interest…easier filtering
- Allow for a wider Nyquist zone for more flexible frequency planning
- Reduces NSD as quantization noise is spread over a wider Nyquist band
- Maintain reasonable input data rates; achieve higher output frequencies

Interpolation "Penalty"

- Increased digital power consumption
- More digital logic required
- Input BW limited by interpolation filters. BW = 0.4 * Fdata

DAC38RF80 Interpolation Options

	Filters Used						
Interpolation Rate	FIR0 (2x)	FIR1 (2x)	LPFIR0_5X	FIR2 (2x)	LPFIR0_3X	FIR3 (2x)	LPFIR1_3X
6	x				x		
8	x	x		x		x	
10	x		x				
12	x	x					x
16	x	x		x		x	
18	x				x		x
20	x	x	x				
24	x	x		x			x

Sample Rate vs Data Rate with JESD204B Data Converters

- Today's JESD converters are sampling up to **9Gsps!**
  - 16 bit, JESD204B 8 lane DAC with Fs = 9Gsps, input data rate = **90Gbps per lane!**
  - Cannot be support by FPGA or ASIC's
  - Interpolation must be used to reduce the data rate
  - This would meet JESD204B max data rate of 12.5Gbps
  - ADC12J4000 with Fs = 4Gsps, output data rate = 80Gbps
  - Decimation must be used if number of lanes is less than 8.

JESD204B DAC Example

- DAC38J84: 16b Quad DAC with up to 8 lanes JESD204B up to 12.5Gbps/lane
- Data rate = 2.5Gsps/DAC, 4 DACs = M = 4, Int 4x
- Octet rate per DAC: 2 octets (16 bits) per sample. Fs = 2.5Gsps / 4 = 625Msps
  - 625Msps*2 = 1250Moctets/sample/DAC
- Bitrate per DAC: 8b/10b coding
  - 1250Moctets/s*10bits/octet = 12,500Mbps
- Total bit rate = 4 DACs * 12.500 Gbps = 50Gbps (total through put)
- If we choose L=8 lanes then the lane rate:
  - Lane rate = 50Gbps/8 = 6.25 Gbps per lane
- **LMFS=8411, lane rate = 6.25Gbps**

Min/Max Sample rates from the DAC38J84 Data Sheet

Table 11. DAC38J84 Speed Limits

L	M	F	S	HD	INTERPOLATION	Min f_{SERDES} (Gbps)	Max f_{SERDES} (Gbps)	Min f_{DATA} (MSPS)	Max f_{DATA} (MSPS)	Min f_{DAC} (MSPS)	Max f_{DAC} (MSPS)	Max BW (MHz)
8	4	1	1	1	1	1.5625	12.3	156.25	1230	156.25	1230	1230
					2	0.78125	12.3	78.125	1230	156.25	2460	984
					4	0.78125	6.25	78.125	625	312.5	2500	500
					8	0.78125	3.125	78.125	312.5	625	2500	250
					16	0.78125	1.5625	78.125	156.25	1250	2500	125

Summary

- Sample rate and Data rate are not always the same frequency.
- Decimation and Interpolation are used to reduce data rates to allow for much higher sampling rates.

Thanks for your time!