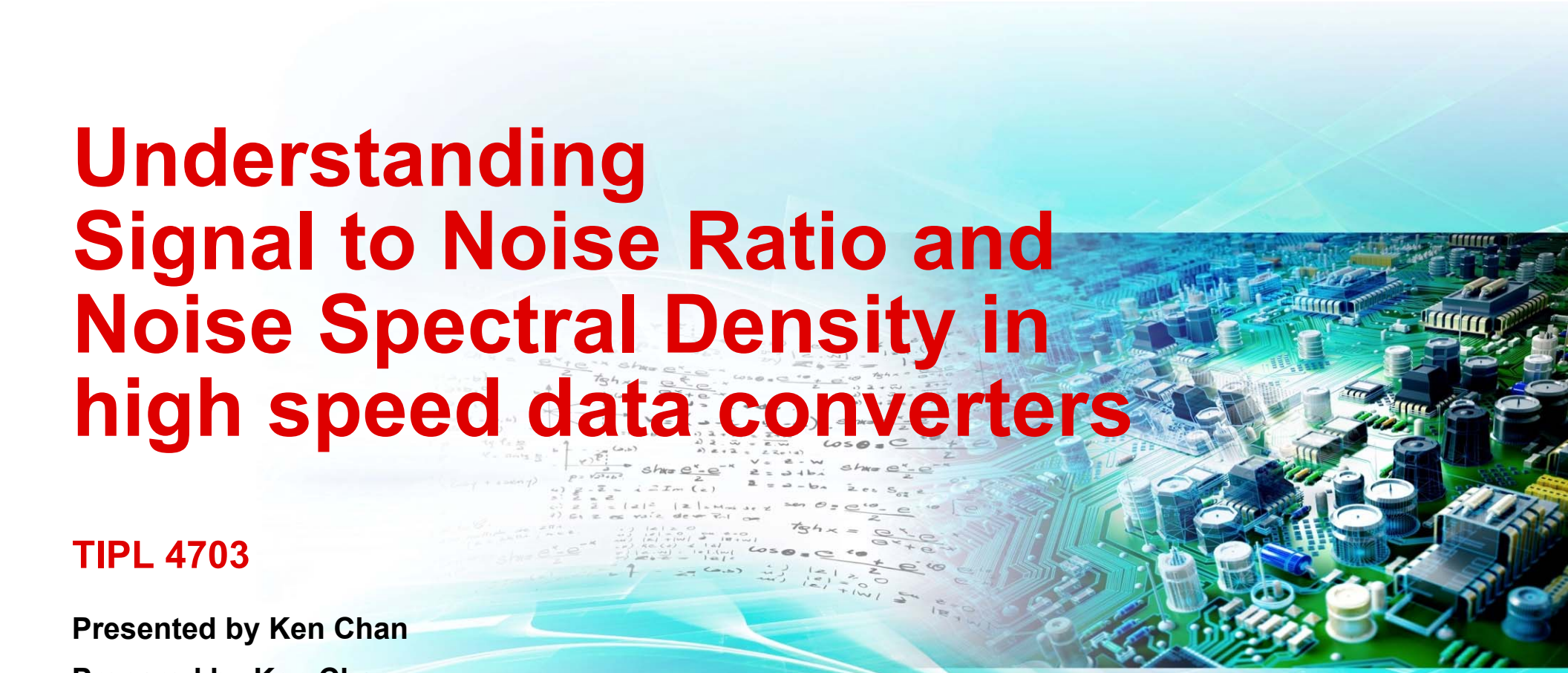
Understanding Signal to Noise Ratio and Noise Spectral Density in high speed data converters



TIPL 4703

Presented by Ken Chan

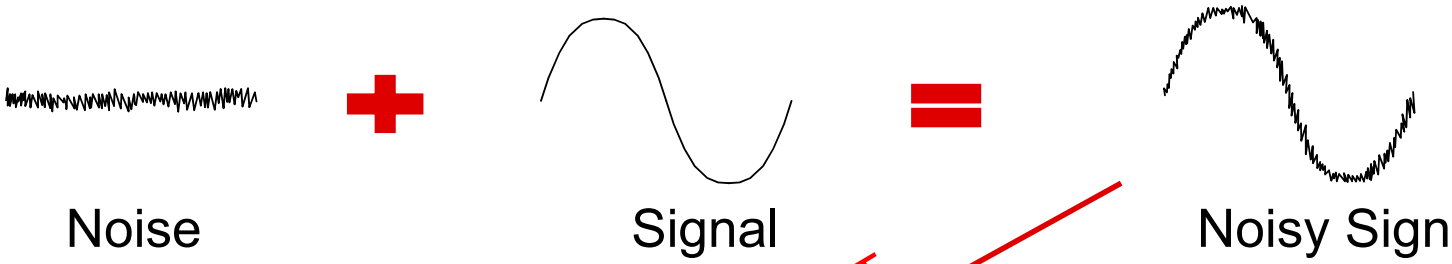
Prepared by Ken Chan

Table of Contents

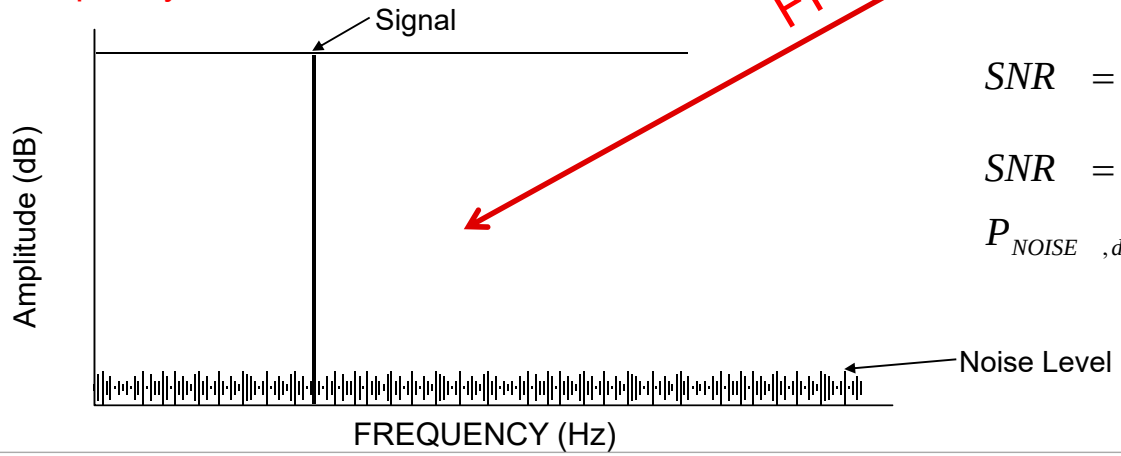
What is SNR - Signal-to-Noise Ratio Basics

- SNR is the ratio of the signal power to the noise power that corrupts the signal. This parameter does not include harmonic distortion.

In the time domain:



In the frequency domain:



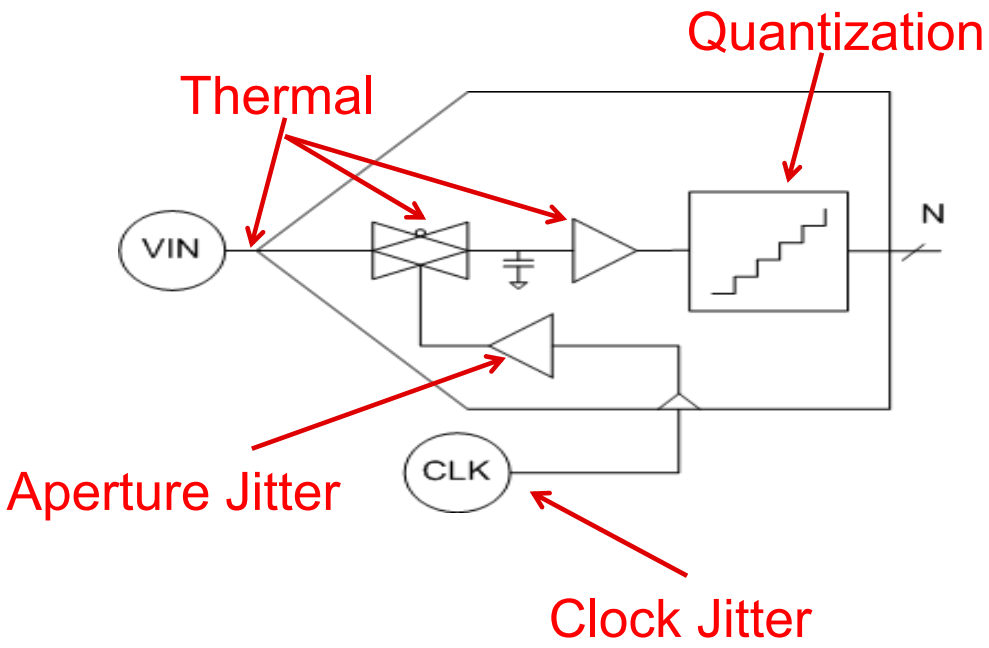
$$SNR = 10 \log \frac{P_{SIGNAL}}{P_{NOISE}}$$

$$SNR = P_{SIGNAL,dBm} - P_{NOISE,dBm}$$

$$P_{NOISE,dBm} = 10 \log P_{NOISE,dBm/Hz} + 10 \log BW_{Hz}$$

Maximizing the SNR in an ADC

$$SNR = P_{SIGNAL,dBm} - P_{NOISE,dBm}$$



SNR can be increased in the following ways:

- Increase signal power ↑
  - Full Scale Range (FSR)
- Decrease noise power ↓
  - Quantization Noise
  - Clock Jitter
  - ADC Aperture Jitter
  - Thermal Noise

SNR by Individual Noise Contributors

- Total SNR can be calculated by the sum of the individual noise sources:

$$SNR_{total} = 10 \log \left(\frac{1}{10^{-SNR_{QUANT}/10} + 10^{-SNR_{JITTER}/10} + 10^{-SNR_{THERM}/10}} \right)$$

SNR_{QUANT} = SNR due to quantization

SNR_{JITTER} = SNR due to clock and aperture jitter

SNR_{THERM} = SNR due to thermal and transistor noise

Design Choice	Effect on Noise
ADC Selection	N-bits affects quantization noise, aperture jitter and thermal noise by design
Sampling Clock Selection	Clock jitter
Sampling Rate	Bandwidth over which noise is distributed

Quantization Noise and SNR

- SNR due to quantization error, assuming a sine wave input:

$$SNR_{QUANT} = 6.02 \cdot N + 1.76 \quad dB$$

Example: 14-bit converter where N=14:

$$SNR_{QUANT} = 6.02 \cdot 14 + 1.76 = 86.04 \quad dB$$

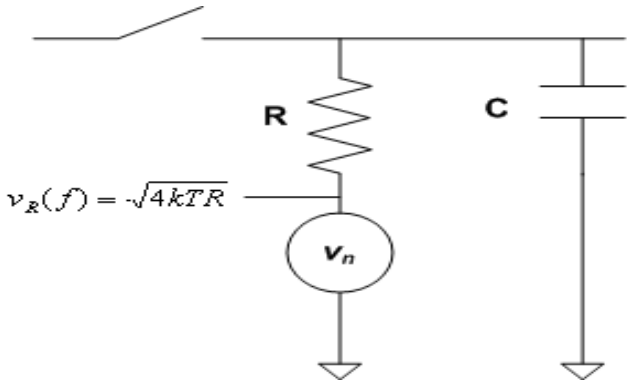
- How to determine the required ADC resolution?
  - An N-bit ADC determines the maximum possible SNR for the system
  - Practically, an ADC's SNR is limited by other factors:
    - Sampling clock jitter
    - ADC jitter and thermal noise
    - Other system noise sources
    - Over-sampling rate and application channel bandwidth

Transistor and Thermal Noise and SNR

Noise Mechanism	α	Spectral Profile	Source	Cause
Shot	I_{DC}	white	pn-junctions	DC bias current is not constant
Flicker	1/f	1/f	Active devices	Carriers are “trapped” and released in a semiconductor
Thermal	T	white	resistors	Thermal excitation of carriers in a conductor

Noise in an ADC:

- Track-and-hold is dominant source
- Capacitors source no noise
- Resistor results in “kT/C” noise



$$v_{no}^2(f) = v_R^2(f) * \frac{\pi}{2} * f_o$$

$$= (4kTR) * (\frac{\pi}{2}) * (\frac{1}{2\pi RC})$$

$$= \frac{kT}{C}$$

Clock Jitter and SNR

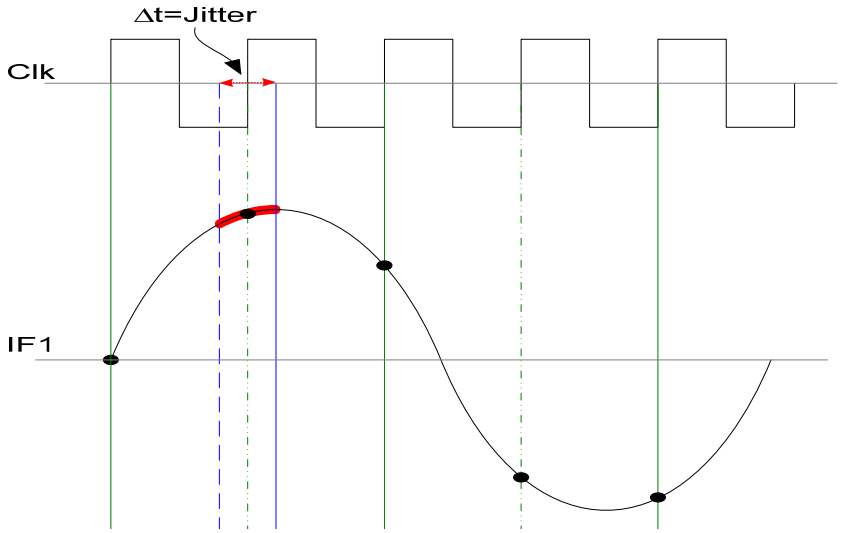
- *Clock jitter* is the random variation of the clock edge compared to its ideal point in time
- Theoretical limit of SNR due to jitter:

$$SNR_j[dBc] = -20 \cdot \log(2\pi f_{in} \cdot \tau_j)$$

where :

f_{in} = *input frequency*

τ_j = *clock jitter*

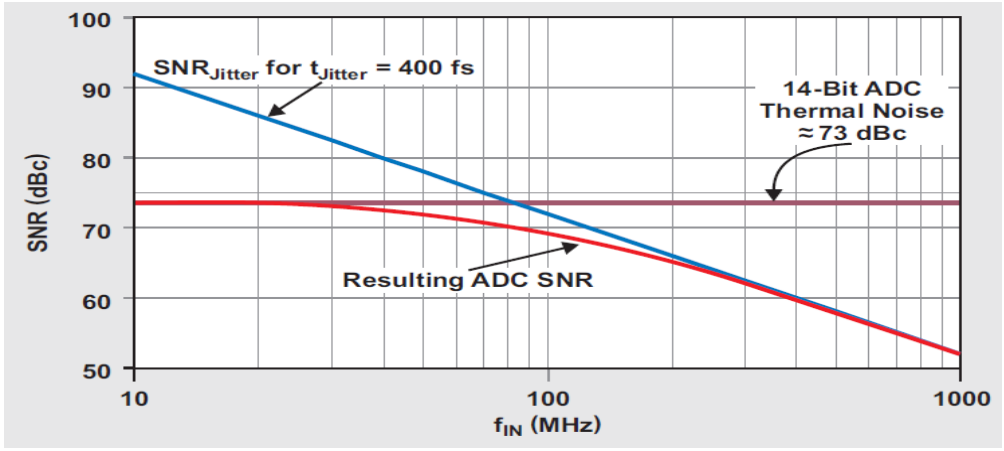


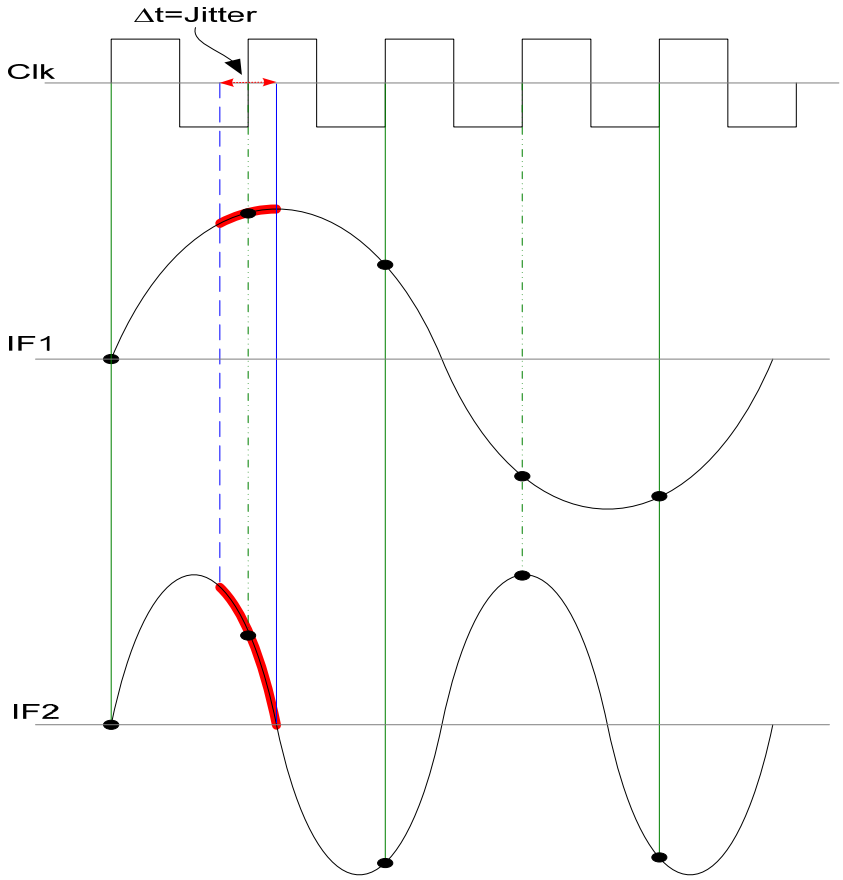
- Total jitter is the rms sum of the individual jitter contributions
  - For ADCs, this is generally the external clock jitter and aperture jitter

$$\tau_T = \sqrt{\tau_{external}^2 + \tau_{aperture}^2}$$

More on Clock Jitter

- Clock jitter causes imprecise sampling intervals which results in incorrect sampling instances and therefore errors in the sampled signal
- Clock jitter has an increased effect at higher input frequencies or higher maximum input slew rates





Sources of Clock Jitter

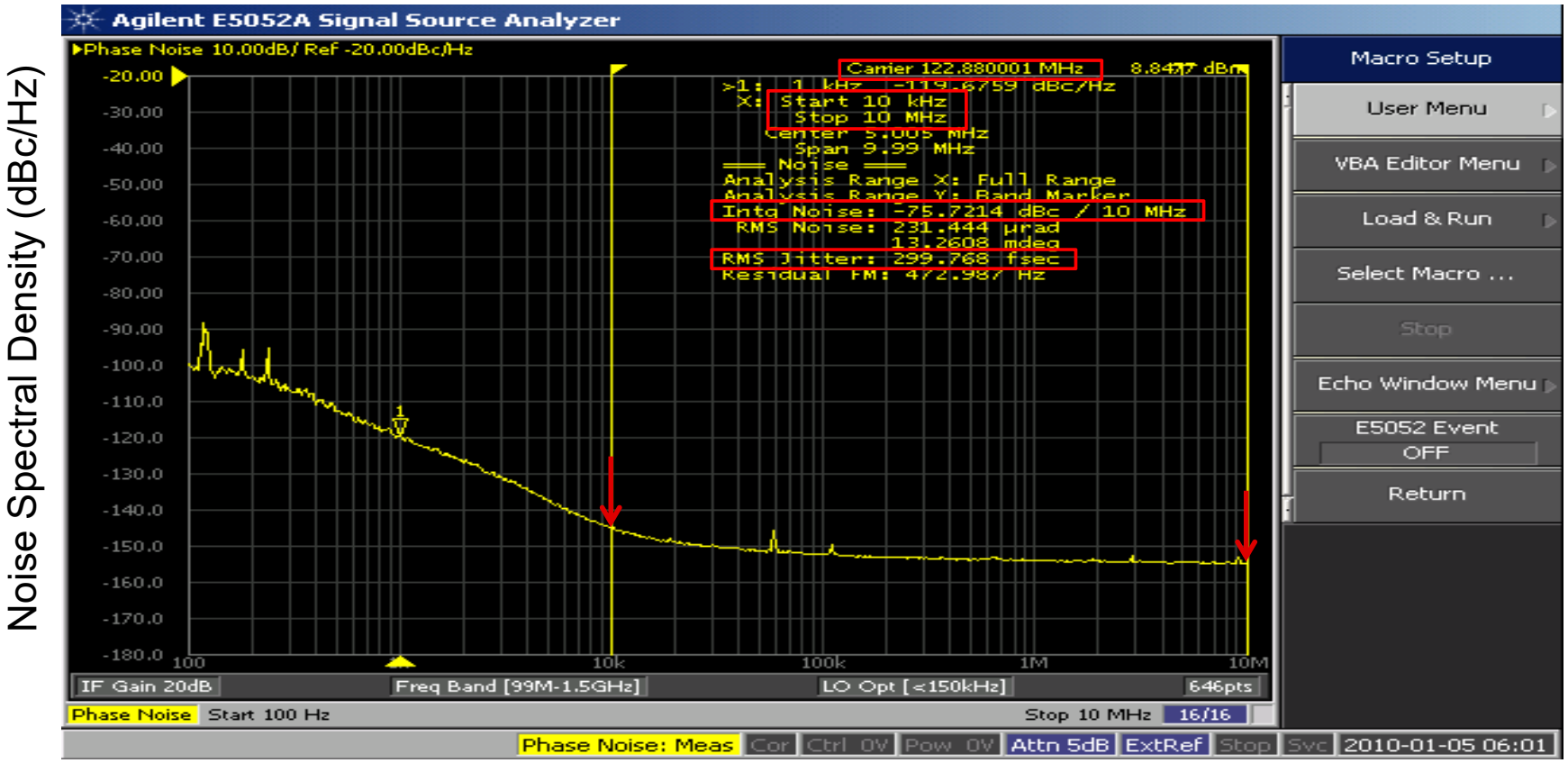
- The total clock jitter for an ADC is from the ***aperture jitter*** and the external sampling ***clock jitter***.
- *Clock jitter* is the jitter contribution from the external clock source and can be measured by using a phase noise analyzer
- *Aperture jitter* (a.k.a. aperture uncertainty) is the jitter contribution from the ADC, due to the internal clock buffers. This cannot be measured directly using a phase noise analyzer.
- ***Example:*** aperture jitter for the ADS4249

PARAMETER		DESCRIPTION	MIN	TYP	MAX	UNIT
t_J	Aperture jitter			140		f_S rms

- The *total clock jitter* is determined by rms sum of all individual contributions:

$$\tau_{TOTAL} = \sqrt{\tau^2_{EXTERNAL} + \tau^2_{APERTURE}}$$

Example Phase Noise Plot



Noise Spectral Density (dBc/Hz)

Frequency (MHz)

Calculating Jitter from Clock Phase Noise

- Jitter is a result of noise on the sampling clock. Assuming the wideband clock noise is relatively low, then the clock jitter is calculated by integrating the clock phase noise over a specified BW then converting to seconds.

$$\tau_j = \frac{\sqrt{2 \cdot 10^{\frac{\Phi_N}{10}}}}{2\pi f_{clk}}$$

Where:
Φ_N= Phase Noise Power (dBc)
f_0, f_1= frequency limits of integration
τ_j = clock jitter

- Example from previous slide's phase noise plot:
  - Φ_N = -75.72 dBc/Hz (from 10 kHz to 10 MHz offset)
  - F_{clk} = 122.88 MHz

$$\tau_j = \frac{\sqrt{2 \cdot 10^{\frac{-75.72\ dBc/Hz}{10}}}}{2\pi(122.88\ MHz)} = 299.77\ fs$$

A DIFFERENT WAY TO LOOK AT CLOCK JITTER/NOISE

Limitation of the Traditional SNR Calculation Due to Jitter

- The traditional SNR due to jitter equation gives the SNR over the entire Nyquist band, with the jitter measured over a wide clock offset frequency
- The equation is a function of the analog input frequency and jitter performance

$$SNR_j[dBc] = -20 \cdot \log(2\pi f_{in} \cdot \tau_j)$$

where :

f_{in} = *input frequency*

τ_j = *clock jitter*

- If the ADC clock is already fine tuned to the best jitter performance, would the only option left to meet stringent SNR performance is to adjust the input frequency?
- If so, what is the point of over-sampling ADCs?

General Equation for ADC SNR

- It turns out the SNR equation is also a function of clock frequency as well. Recall the jitter equation:

$$\tau_j = \frac{\sqrt{2 \cdot 10^{\frac{\Phi_N}{10}}}}{2\pi f_{clk}}$$

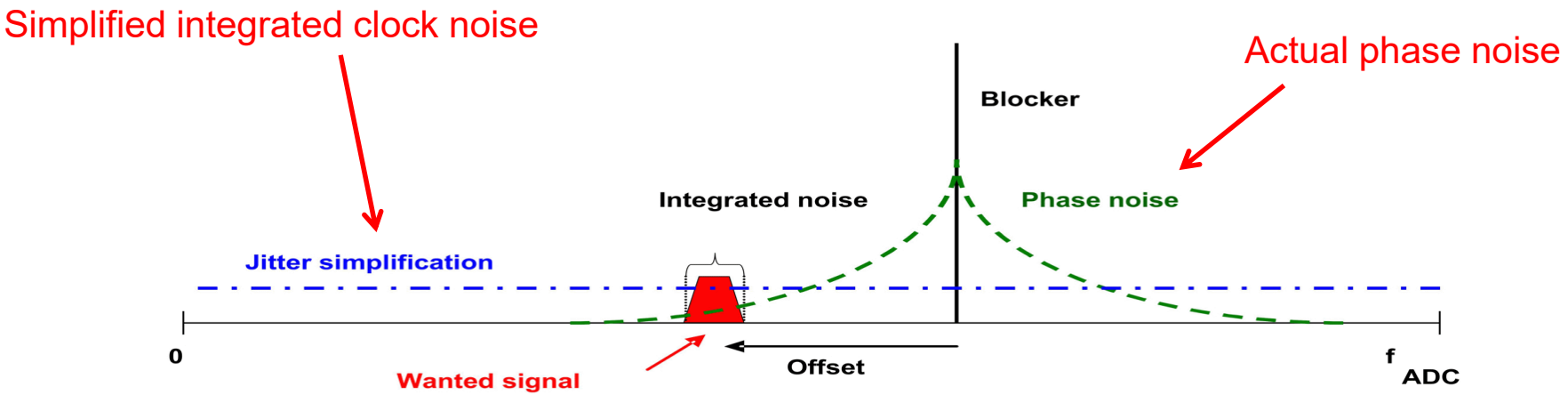
- If we substitute the jitter equation into the SNR equation, we would get the following:

$$\begin{aligned} SNR_j[dBc] &= -20 \cdot \log\left(2\pi f_{in} \cdot \frac{\sqrt{2 \cdot 10^{\frac{\Phi_N}{10}}}}{2\pi f_{clk}}\right) \\ &= -20 \cdot \log\left(\sqrt{2 \cdot 10^{\frac{\Phi_N}{10}}} \cdot \frac{f_{in}}{f_{clk}}\right) \\ &= -20 \cdot \log\left(\sqrt{2 \cdot 10^{\frac{\Phi_N}{10}}}\right) - 20 \cdot \log\left(\frac{f_{in}}{f_{clk}}\right) \\ &= -20 \cdot \log\left(\sqrt{2 \cdot 10^{\frac{\Phi_N}{10}}}\right) + 20 \cdot \log\left(\frac{f_{clk}}{f_{in}}\right) \end{aligned}$$

- The first term is the inherent integrated noise due to clock noise. The second term is a correction term. This is important to help us understand the performance of over-sampling. If over-sampling is used, the SNR can be improved

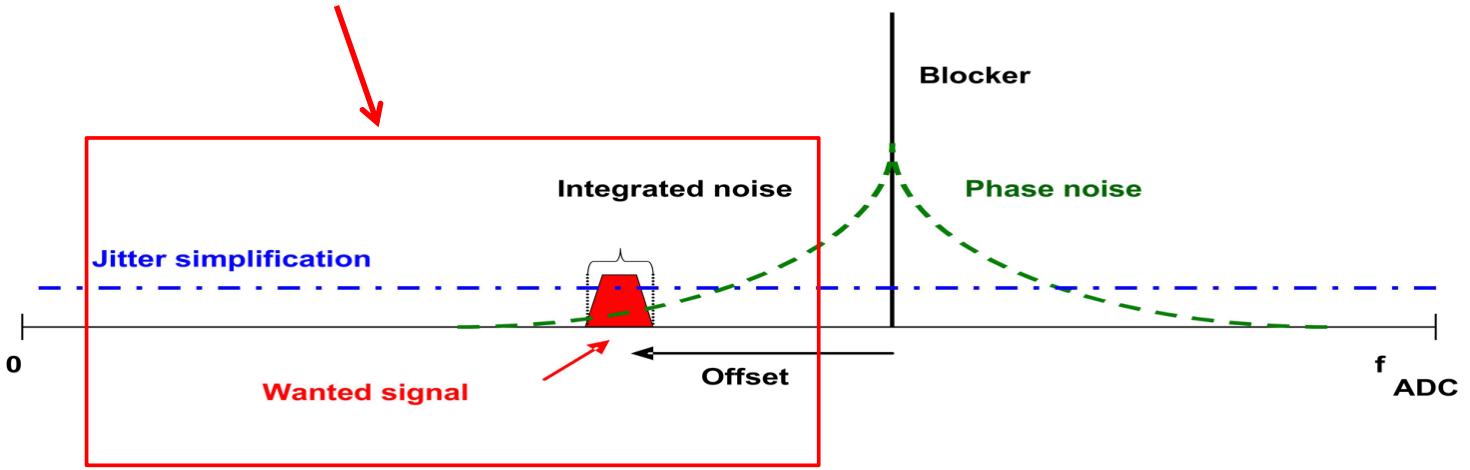
Why is the general equation important?

- The general equation is important because the traditional equation often simplifies the ADC clock noise floor as an uniform white noise.
- In reality, the ADC clock usually has better noise behavior as the offset frequency increases, and also, the clock is often well filtered.



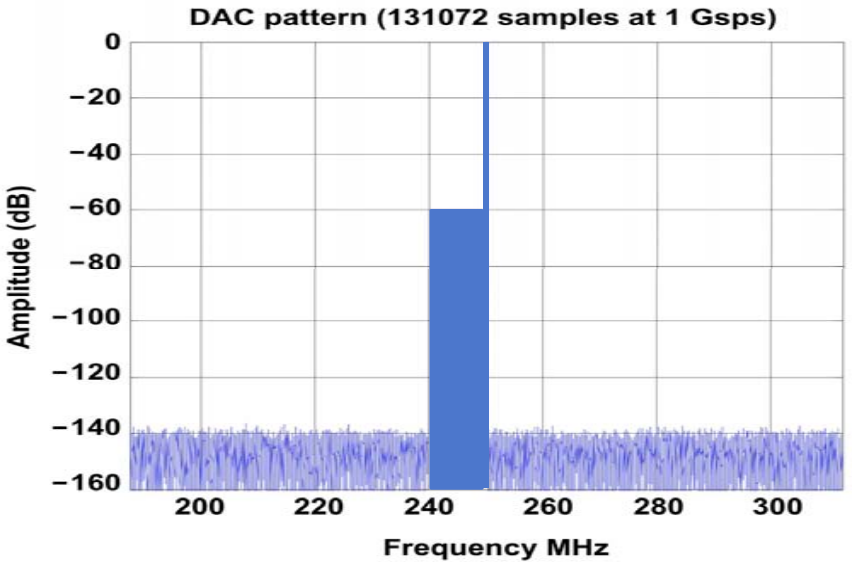
System Requirement Implication

- Most importantly, some of the stringent system requirements often are bandwidth specific. I.e. noise spec over a specific bandwidth.
- For instance, when given a certain blocker signal, the traditional SNR calculation may overestimate the noise over the bandwidth of the wanted signal. This may make jitter specification of the clock impossible to achieve.



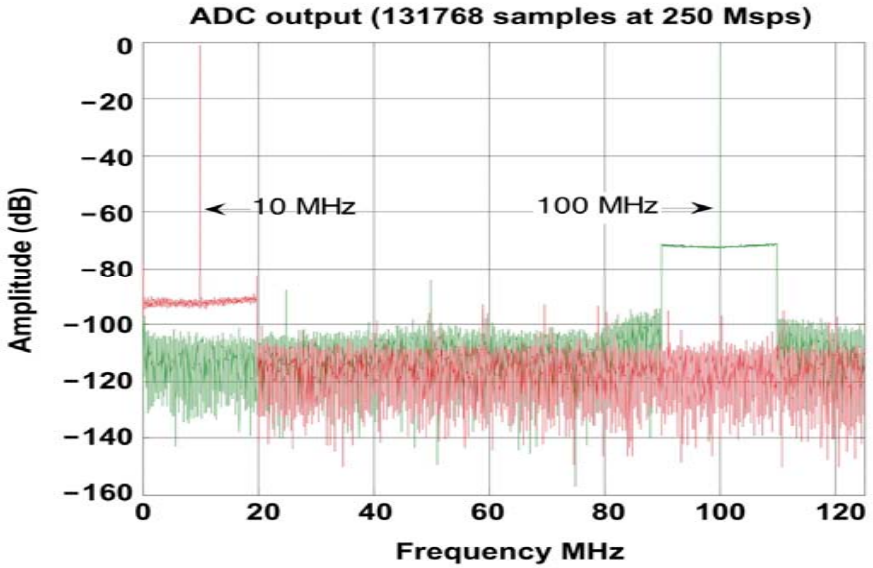
Experiment Result

Clocking the ADC with a 250MHz tone + 10MHz noise ranging from 240MHz to 250MHz



(DAC5681 output)

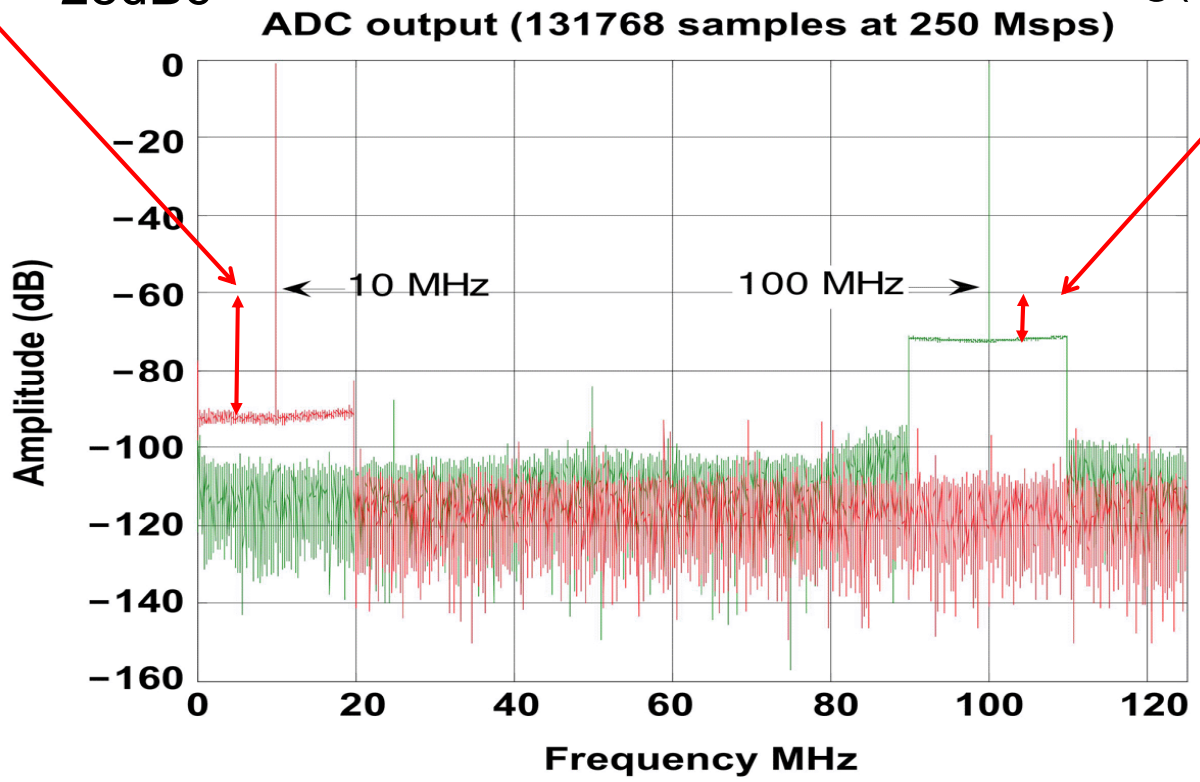
ADS4149 at 250MSPS
Two inputs shown and overlaid: 10MHz and 100MHz



ADC Test Result

20log(250/10) = 28dBc

20log(250/100) = 8dBc



DAC NSD VS SNR

SNR Jitter estimate is the same for DACs

- The total SNR is the vector sum of all individual SNR contributions

$$SNR_{total} = 10 \log\left(\frac{1}{10^{-SNR_{QUANT}/10} + 10^{-SNR_{CLK}/10} + 10^{-SNR_{THERM}/10}}\right)$$

SNR_{QUANT} = SNR due to quantization
SNR_{CLK} = SNR due to clock and aperture jitter
SNR_{THERM} = SNR due to thermal and transistor noise

- Similar treatment of clock jitter (integrated phase noise) for SNR limit of DAC sampled system

$$SNR_j[dBc] = -20 \cdot \log(2\pi f_{if} \cdot \tau_j)$$

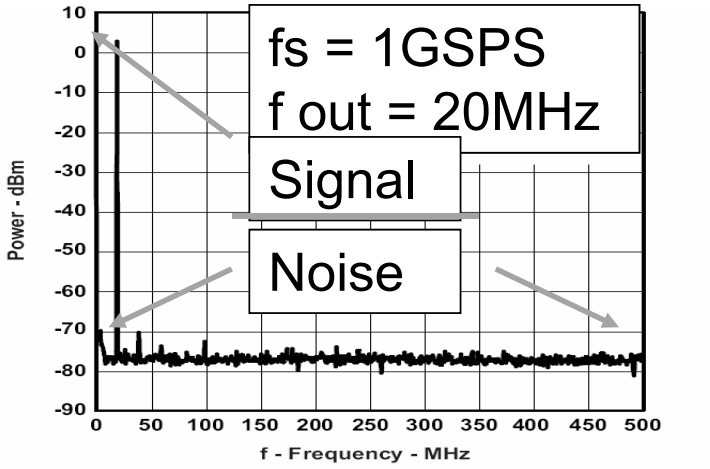
$where$:

$f_{if} = output \quad frequency$

$\tau_j = clock \quad jitter$

NSD or SNR?

- For DACs, generally the noise spectral density (NSD) is more important than overall SNR
  - The shape of the NSD around the carrier must meet mask requirements
  - When SNR is required, customer's often limit the bandwidth of the transmitted signal by a bandpass or lowpass filter
- For this reason, newer datasheets report NSD rather than SNR



- DAC output noise is comprised of
  - Quantization noise
  - Thermal noise
  - Jitter noise
  - Data dependent noise

Why NSD over SNR?

- In real systems, there is often tight filtering around the band of interest, where all the noise outside of that band is filtered out.
- Rather than showing the SNR of the signal in the first Nyquist zone, it is more convenient to show the noise power so that the total noise power in the unfiltered band can be readily calculated
- For example, consider a DAC3484 running at 1228.8 MSPS with a band of interest of 100 MHz and the following filters:
  - A 614.4-MHz low-pass filter (passing full first Nyquist zone):

$$SNR_{dBFS} = 0\ dBFS - (-160\ dBc/Hz + 10\log(614.4\ MHz)) = 72.12\ dBFS$$

  - A 100-MHz low-pass filter:

$$SNR_{dBFS} = 0\ dBFS - (-160\ dBc/Hz + 10\log(100\ MHz)) = 80\ dBFS$$

Converting NSD to SNR

- The SNR of the DAC can be calculated from the NSD spec
- The SNR was traditionally defined as the ratio of the power of the fundamental to the power of the noise integrated over the first Nyquist zone.

$$SNR_{dBc} = P_{dBm,\ fundamental} - \left(NSD_{dBm/Hz} + 10 \log\left(\frac{F_S}{2}\right)\right)$$

- It can also be calculated directly in dBFS from the NSD in dBc/Hz

$$SNR_{dBFS} = 0\ dBFS - \left(-NSD_{dBc/Hz} + 10 \log\left(\frac{F_S}{2}\right)\right)$$

- Example: DAC3484 running at 1.25 GSPS with 10 MHz output

$$SNR_{dBFS} = 0\ dBFS - \left(-160\ dBc/Hz + 10 \log\left(\frac{1.25\ GHz}{2}\right)\right) = 72.04\ dBFS$$

NSD to SNR tradeoffs – Jitter/Phase noise

- SNR estimates based on Jitter are good estimates for SNR for the entire Nyquist band – may be too pessimistic for BW limited applications.
- SNR estimates based on NSD (typically measured at some MHz offset) do not account for close-in phase noise which could affect inband EVM
  - Useful for out of band estimates like ACPR
  - Also useful for transmit mask requirements
- Using the clock NSD curve and BW limited noise calculations would be the ideal solution for in-band and out-of-band measurements.