Understanding and Comparisons of High Speed ADC and DAC Architectures
TIPL 4706

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Architectures

• Flash converter
  – Track and hold

• Comparators
  – For n bits:
    • $2^n - 1$ comparators
Architectures

- Pipelined – successive stages of flash
  - Each stage adds n bits more precision
    - Requires good matching/trimming
Architectures

- SAR – Successive Approximation
  - DAC = digital-to-analog converter
  - EOC = end of conversion
  - SAR = successive approximation register
  - S/H = sample and hold circuit
  - $V_{in}$ = input voltage
  - $V_{ref}$ = reference voltage
- Source - Wikipedia
ADC Interleaving Basics

- Multiple ADC cores sample signal to increase total sampling rate
- ADC cores sample at same divided frequency but different phase offset
- Digital outputs are re-aligned in time
- Input buffer typically drives cores
Non-Ideal Interleaving

- **Offset Errors**
  - Mismatched ADC core voltage offset

- **Amplitude Errors**
  - ADC core gain error
  - ADC reference voltage error

- **Phase Errors**
  - Input routing delay
  - Input BW difference
  - Clock phase error
  - ADC sampling instant
Non-Ideal Interleaving

- Offset Error
  - Different voltage offset at ADC input between different cores
- Alternating up/down in transient waveform
- Creates signal independent spurss in spectrum at $F_s*n/N$ for $n=1,2,...,N-1$ where $N$ is # of interleaved cores
Non-Ideal Interleaving

- Amplitude (Gain) errors
  - Gain difference between different ADC cores
- Creates N-1 input signal dependent images from 0 to $F_s/2$ in a repetitive, mirror-image pattern where N is # of interleaved cores
- Also creates harmonic distortion images

![Diagram showing input signal and images](image-url)
Interleaving Correction

- Relying on process matching not suitable for most applications
- Interleave correction reduces spectrum offset spurs and images
- *Estimate* the errors and *correct* the data with coefficients
- Estimation
  - Detection in time-domain or frequency domain
  - Convergence
- Correction
  - Analog/Digital
- Calibration time
  - Foreground: Calibration interrupts normal operation
  - Background: Calibration runs continuously
## Current Steering DAC

### Diagram Description:
- **DAC**: The input for the decoder logic.
- **Decoder Logic**: Processes the digital input data.
- **Switch Drivers**: Controls the switch array.
- **Switch Array**: Switches the current outputs.
- **Bias Circuit**: Provides the bias for the current source array.
- **Current Source Array**: Produces the analog outputs.
- **Analog Output**: The final output of the DAC.

### Table: Full Scale = 30mA

<table>
<thead>
<tr>
<th>Digital Input</th>
<th>IOUT1</th>
<th>IOUT2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0mA</td>
<td>30mA</td>
<td>0mA</td>
</tr>
<tr>
<td>15mA</td>
<td>15mA</td>
<td>0mA</td>
</tr>
<tr>
<td>30mA</td>
<td>0mA</td>
<td>30mA</td>
</tr>
</tbody>
</table>
DACs can be current source or current sink

**PMOS**

- VCC
- Current Source Cascodes
- Switches
  - +1/0.5 Volts
  - -1/0.5 Volts

DAC90x, DAC290x, DAC2932, DAC56x2
DAC34xx, DAC3174

**NMOS**

- VCC + 0.5 Volts
- VCC - 0.5 Volts
- Switches
- Current Sink Cascodes

DAC5686/87/88/89, DAC5681/82Z, DAC3282/83, DAC3152/62

Texas Instruments
Simple 3-bit Binary DAC

Pro: Least number of current sources and switches.
Con: Higher distortion.
Equivalent 3-bit Thermometer Coded DAC

Pro: Reduced distortion (easier to match equal current sources.)
Con: More current sources and switches required.

One more equal valued current source turns on

Pro: Reduced distortion (easier to match equal current sources.)
Con: More current sources and switches required.
DACs can be segmented and mixed coded

- Input 6b word
- Decoder logic

Therm(7:1) to MSB segment
Bit(3:1) to LSB segment

Thermometer 3b
MSB DAC

Binary 3b LSB DAC

Vout
Simplified TI 16b DAC topology

Ex: DAC34xx

D(15:10) (6 MSB Bits)
MSB segment decoding

D(9:0) (10 LSB Bits)
LSB segment decoding

MSB Thermo(63:0)

LSB binary(9:0)

73 switch drivers

73 switches

63

10

bias circuits

MSB cascodes
MSB current sources

LSB cascodes
LSB current sources

IOUT1

IOUT2

EXTIO
RBIAS

IOUT1

IOUT2
Thanks for your time!