Understanding and Comparisons of High Speed ADC and DAC Architectures

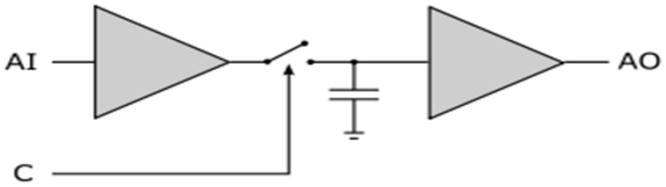
TIPL 4706

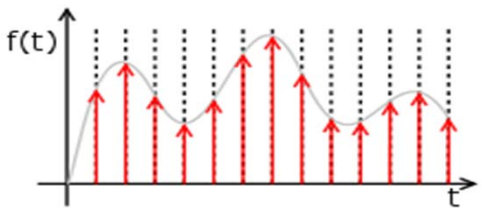
Presented by Richard Prentice

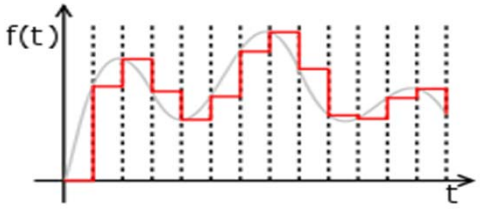
Prepared by Richard Prentice

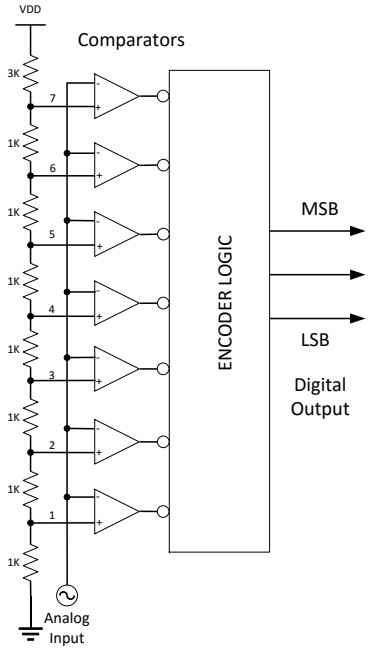
Architectures

- Flash converter
  - Track and hold





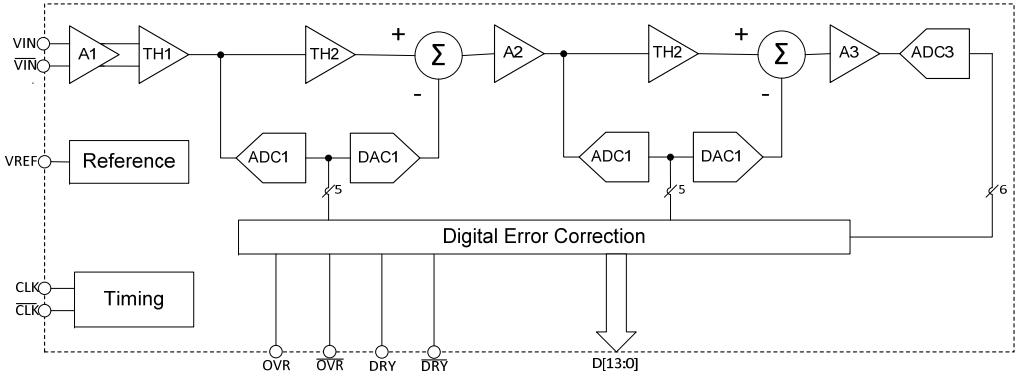


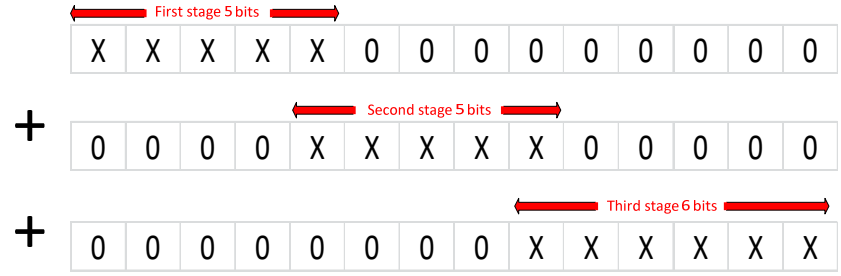


- **Comparators**
  - **For n bits:**
    - **2^n – 1 comparators**

Architectures

- Pipelined – successive stages of flash
  - Each stage adds n bits more precision
    - Requires good matching/trimming

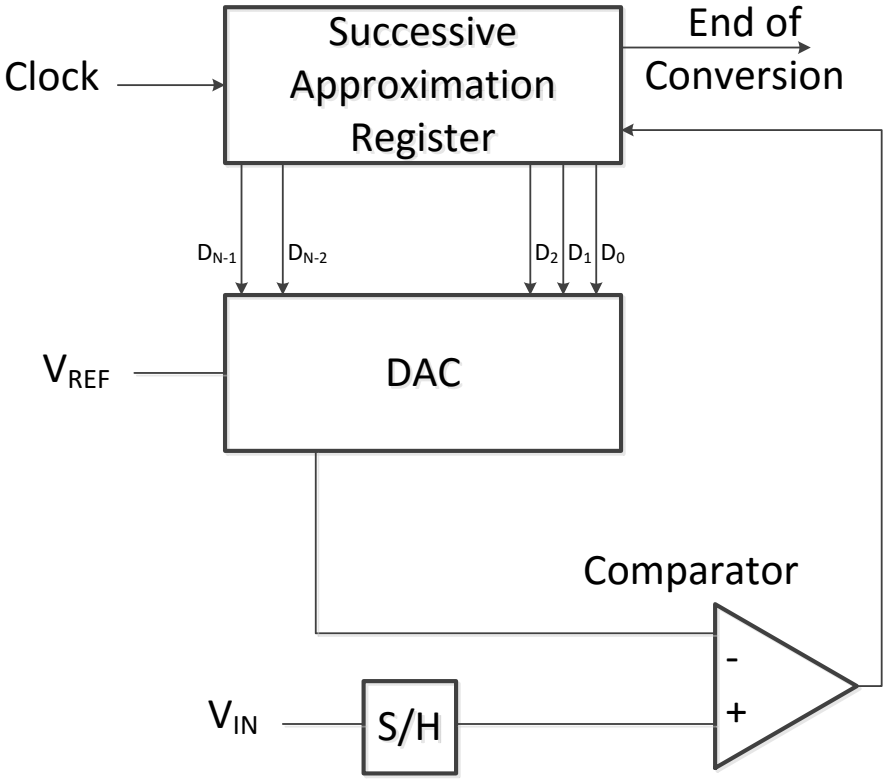




Result = (First stage bits * 512) + (Second stage bits * 32) + Third stage bits

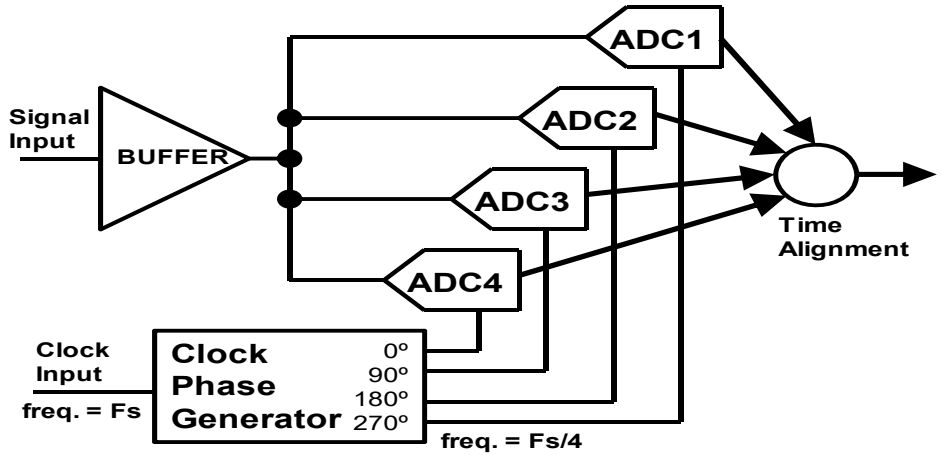
Architectures

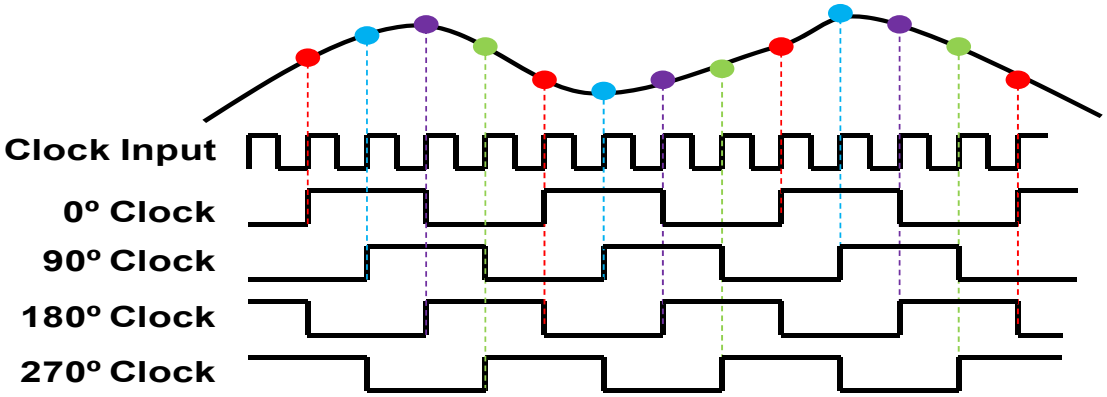
- SAR – Successive Approximation
  - DAC = digital-to-analog converter
  - EOC = end of conversion
  - SAR = successive approximation register
  - S/H = sample and hold circuit
  - V_{in} = input voltage
  - V_{ref} = reference voltage
    - Source - Wikipedia



ADC Interleaving Basics

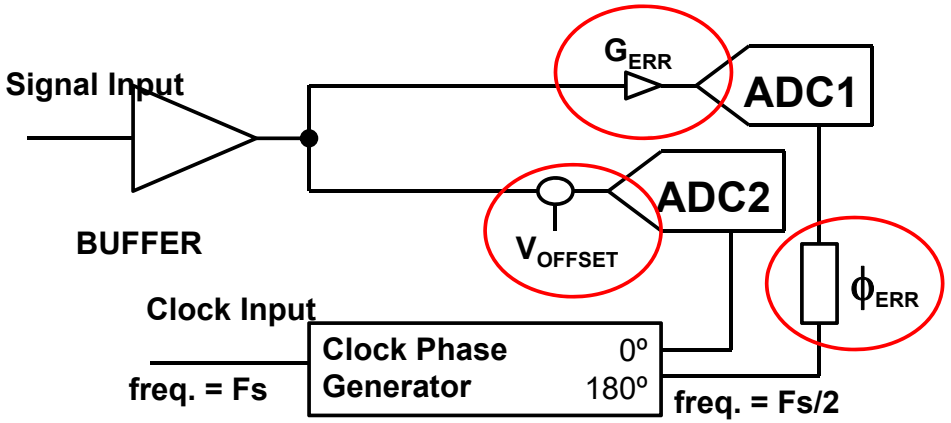
- Multiple ADC cores sample signal to increase total sampling rate
- ADC cores sample at same divided frequency but different phase offset
- Digital outputs are re-aligned in time
- Input buffer typically drives cores





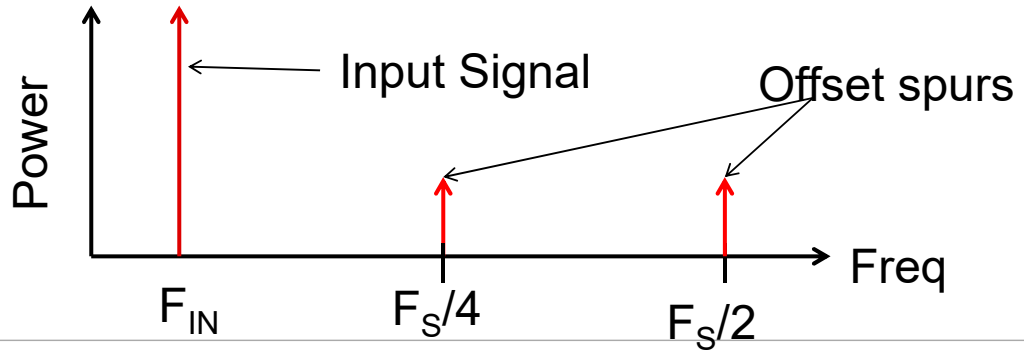
Non-Ideal Interleaving

- Offset Errors
  - Mismatched ADC core voltage offset
- Amplitude Errors
  - ADC core gain error
  - ADC reference voltage error
- Phase Errors
  - Input routing delay
  - Input BW difference
  - Clock phase error
  - ADC sampling instant

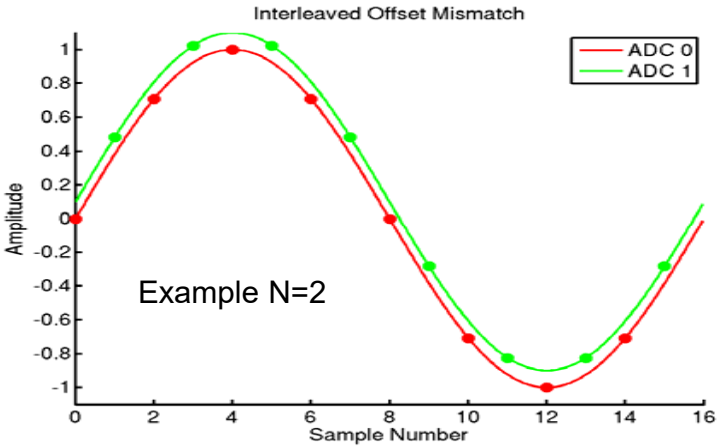


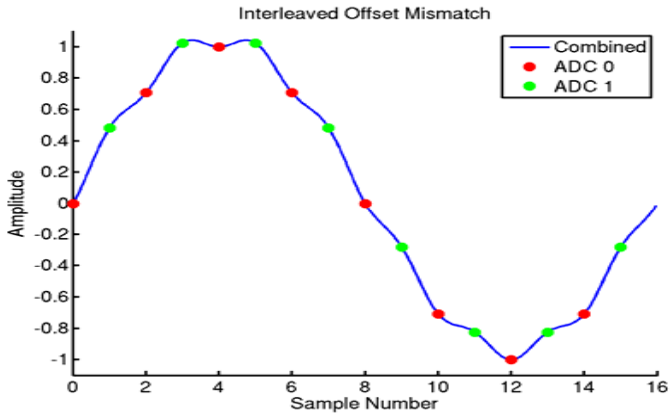
Non-Ideal Interleaving

- Offset Error
  - Different voltage offset at ADC input between different cores
- Alternating up/down in transient waveform
- Creates signal independent spurs in spectrum at Fs*n/N for n=1,2,…,N-1 where N is # of interleaved cores



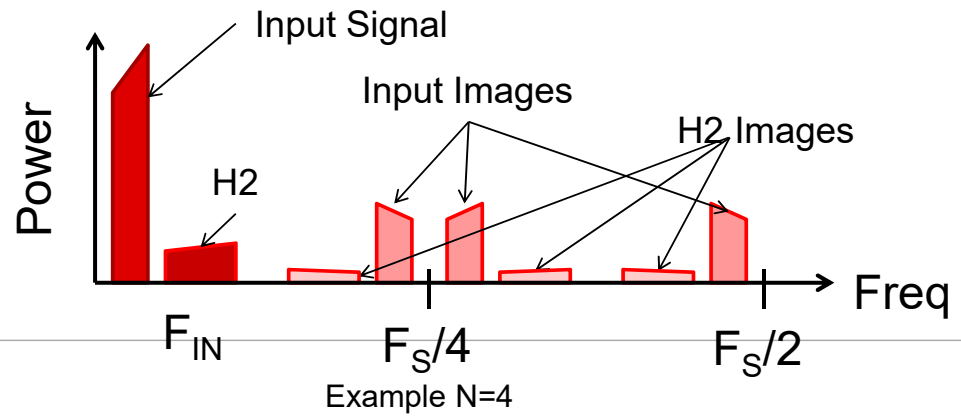
Example N=4

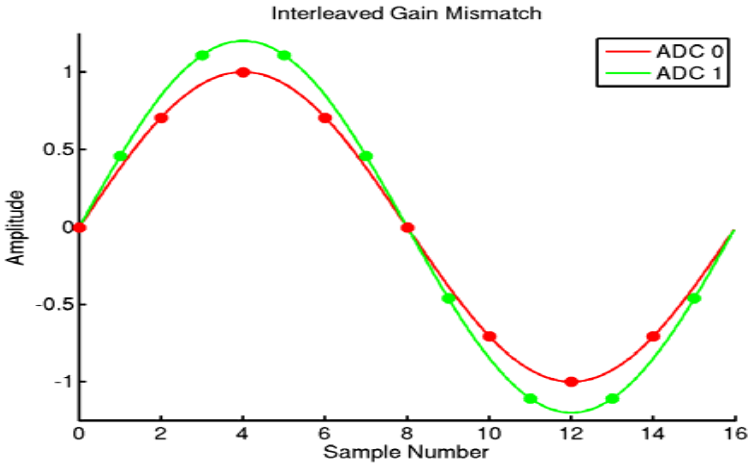


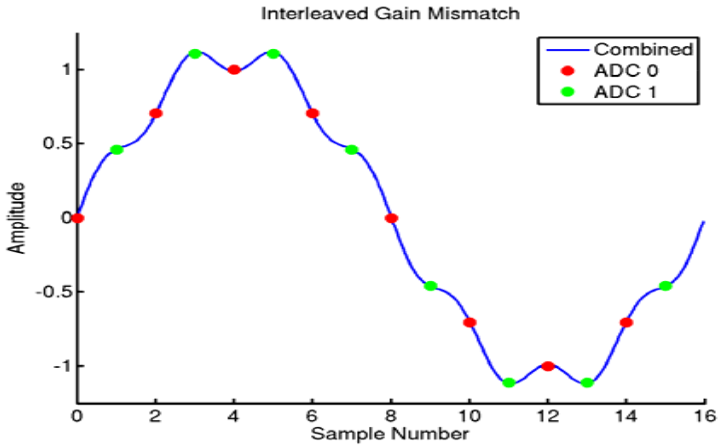


Non-Ideal Interleaving

- Amplitude (Gain) errors
  - Gain difference between different ADC cores
- Creates N-1 input signal dependent images from 0 to Fs/2 in a repetitive, mirror-image pattern where N is # of interleaved cores
- Also creates harmonic distortion images



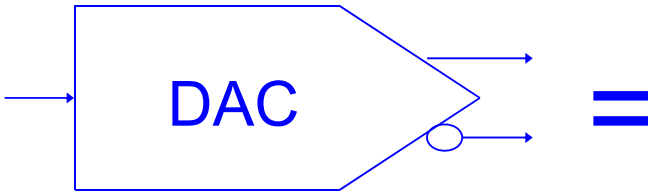




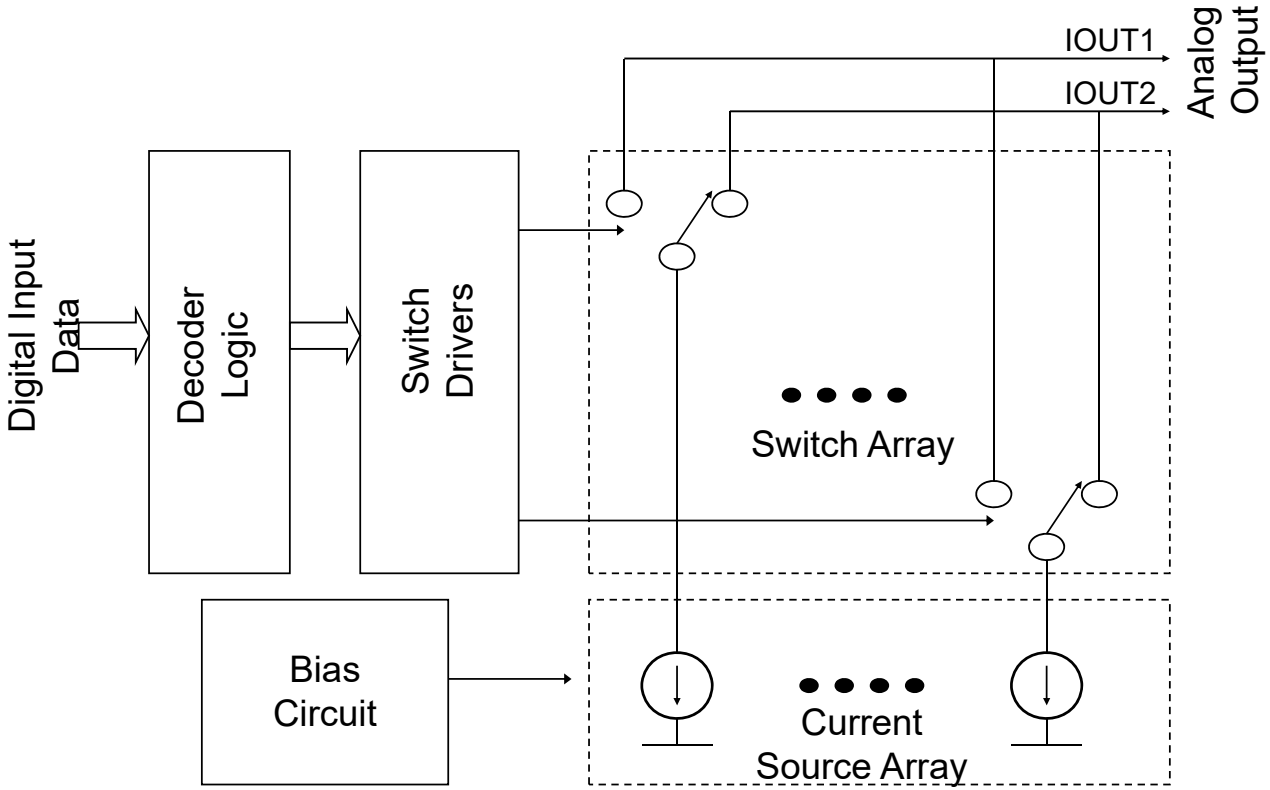
Interleaving Correction

- Relying on process matching not suitable for most applications
- Interleave correction reduces spectrum offset spurs and images
- *Estimate* the errors and *correct* the data with coefficients
- Estimation
  - Detection in time-domain or frequency domain
  - Convergence
- Correction
  - Analog/Digital
- Calibration time
  - Foreground: Calibration interrupts normal operation
  - Background: Calibration runs continuously

Current Steering DAC



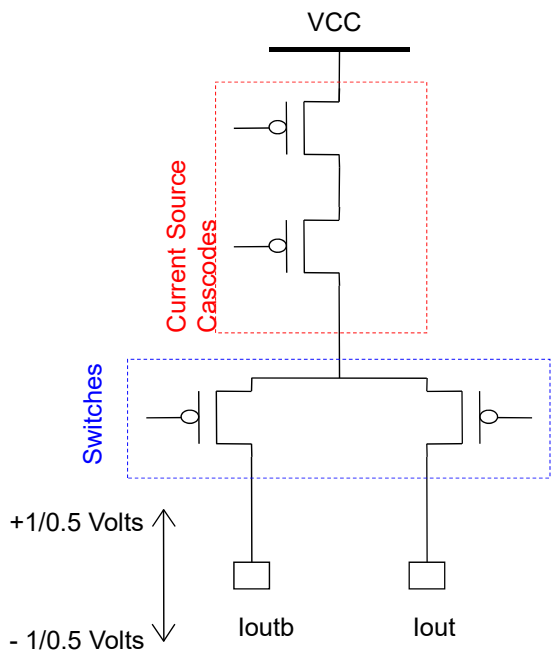
=



Full Scale = 30mA	
IOUT1	IOUT2
30mA	0mA
15mA	15mA
0mA	30mA

DACs can be current source or current sink

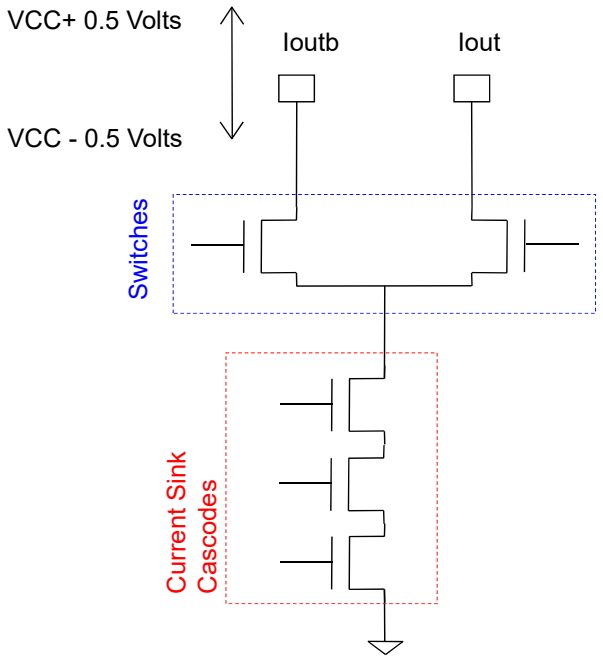
PMOS



DAC90x, DAC290x, DAC2932, DAC56x2

DAC34xx, DAC3174

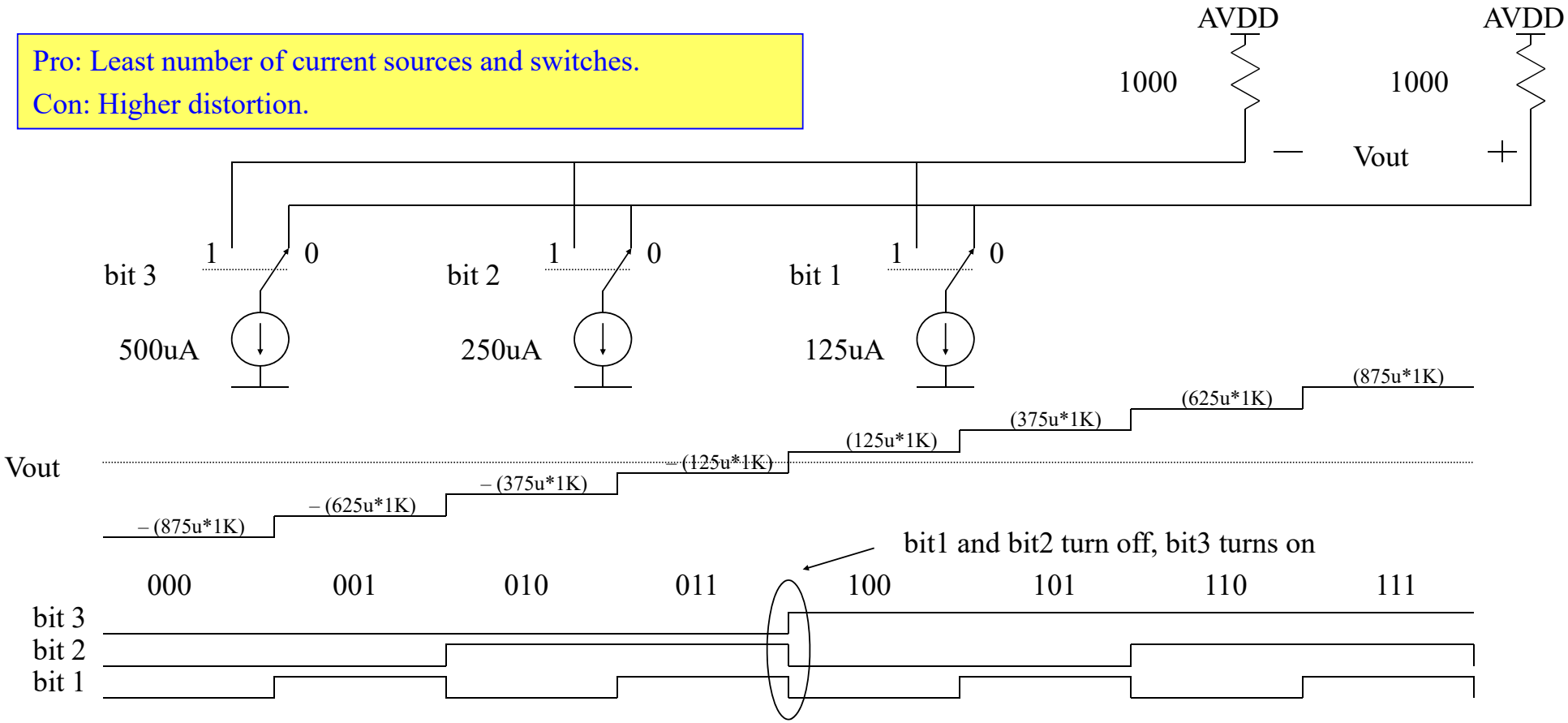
NMOS



DAC5686/87/88/89,
DAC5681/82Z,
DAC3282/83
DAC3152/62

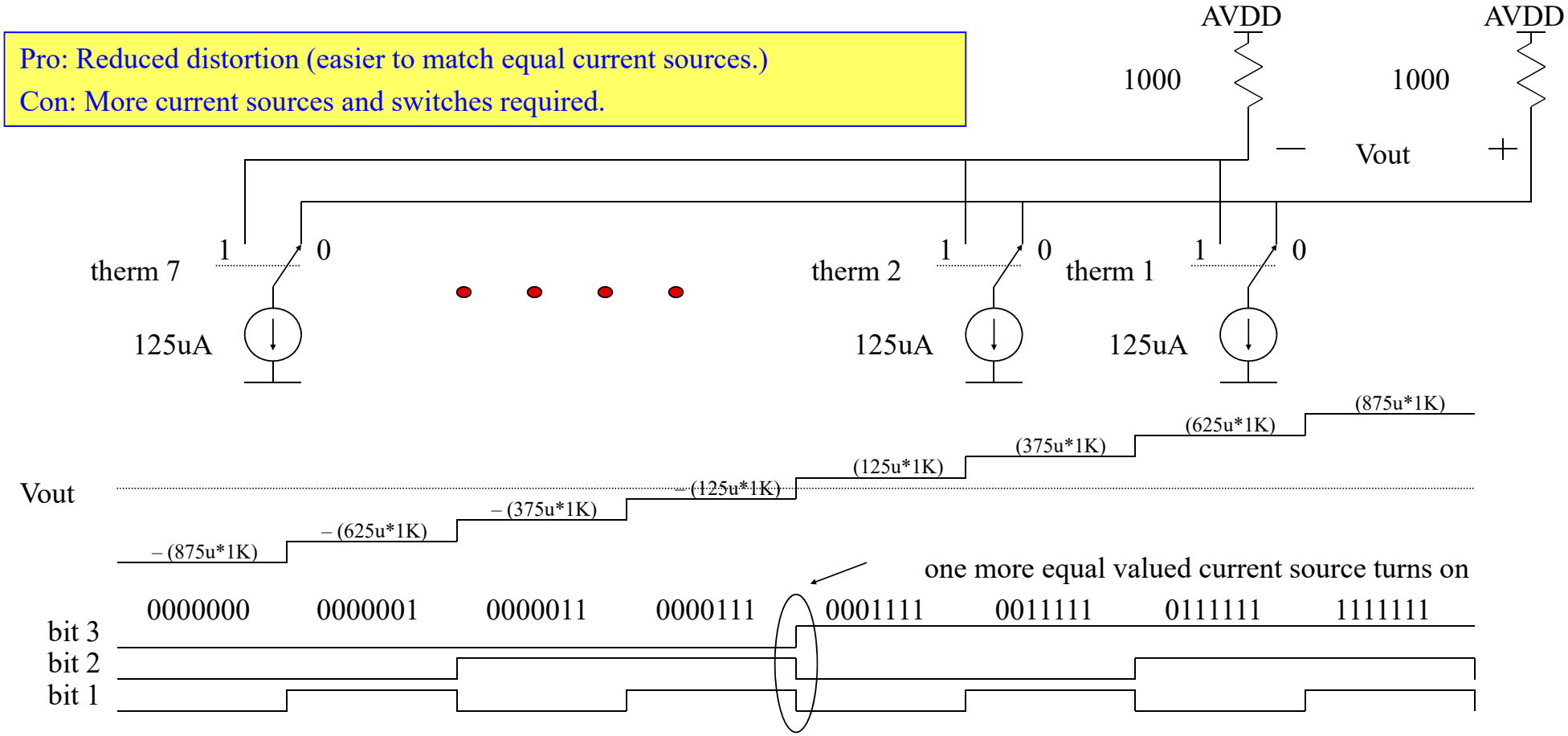
Simple 3-bit Binary DAC

Pro: Least number of current sources and switches.
Con: Higher distortion.

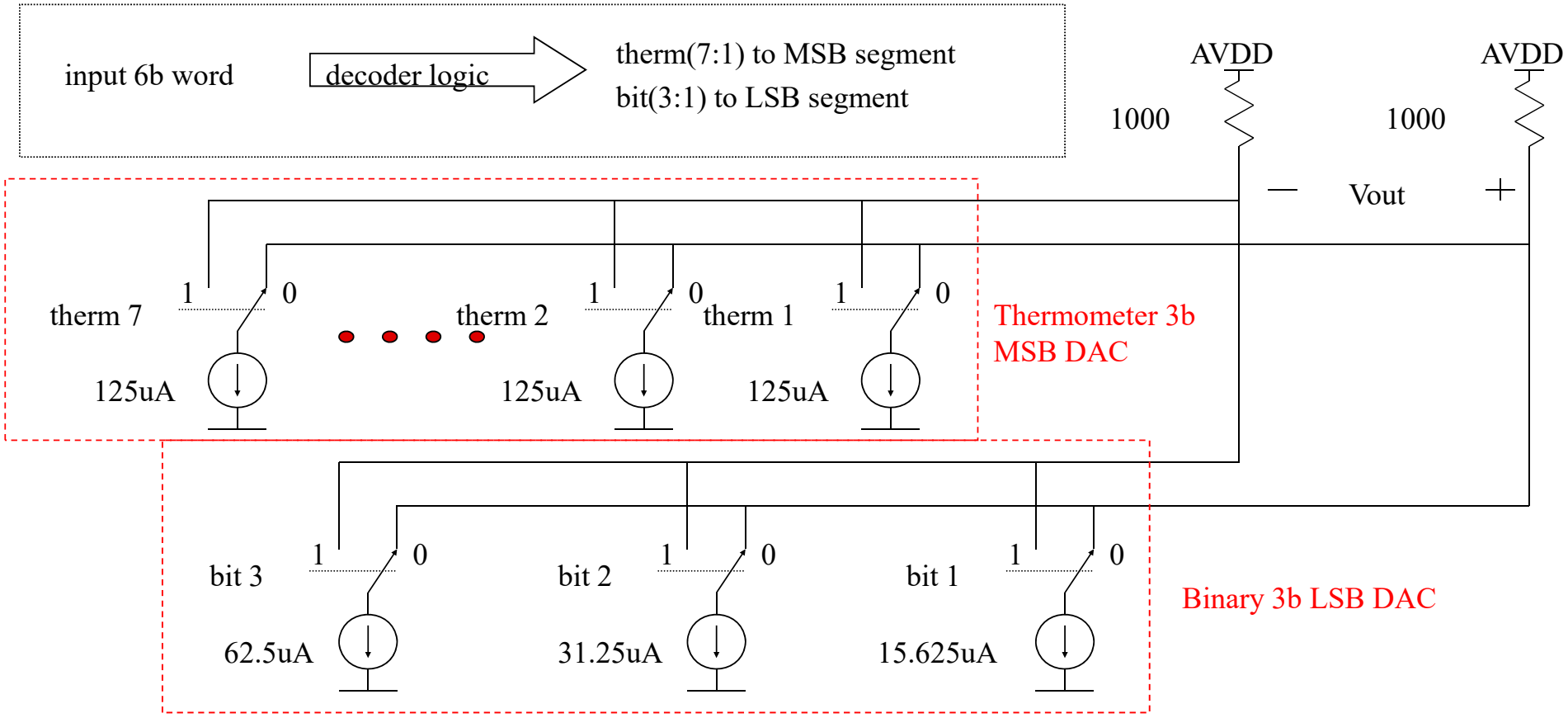


Equivalent 3-bit Thermometer Coded DAC

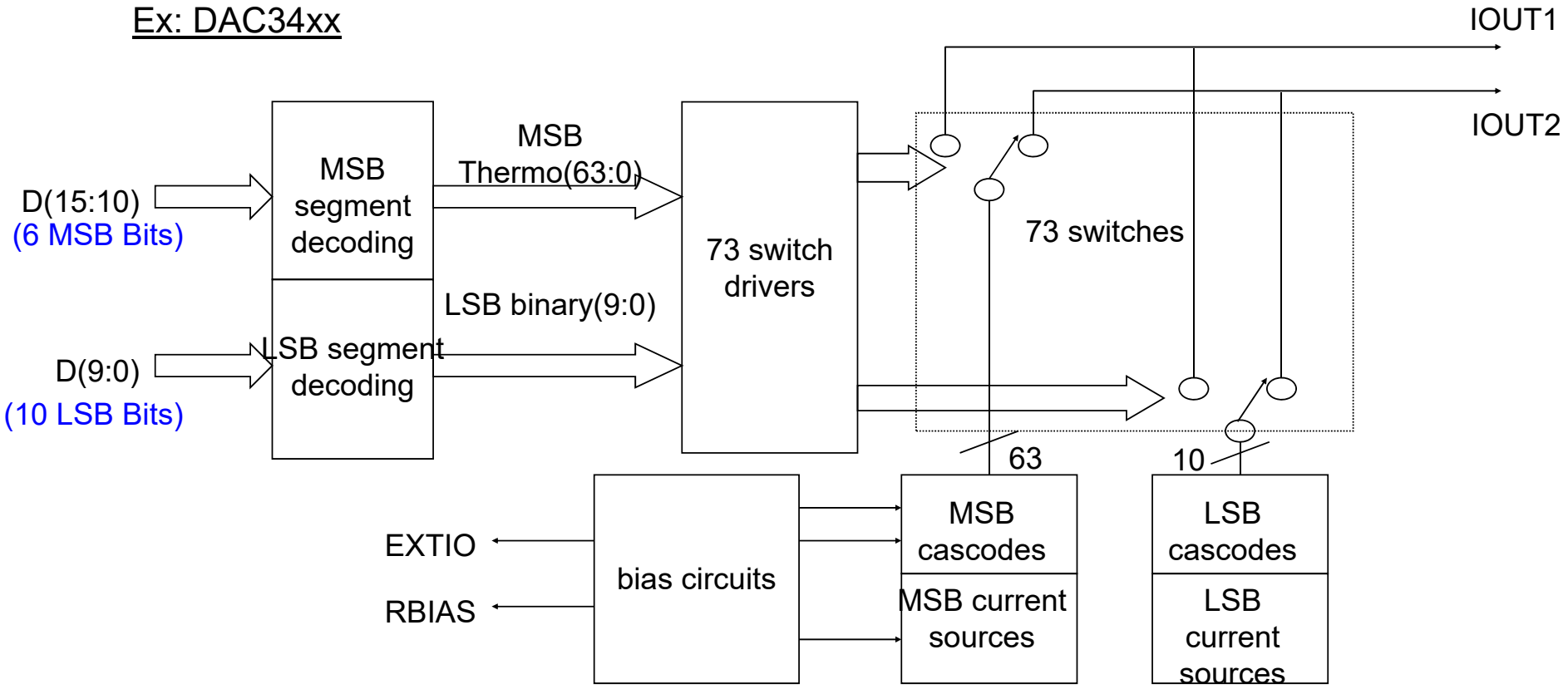
Pro: Reduced distortion (easier to match equal current sources.)
Con: More current sources and switches required.



DACs can be segmented and mixed coded



Simplified TI 16b DAC topology



Thanks for your time!