Tips and Tricks for Successful Power Designs

Part 1: EMI/EMC
Part 2: Optimizing Efficiency
Agenda: Part 1 – EMI/EMC

• EMI/EMC – Definition & Standards

• EMI analysis of various power stages

• Ways to mitigate using PCB Layout

• EMI in AC/DC Converters

• EMI Analysis
Key Learnings

• EMI and the standards

• Root cause of EMI created by ALL Switched Mode Power Supplies

• PCB and Ground Techniques to Mitigate EMI

• Noise Sources in a Real Schematic

• Measurement of EMI
**What is EMI & EMC?**

**EMI**
(Electromagnetic Interference)

Unwanted coupling of signals from one circuit to another, or to system

**Conducted EMI:**
coupling via conduction through parasitic impedances, power and ground connections

**Radiated EMI:**
unwanted coupling of signals via radio transmission

**EMC**
(Electromagnetic Compatibility)

An electrical systems ability to perform its specified functions in the presence of EMI generated either internally or externally by other systems.
EMI/EMC Standards

- EMC Standards vary by:
  - Region
    - US = FCC
    - Europe = CISPR = EN
  - Application usage
    - Consumer
    - Medical
    - Automotive
  - What standards do we use
    - FCC part 15 B
    - CISPR 22 = EN 55022
Conducted vs. Radiated Emission Limits

**Conducted**

FCC/CISPR Conducted Emission Limits

- FCC and CISPR standards the same

**Radiated**

FCC/CISPR Radiated Emission Limits (measured at 10m)

- FCC and CISPR standards somewhat different
- FCC B (consumer) much more stringent than FCC A (commercial, industrial, and business)
Compliance Tests for DC Converters

- There are no specified EMC limits for DC converters
  - EMC requirements are for complete systems measured on AC lines (and signal lines)
  - DC converter is a subcomponent

- Pre-compliance testing can be performed to determine if EMI issues might exist
  - Use limit curves from FCC Part 15 B/CISPR 22/EN55022
  - Use same test set up and LISN as AC mains testing
  - Use same average, quasi-peak, peak measurement methods

- Exception is Power over Ethernet (PoE)
  - DC input power is on CAT-5 ethernet cable which also is system (signal) cable
  - EMC requirements usually apply to this cable
  - EMC specifications and testing the same as AC lines
  - Special TLISN required to measure 8 wires inside CAT-5 cable (no shield or ground connections)
Understanding EMI log scale

• Define dB\(\mu\)V:

\[
V_{dB\mu V} = 20 \log \left( \frac{V}{10^{-6}} \right)
\]

– Ex: 500\(\mu\)V = 54dB\(\mu\)V; 2000\(\mu\)V = 66dB\(\mu\)V

Noise voltage ratio is 4. → Only 12dB\(\mu\)V difference in dB\(\mu\)V scale!

Be careful! Small difference in dB\(\mu\)V could refer to large difference in \(\mu\)V!
How does Noise show up in the System?

**NOISE SOURCE**
*Emissions !!!*

**ENERGY COUPLING MECHANISM**
- **Conducted**
  - Low Frequency
- **Electric Fields**
  - Low, Mid Frequency, LC Resonance
- **Magnetic Fields**
- **Radiated**
  - High Frequency

**SUSCEPTIBLE SYSTEM**
*Immunity*
Field Apps Engineering Approach to mitigate EMI

identify significant EMI Sources

figure out EMI Coupling Paths

engineer Circuit Layout to mitigate EMI

add EMI Filter / Snubber / Shielding

NOISE SOURCE
Unwanted Emissions

ENERGY COUPLING MECHANISM

Conducted Electric Fields
Magnetic Fields
Radiated

EMI Filters

SUSCEPTIBLE SYSTEM

EMI Filters

Shielding

Shielding

Snubber

EMI Filter / Shielding
SMPS is Big Generator of Radiated and Conducted Emissions

• Due to
  – High power
  – High di/dt on the switches and diodes
  – Fast transients (voltage and current)
  – Not generally enclosed (not shielded)
  – Parasitic inductance and capacitance in current paths

• Causing
  – **Noise** Conducted to Supply and / or Load
  – **Interfere** with circuits in the same system
  – **Interfere** with other systems
EMI to be considered for a SMPS

- Conduction emission issue:
  - Solve by EMI filter.

- Near-field radiation emission issue:
  - Solve by better PCB layout and component placement.

- Far-field radiation emission issue:
  - Not focused on in this presentation
Identify Critical Path

Buck Converter

Boost Converter

Buck-Boost Converter

Switching Current exist in the input side

Critical path
Identify Critical Path

Buck Converter

Boost Converter

Buck-Boost Converter

Critical path
Identify Critical Path

Buck Converter

Boost Converter

Buck-Boost Converter

Critical path

Non-Inverting

Inverting
What can we do in PCB Layout? → Buck Example

- Minimize critical path area
- Separate noisy ground path from quiet ground
Identify Critical Paths in Isolated Converters

Flyback Converter

Forward Converter

Push-Pull Converter

Half Bridge Converter

Full Bridge Converter

Critical paths
Identify Critical Paths in Isolated Converters

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HALF-BRIDGE

Critical paths
Identify Critical Paths in Isolated Converters

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Full Bridge Converter

FULL-BRIDGE

Critical paths

Vin

Q1

Q2

D1

L

Q3

Q4

Cin

NS1

NS2

Np

Vout

C0

D2
EMI Mitigation by PCB Layout

**Critical Path Area Reduction**

- BUCK Example

![Diode Circuit Diagram]

- Bypass Caps in High di/dt loop should be placed as close as possible to the switching components.
- Low side FET SOURCE should be connected as close as possible to the input capacitor.
- Apply to critical paths in other SMPS topologies.

**Grounding**
Lower EMI can be achieved by…

- Place capacitors on same side of board as component being decoupled
- Locate as close to pin as possible
- Keep trace width thick and minimized

Connecting to decoupling capacitors

Connecting to output capacitors
EMI Mitigation by PCB Layout

Critical Path Area Reduction

- Switch node SW swings from $V_{IN}$ or $V_{OUT}$ to ground at $F_{sw}$.
  - very high $dv/dt$ node! = electrostatic radiator!

- Requires a contradiction:
  - As large as possible for current handling,
  - yet as small as possible for electrical noise reasons

- Solutions:
  - Switch node short and wide
  - Minimum Copper Width Requirement:
    - Roughly 30mils/Amp for 1 Oz Cu and 60 mils/Amp for ½ Oz Cu
Contradiction on SW node transition rate:

- Faster Rising and Falling Times
  - Less Losses
  - Higher EMI

Resistor Value:

Start with 1-10 ohms and adjust from there.
EMI Mitigation by PCB Layout

Critical Path Loop Reduction

- Ground Plane
  - Return Current takes the least IMPEDANCE path
  - Unbroken Ground Plane provides shortest return path – image current return path:

Grounding

Current flow in top layer trace

Return current path in unbroken ground plane directly under path:
Area minimized & B field minimized

Trace or Cut on the ground plane

Return current path enclose much larger area if the direct path is blocked!
Conduction EMI – Common mode noise

Key parameters:
1. $C_{ps}$
2. $V_{ps}$

CM EMI model
Conduction EMI – Differential mode noise

Key parameters:
1. ESL of Cbus.
2. EPC of L, L_{pfc}.
3. V_{ds} dV/dt.
The Usual Suspects - Noise Sources

Input Ripple Current

Inter-winding Capacitance

Stray Capacitance from High DV/DT Surfaces to the Outside World
Conduction EMI – Lower transformer $C_{PS}$

Target: lower CPS to reduce CM noise.
Possible actions:
1. Increase the distance between primary and secondary.
   • Side effect: larger leakage and larger losses.
2. Decrease the facing area between primary and secondary.
   • Side effect: larger leakage and larger losses.
   • Side effect: increase cost and need more space.
4. Suitable terminal connection: easy and a must do!
Conduction EMI – Better transformer winding

Original design

 Better design

Hot-voltage Terminal

EMI Filter

Original design

 Better design
Typical Mitigation Techniques

- **Common-mode Choke**: To reduce Common-Mode Noise
- **Y-Cap**: To reduce Common-Mode Noise
- **Filtering for Differential-mode Noise**: Techniques for reducing noise in differential signals
- **Shielding Techniques Inside Transformer**: Methods to provide electromagnetic protection
- **Snubber**: To reduce ringing effects in the circuit

**Input**: 85VAC-265VAC

**Output**: 13.5V/0.9A
Rectifier Location in Flyback Converter

- Rectifier in return lead of transformer
- CIN/CEMI/COUT couple dot end of primary and non-dot end of secondary to 0 Vac
- Maximum voltage potential between windings
- AC current flows in transformer capacitance, resulting in common mode current flow and EMI issues
Rectifier Location in Flyback Converter

- Rectifier in positive lead of transformer
- CIN/CEMI/COUT couple dot end of primary and dot end of secondary to 0 Vac
- No voltage potential between windings
- No AC current flows in transformer capacitance, no common mode currents, less EMI
Conducted EMI Test Setup
Compliance Test Procedure

- Start with Peak Detector measurement
- If Peak measurement is below AVG and QP, no need for further testing
- Only test AVG and QP at frequencies where Peak measurement is above AVG/QP limits
Compliance Testing Data Example

National Technical Systems, Plano TX
CISPR Class B Conducted Emissions
CISPR Pre-Scan Neutral 150kHz - 30MHz

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>QP Limit dBuV</th>
<th>AVE Limit dBuV</th>
<th>AVE Readings dBuV</th>
<th>AVE Margin dB</th>
<th>OP Readings OP Margin dB</th>
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<tbody>
<tr>
<td>8.927</td>
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<td>9.029</td>
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<td>50.000</td>
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<td>56.798</td>
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</table>

CISPR Class B 0.150-30MHz
EUT On / PEM9204
Testing On 120VAC/60Hz

Just Barely Failed
### What Scan to Use for Testing PMP Boards?

<table>
<thead>
<tr>
<th>Scan Type</th>
<th>Time Per Scan</th>
<th>Time for Complete Set of Scans</th>
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<tbody>
<tr>
<td>Average Detector</td>
<td>~1 hour</td>
<td>4-5 hours</td>
</tr>
<tr>
<td>Quasi-Peak Detector</td>
<td>1-2 hours</td>
<td>6-8 hours</td>
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<tr>
<td>Peak Detector</td>
<td>&lt;1 minute</td>
<td>5 minutes</td>
</tr>
<tr>
<td>Peak Detector Max-Hold</td>
<td>1-5 minutes</td>
<td>10-20 minutes</td>
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