SAR ADC’s vs. Delta-Sigma ADC’s:
Different Architectures for Different Applications
# Common ADC Topologies

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<th>Data Rate</th>
<th>Resolution</th>
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<td>≤ 5 MSPS</td>
<td>≤ 20-bit</td>
<td>• Easy to Use • Zero Latency • Low Power</td>
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Common ADC Topologies

- **Pipeline**
  - Advantages
    - Low Latency-time
  - Disadvantages
    - Max $F_{SAMP}$ of 2-5Mhz

- **SAR**
  - Advantages
    - Low Latency-time
    - High Accuracy
    - Typically Low Power
    - Easy to Use
  - Disadvantages
    - Max $F_{SAMP}$ of 2-5Mhz

- **Delta-Sigma**
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Delta-Sigma (∆Σ):  
| ADC0x/1x      | ≤ 10 MSPS  | ≤ 32-bit   | • High Resolution              |
| ADS12xxx      |            |            | • High Integration             |
| ADS13xxx      |            |            |                                |
| ADS16xx       |            |            |                                |

Pipeline:  
| ADC3xxx      | ≤ 1000 MSPS| ≤ 16-bit   | • Higher Speed                 |
| ADS5xxx      |            |            | • Higher Power                 |
Common ADC Topologies

Delta-Sigma Architecture

**Advantages**
- High Resolution
- Low Noise
- High Stability
- High Integration

**Disadvantages**
- Cycle-Latency

- **Delta-Sigma**
  - ~

- **SAR**
- **Pipeline**

**Converter Resolution (bits)**

**Conversion Rate (SPS)**

- 10
- 100
- 1K
- 10K
- 100K
- 1M
- 10M
- 100M
- 1G
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ADC Technologies

Converter Resolution (bits) vs Conversion Rate (SPS)

- **Delta-Sigma**:
  - Advantages: Higher Bandwidth
  - Disadvantages: Lower Resolution

- **SAR**: Pipeline Delay/Latency

- **Pipeline**: Higher Power

**Pipeline Architecture**
- Advantages: Higher Speeds
- Disadvantages: Pipeline Delay/Latency
SAR ADC takes “snapshots”
Each conversion command captures the signal level, at that point in time, onto the sample/hold

ΔΣ ADC calculates an average
The signal is sampled continuously
## SAR vs. Delta-Sigma

How does the ADC control happen?

- SAR conversions have Start Conversion Signal
- Delta-Sigma’s are always sampling/converting

<table>
<thead>
<tr>
<th>SAR Converter</th>
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<th></th>
<th></th>
</tr>
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<tbody>
<tr>
<td>Start Conversion</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Conversion Done</td>
<td></td>
<td></td>
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<th>Delta-Sigma Converter</th>
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<tr>
<td>Input Sampling</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Conversion Done</td>
<td></td>
<td></td>
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How Does a SAR ADC Work?

- Similar to a balance scale
How Does a SAR ADC Work?

• Similar to a balance scale
How Does a SAR ADC Work?

- Similar to a balance scale
How Does a SAR ADC Work?

- Similar to a balance scale

The MSB is determined first
How Does a SAR ADC Work?

- Similar to a balance scale

The test is repeated for each Binary weighted bit
How Does a SAR ADC Work?

• Similar to a balance scale

The LSB is determined last

MSB: 1
Mid: 0
LSB: 1

$\frac{1}{2}$
Typical Topology of a SAR ADC

![Diagram of SAR ADC topology]
SAR ADC Acquisition Phase

- **V_IN**
- **SAMPLE & HOLD**
- **COMPARATOR**
- **DAC**
- **SAR**
- **S1**
- **S2**
- **C**
- **N-bit Search DAC**
- **Data Register**
SAR ADC Acquisition Phase

![Diagram of SAR ADC Acquisition Phase](image)

- **V**
- **SH0**
- **VIN**
- **t**
- **AQ Time**
- **1/2 LSB**
- **VCSH(t)**
- **t0**
- **tAQ**

**Key Components:**

- **SAMPLE & HOLD**
- **DAC**
- **COMPARATOR**
- **V**
- **IN**
- **DAC**
- **S1**
- **S2**
- **C**
- **SAR**
- **Data Register**
- **N-bit Search DAC**

**Graph:**

- **V**
- **IN**
- **VCSH(t)**
- **VSH0**
- **1/2 LSB**
- **t0**
- **tAQ**

**Time Axis:**

- **Time**
SAR ADC Acquisition Phase

\[ V_{CSH}(t) = V_{CSH}(t_0) + (V_{IN} - V_{CSH}(t_0)) \times (1 - e^{-\frac{t}{\tau}}) \]

\[ \tau = R_{S1} \times C_{SH} \]
SAR ADC Conversion Phase

Time

Digital Output Code = 10100

DAC Output

V_{DAC}

0

1/4FS

1/2FS

3/4FS

FS

Bit = 0

Bit = 1

Bit = 1

Bit = 0

Bit = 0

Bit = 0

Bit = 1

Bit = 0

Bit = 0

Bit = 0

TEST MSB

TEST MSB -1

TEST MSB -2

TEST MSB -3

TEST LSB

Analog Input

FS

1/4FS

1/2FS

3/4FS

V

DAC

Digital Output Code = 10100
SAR ADCs

• Very Popular Topology
• Attractive in “Point in Time” or Multiplexed Measurements
• Advantages
  – “no latency”
    • input is sampled once
    • “balancing” done internally
  – good tradeoff between speed, resolution and power
• Speed: DC to 5 MSPS
• Resolution: 8 to 20 bits
• TI Part Numbers:
  – ADC0x/1x
  – ADS7xxx
  – ADS8xxx
  – ADS9xxx
Delta-Sigma Topology

Delta-Sigma Modulator

Analog Input

Digital Filter

Decimator

Digital Decimating Filter

Digital Output
Delta-Sigma Topology

SAMPLING RATE (F_s)

Analog Input

(Samples at High Frequency)

Delta-Sigma Modulator

Digital Filter

Decimator

Digital Decimating Filter

High frequency, 1 bit PCM data stream

Digital Output

(2)
Delta-Sigma Topology

**Delta-Sigma Modulator**

- Analog Input
- Input Oversampling

**Digital Filter**

- Digital Decimating Filter

**Decimator**

- High frequency, 1 bit PCM data stream
- Lower data rate, very high resolution digital output

**Sampling Rate ( Fs )**

**Data Rate ( Fd )**

- Lower data rate, very high resolution digital output
Oversampling

Ideal N-Bit ADC
SNR = 6.02 N + 1.76 dB

Average Noise energy distributed from DC to fs/2

Input Signal

Average Noise Floor

Power

DC

fs/2

fs

26
Oversampling

On a Delta-Sigma Converter, the analog input is sampled at a Frequency much higher than the Nyquist rate.

- Average Noise energy distributed from DC to fs/2
- Average Noise energy distributed over a wider range from DC to K fs/2

Ideal N-Bit ADC

\[
\text{SNR} = 6.02N + 1.76 \, \text{dB}
\]

\[
\text{SNR} = 6.02N + 1.76 \, \text{dB} + 10 \log (\text{OSR})
\]

Digital Low Pass filter

Power

Average Noise Floor

Average Noise energy distributed from DC to fs/2

Average Noise energy distributed over a wider range from DC to K fs/2

– On a Delta-Sigma Converter, the analog input is sampled at a Frequency much higher than the Nyquist rate
Delta Sigma Modulator

Analog Input ↔ Delta-Sigma Modulator

Digital Filter

Digital Decimating Filter (usually implemented as a single unit)

Decimator

Digital Output
First Order Delta-Sigma Modulator \(^{(1)}\)

Noise Shaping

\[
A(f) = \frac{1}{f}
\]

\[
\sum \left[ X_i + \sum e_i \right] - \sum Y_i
\]

1-Bit ADC

1-Bit Quantization Noise

Input Signal \(X_i\)
First Order Delta-Sigma Modulator

Noise Shaping

\[ Y = (X - Y) A(f) + e(n) \]  \hspace{2cm} (1)

\[ Y = e(n) \left( \frac{f}{1+f} \right) + X \left( \frac{1}{1+f} \right) \]  \hspace{2cm} (2)
First Order Delta-Sigma Modulator

Noise Shaping

\[ Y = (X - Y) A(f) + e(n) \]  
\[ Y = e(n) \left( \frac{f}{1 + f} \right) + X \left( \frac{1}{1 + f} \right) \]
First Order Delta-Sigma Modulator (4)

Noise Shaping

Modulator Output:
TIME DOMAIN

Believe it or not, the sine wave is in there!
(drawing is approximate)
First Order Delta-Sigma Modulator
Noise Shaping

Modulator Output:
TIME DOMAIN

Believe it or not, the sine wave is in there!
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First Order Delta-Sigma Modulator

Noise Shaping

Modulator Output:
TIME DOMAIN

Believe it or not, the sine wave is in there!
(drawing is approximate)

Modulator Output:
FREQUENCY DOMAIN

Signal

Quantization Noise

SIGNAL

Fs
Higher Order Delta-Sigma Modulators

- First Order \( \Delta \Sigma \) Modulator
- Second Order \( \Delta \Sigma \) Modulator
- Third Order \( \Delta \Sigma \) Modulator

Frequency vs. \( F_S \)
Delta-Sigma A/D Signal Path

Delta-Sigma Modulator

Digital Filter

Decimator

Digital Decimating Filter
(usually implemented as a single unit)
Modulator Noise Shaping and Digital Filter

\[ \Delta \Sigma \text{ Modulator Noise Shaping} \]
Modulator Noise Shaping and Digital Filter (2)
Modulator Noise Shaping and Digital Filter

Filter set by Oversampling Ratio

$\Delta \Sigma$ Modulator Noise Shaping

Frequency $F_S$
Digital Filter

- Digital filter architecture determines overall ADC response.
- Common filters: “Sinc” and “Flat Passband”
Sinc Digital Filter

- Typically used for DC measurements, or slow moving signals

**Advantages**
- Economical silicon area, easy to implement
  - Low cost
  - Low power
- Low latency
- Filter notches can target specific frequencies (ex. 50/60 Hz)

**Disadvantages**
- Pass band signal droop
- Weak Stop band attenuation for low-order Sinc filters
Settling time for an input step change, Sinc³ filter
Need n cycles to settle for a Sincⁿ filter
Delta-Sigma: Zero Cycle Latency

- Zero cycle Latency =
  - Zero latency
  - Single cycle conversion
  - Single cycle settling
  - No Latency
Delta-Sigma: Zero Cycle Latency

- Zero cycle Latency =
  - Zero cycle latency
  - Single cycle conversion
  - Single cycle settling
  - No Latency

Analog IN

Data OUT

"Hidden Conversions"
Flat Pass Band Filter

Advantages

• Frequency Response
  • Very low ripple pass band
  • Sharp Nyquist transition band
  • Large stopband attenuation: lower than -100dB (simplify aliasing requirement)
• Frequency response scalable with master clock

Disadvantages

• Large area – Costly
• Higher-order / high-tap filter – large latency
Delta-Sigma: Flat Passband Digital Filter Settling

- The latency of the filter depends on the number of delay blocks used.
- Flat Passband filters require a lot of delay blocks to maintain desired AC response.
- Many Delta-Sigma Converters incorporate filters with programmable settings:
  - Optimize for lower latency, power consumption, or for AC performance/higher resolution.

![FIR filter block topology diagram](image-url)
ΔΣ ADCs: Simplifying the Signal Chain

Sensor

Passive Network + Protection
Passive Network + Protection

Gain Stage

Signal Conditioning and Protection

In
R1
R2
Out

MUX

ADC Drive Circuitry

ADC Drive

ADC

ADC

Processor

Iso

MCU
ΔΣ ADCs: Simplifying the Signal Chain (2)

Delta-Sigma ADCs integrate many signal chain elements into one device
Delta-Sigma ADCs

- Useful for Lower Bandwidth Signals
- Very High Resolution
- Very High Linearity
- Incorporate a Digital Filter
- Frequency Response, and Latency dependent on Digital Filter
- Very Low Power
- Typically Highly Integrated devices:
  - Digital Filter, Buffer, PGA, MUX, Vref, Calibration/diagnostics
- Simple Anti-Aliasing Filter
- Typically Requires Configuration of Registers
SAR ADCs

• Very Popular Topology
• Attractive in “Point in Time” or Multiplexed Measurements
• Advantages
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Input Driver Circuit for SAR ADC

**HIGH GBW**

Faster load transient response

$C_F$ is an ideal source to high frequency transients
Isolation Resistor
Stabilizes op amp by isolating it from the capacitive load.
In addition, the RC network slows the load transient seen by the op amp and provides noise and anti-aliasing filtering.
Fully Differential ADC Inputs

THS4551 Based Single-Ended Input to Differential Output with Multiple Feedback Filter Interface to the 24-bit, 512 kSPS ADS127L01 Delta-Sigma ADC
THS4551 Fully Differential ADC Driver

Popular Texas Instruments ADC Families Supported by the THS4551

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<th>Device</th>
<th>Architecture</th>
<th>Resolution</th>
<th>Speed</th>
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<td>ADS127L01</td>
<td>ΔΣ</td>
<td>24-bit</td>
<td>512 kSPS</td>
</tr>
<tr>
<td>ADS8900B</td>
<td>SAR</td>
<td>20-bit</td>
<td>1 MSPS</td>
</tr>
<tr>
<td>ADS8910B</td>
<td>SAR</td>
<td>18-bit</td>
<td>1 MSPS</td>
</tr>
<tr>
<td>ADS9110</td>
<td>SAR</td>
<td>18-bit</td>
<td>2 MSPS</td>
</tr>
<tr>
<td>ADC3241</td>
<td>Pipeline</td>
<td>14-bit</td>
<td>25 MSPS</td>
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More Analog Signal Chain Information

Precision ADC Web Page: www.ti.com/precisionadc

Fully Differential Amplifier Web Page: www.ti.com/fda
  • Data Sheets & Technical Reference Manuals
  • Application Notes
  • Software, Tools & SPICE Model Downloads
  • Order Evaluation & Performance Demonstration Kits

Precision ADC E2E™ Support Forum: www.ti.com/precisionadcsupport
  • Ask Technical Questions
  • Search for Technical Content

Precision HUB Blog Series: e2e.ti.com/blogs_/b/precisionhub
  Tips, tricks and techniques from TI precision analog experts

TI Designs - Precision: www.ti.com/precisiondesigns
  • Reference Designs
  • Board Schematics & Verification Results
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- Vinay Agarwal – SAR ADC