DCDC Power Solutions for FPGAs and Data Converters

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LPDCDC
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Abstract

With the increasing complexity of industrial systems, such as factory automation, more powerful controllers are required. FPGAs and precision data converters are widely used to handle and coordinate the diverse set of tasks required. These devices have tight power supply requirements which needs to be addressed. In this session we will discuss the key power requirements of such industrial systems and compare different solutions with our newest industrial switching power supplies. To help getting started, the technical aspects of various reference designs are discussed.
Agenda

• FPGA Power Considerations
  ➢ Estimating Current Requirements
  ➢ System Architecture
  ➢ FPGA Rail Requirements
  ➢ Sequencing
  ➢ Example Calculation with TPS62135

• Powering ADC/Data Converter

• Q&A
Typical FPGA Supply Rails

Intermediate Rail (3.3V, 5V, 12V)

DC/DC → 1.2V
DC/DC → 2.5V
DC/DC → 1.5V-3.3V
DC/DC → 1.2V

Core
Analog
I/O
AUX

Current Requirements?
Estimating Current Requirements:

- WEBENCH® FPGA Power Architect
  - Load current shown is a starting point
  - Load current may vary with clock speed and specific usage

- Use FPGA vendor provided power estimator tool for more accurate calculation

Vendor spreadsheets calculates the currents
Typical System Architectures

<table>
<thead>
<tr>
<th>Intermediate Rail</th>
<th>Advantage</th>
<th>Disadvantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>12V</td>
<td>Lower input current</td>
<td>Lower efficiency conversion to POL Possible duty cycle limitation</td>
</tr>
<tr>
<td>5V</td>
<td>Higher efficiency conversion to POL</td>
<td>Higher input current compared to 12V</td>
</tr>
<tr>
<td>3.3V</td>
<td>Higher efficiency conversion to POL</td>
<td>Highest input current Fewest available parts (min Vin)</td>
</tr>
</tbody>
</table>
# Typical FPGA Rail Requirements

<table>
<thead>
<tr>
<th>Rail Requirement</th>
<th>Core</th>
<th>Analog</th>
<th>I/O</th>
<th>AUX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td>1.2V</td>
<td>2.5V</td>
<td>1.5V - 3.3V</td>
<td>1.2</td>
</tr>
<tr>
<td>Tolerance</td>
<td>3% / 5%</td>
<td>5%</td>
<td>5%</td>
<td>5%</td>
</tr>
<tr>
<td>Transient (typical)</td>
<td>50% load ≥ 1A/us</td>
<td>50% load ≥ 1A/us</td>
<td>50% load ≥ 1A/us</td>
<td>50% load ≥ 1A/us</td>
</tr>
<tr>
<td>Sequencing Order</td>
<td>1&lt;sup&gt;st&lt;/sup&gt;</td>
<td>2&lt;sup&gt;nd&lt;/sup&gt;</td>
<td>2&lt;sup&gt;nd&lt;/sup&gt;</td>
<td>3&lt;sup&gt;rd&lt;/sup&gt;</td>
</tr>
</tbody>
</table>

Example: Altera MAX 10 FPGA
Output Voltage Tolerance

Power supply performance is considered under two operating conditions:

- **Static**: Fixed/gradual changes (DC)
- **Dynamic**: Quick changes (AC)
Static: Output voltage accuracy (DC)

Influencing Parameters:

- Feedback voltage accuracy $V_{fb}$
- Feedback divider tolerance
- Load regulation
- Line regulation (if $Vin$ varies over a wide range)

| $V_{OUT}$ | Load regulation | $V_{OUT} = 3.3\,\text{V}$  
PWM mode operation | 0.05 % | / A |
| --- | --- | --- | --- | --- |
| $V_{OUT}$ | Line regulation | $3V \leq V_{IN} \leq 17\,\text{V}, \, V_{OUT} = 3.3\,\text{V}, \, I_{OUT} = 1000\,\text{mA}$  
PWM mode operation | 0.02 % | / V |
1. Output voltage accuracy in percent:

\[
\frac{\Delta V_{\text{out}}}{V_{\text{out}}} = \pm 2 \cdot T_R \cdot \left(1 - \frac{V_{\text{fb}}}{V_{\text{out}}} \right) + T_{V_{\text{fb}}}
\]

- $T_R$ = Tolerance of Resistors in %
- $T_{V_{\text{fb}}}$ = Tolerance of Feedback Voltage in %
- $V_{\text{fb}}$ = Reference Voltage of IC
- $V_{\text{out}}$ = Set output voltage

2. The line and load regulation needs to be added in addition.

### Static: Examples for a 1.8V output

\[
\frac{\Delta V_{\text{out}}}{V_{\text{out}}} = \pm 2 \cdot T_R \cdot \left(1 - \frac{V_{\text{fb}}}{V_{\text{out}}}\right) + T_{V_{\text{fb}}}
\]

- \(T_R = \text{Tolerance of Resistors in \%}\)
- \(T_{V_{\text{fb}}} = \text{Tolerance of Feedback Voltage in \%}\)
- \(V_{\text{ref}} = \text{Reference Voltage of IC}\)
- \(V_{\text{out}} = \text{Set output voltage}\)

<table>
<thead>
<tr>
<th></th>
<th>Example 1</th>
<th>Example 2</th>
<th>Example 3</th>
<th>Example 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>(T_R)</td>
<td>1%</td>
<td>0.1%</td>
<td>1%</td>
<td>0.1%</td>
</tr>
<tr>
<td>(T_{V_{\text{fb}}})</td>
<td>2%</td>
<td>2%</td>
<td>2%</td>
<td>1%</td>
</tr>
<tr>
<td>(V_{\text{fb}})</td>
<td>0.8V</td>
<td>0.8V</td>
<td>0.7V</td>
<td>0.8V</td>
</tr>
<tr>
<td>(V_{\text{out}})</td>
<td>1.8V</td>
<td>1.8V</td>
<td>1.2V</td>
<td>1.8V</td>
</tr>
<tr>
<td>Error</td>
<td>3.1%</td>
<td>2.1%</td>
<td>2.83%</td>
<td>1.1%</td>
</tr>
</tbody>
</table>

Highest Margin for load regulation and AC tolerance
Static: Minimizing DC Loss

DC loss is the voltage drop due to board impedance
- Can be reduced by:
  • Remote Sense
  • Wide/thick copper traces
  • Place power supply near FPGA
Static: Measuring Output Voltage

**Bad**
- The alligator clip and GND wire of the scope probe will form a loop antenna and pick up radiated noise.

**Good**
- Wrapping a GND wire around the barrel of the scope probe will minimize the loop area of the antenna and greatly reduce noise pickup.
Dynamic: Output voltage accuracy (AC)

Influencing Parameters:

- Load Transient:
  - Slope (A/us)
  - Step size (A)
  - Converter Topology
    - Voltage Mode
    - Current Mode
    - Hysteric
    - DCS Control
  - Output Filter
Dynamic: Transient Droop

- Transient Droop is affected by:
  - Load step size (A)
  - Load step speed (A/µs)
  - Output capacitance

- Capacitor Model

- Capacitor Model
Dynamic: Output Capacitor Network

• Minimizing Transient Voltage Droop

Complete and effective decoupling network
Ceramic X5R and X7R dielectrics are great choices
Sequencing

- **Requirements**
  - Monotonic
  - Ramp-up Time
  - Sequencing Series
    - Power Up
    - Power Down

- **Techniques**
  - R/C Sequencing
    - Power Up Only
  - Power Good drives EN
    - Power Up Only
  - Sequencing Controller
    - Power Up/Down
Sequencing Up & Down

- Sequencing down not always required but strongly recommended
- LM3880
  - Sequence Up (1-2-3)
  - Sequence down in reverse order (3-2-1)
  - Built in delay
  - Open drain outputs
  - Daisy chain for more rails

![Diagram of LM3880](image)
Recommended Design Steps

1. Use Vendor FPGA Power Estimator Tools
   - Altera
   - Xilinx

2. Check TI Reference Designs
   - Altera
   - Xilinx

3. Use WEBENCH® FPGA Power Architect
   - FPGA Architect
TPS62135
3-17Vin, 4.0A Buck Converter in 3x2 QFN (HotRod) package

**Features**
- **V\text{OUT}** range: 0.8V to 12V
- ±1% feedback voltage accuracy over -40 to +125 $^\circ$C
- Forced-PWM option with 2.5MHz Fsw
- Supports high output capacitance
- Output Voltage Select
- Adjustable Softstart & Tracking
- 100% duty cycle operation
- 18µA quiescent current
- Power Good, Output Discharge
- HICCUP current protection
- 2mm x 3mm HotRod™ QFN package

**Benefits**
- VSEL pin allows for simple voltage scaling
- Mode pin to allow choose between high efficiency over full load range or lowest output voltage ripple; simplifies design for RF, Signal Chain or Audio applications.
- Small solution of < 60mm$^2$ with high power density (750W/cm$^3$ = 12.3kW/inch$^3$)

**Applications**
- Industrial point of load regulator
- Telecom / datacom
- FPGA Power

![Diagram of TPS62135](image)
Why PWM is important?

DC Accuracy:

<table>
<thead>
<tr>
<th>$V_{FB}$</th>
<th>Feedback Voltage Accuracy (2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN} \geq V_{OUT} +1 , V$</td>
<td>PWM mode</td>
</tr>
<tr>
<td>$V_{IN} \geq V_{OUT} +1 , V$; $V_{OUT} \geq 1.5 , V$</td>
<td>PFM mode; $C_{i}, eff \geq 47 , \mu F, L = 1 , \mu H$</td>
</tr>
<tr>
<td>$1 , V \leq V_{OUT} &lt; 1.5 , V$</td>
<td>PFM mode; $C_{o}, eff \geq 47 , \mu F, L = 1 , \mu H$</td>
</tr>
<tr>
<td>$V_{OUT} &lt; 1 , V$</td>
<td>PFM mode; $C_{o}, eff \geq 75 , \mu F, L = 1 , \mu H$</td>
</tr>
</tbody>
</table>

Load Regulation at light load:

Figure 16. Output Voltage vs Output Current

Figure 17. Output Voltage vs Output Current
TPS62135 Solution size

- Solution size EVM: $<60\text{mm}^2$
- Solution size using 0805 chip inductor and 0402 components: $<40\text{mm}^2$

Cin: 10uF
Cout: 10uF
L: 1uH
Example Calculation for Core supply with TPS62135

Intermediate Rail = 12V

DC/DC

1.2V
4A max

Core
Analog
I/O
AUX
FPGA

<table>
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<th>Rail Requirement</th>
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<tr>
<td>Voltage</td>
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</tr>
<tr>
<td>Tolerance</td>
<td>5%</td>
</tr>
<tr>
<td>Transient (typical)</td>
<td>50% load ≥1A/us</td>
</tr>
<tr>
<td>Sequencing Order</td>
<td>1st</td>
</tr>
</tbody>
</table>
Example Calculation for Core supply with TPS62135

- Step 1: Setting the output voltage to 1.2V using 0.1% resistors.
  
  With \( V_{fb} = 0.7V, \) \( R1 = 130k\Omega, \) \( R2 = 180k\Omega \)
  
  \( \Rightarrow V_{out} = 1.2V \)

- Step 2: Calculating the max error of \( V_{out} \) (DC)
  
  With \( T_R = 0.1\%, \) \( T_{Vfb} = 1\% \)
  
  \( \Rightarrow Error = 1.08\% \)

- Step 3: adding Load Regulation
  
  With 0.05%/A and 4A
  
  \( \Rightarrow Error = 1.08\% + 0.2\% = 1.28\% \) (at full load)
Example Calculation for Core supply with TPS62135

- Max DC Error = 1.28% (at full load)
- This results in 3.72% margin for Load Transient (AC) (5% total)
# Module or Discrete Regulator?

## Module Solution

**Pro**
- Lower total cost of ownership
- Fewer components for procurement
- Less engineering time debugging
- IC, inductor, and passives in module qualified to TI’s standard
- Small solution size

**Con**
- Narrower operating range
- More expensive

![LMZ31710](images/LMZ31710.png)  
**TPS82130**  
3A POL  
**10A POL**

## Discrete Solution

**Pro**
- More design flexibility
- Optimize to your design conditions
- Lower total solution cost
- Spread heat over larger area
- Small size with optimized layout

**Con**
- Requires more design time
- Higher BOM count

![TPS54020](images/TPS54020.png)  
**TPS62130**  
3A POL  
**10A POL**
TPS82130SIL
12V 3A Step Down Converter with Integrated Inductor

Features

- 3.0 x 2.8 x 1.5mm MicroSiP™ package with integrated inductor
- 3V to 17V Input Voltage Range
- DCS-Control™ Topology
- Power Save Mode for Light Load Efficiency
- 100% Duty Cycle
- 20µA Quiescent Current
- Power Good Output plus Capacitor Discharge
- Adjustable Output Voltage
- Programmable Soft Startup
- -40°C to 125°C operating temperature range

Applications

- General Purpose POL
- Data Card
- Network Switcher, Line Cards
- SSD

Benefits

- Small, low profile solution
- Save 50% PCB area, comparing with discrete solution
- Easy to use
# TI High Density Modules for FPGA Power

<table>
<thead>
<tr>
<th>Supported Intermediate rails</th>
<th>LMZ20501</th>
<th>TPS82084/5</th>
<th>LMZ306002/4/6</th>
<th>LMZ21700/1</th>
<th>TPS82130</th>
<th>LMZ31503/06</th>
<th>LMZ31704/7/10</th>
<th>LMZ31520/30</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V, 5V</td>
<td>3.3V, 5V, 12V</td>
<td>3.3V (required 4.5-14.5V bias), 5V, 12V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vin Range</td>
<td>2.7 to 5.5V</td>
<td>2.3 to 6.0V</td>
<td>2.95 to 6.0 V</td>
<td>3.0 to 17V</td>
<td>3.0 to 17V</td>
<td>3V to 14.5V</td>
<td>3V to 17V</td>
<td>3V to 14.5V</td>
</tr>
<tr>
<td>Vout Range</td>
<td>0.6 to 3.6V</td>
<td>0.8 to Vin</td>
<td>0.8 to 3.6 V</td>
<td>0.9 to 6.0V</td>
<td>0.9 to 6.0V</td>
<td>0.8 to 5.5 V</td>
<td>0.6 to 3.6 V</td>
<td>0.6 to 3.6 V</td>
</tr>
<tr>
<td>iout (max)</td>
<td>1A</td>
<td>2A, 3A</td>
<td>2A, 4A, 6A</td>
<td>0.65A, 1A</td>
<td>3A</td>
<td>3A, 6A</td>
<td>4A, 7A, 10A</td>
<td>20A, 30A</td>
</tr>
<tr>
<td>Freq Range (KHz)</td>
<td>3000</td>
<td>2400</td>
<td>500 to 2000</td>
<td>2000</td>
<td>2000</td>
<td>330 to 780</td>
<td>200 to 1200</td>
<td>300 to 850</td>
</tr>
<tr>
<td>Ext Clock Sync</td>
<td>N</td>
<td>N</td>
<td>Y</td>
<td>N</td>
<td>N</td>
<td>Y</td>
<td>Y</td>
<td>N</td>
</tr>
<tr>
<td>EMI Tested (EN55022, Class B)</td>
<td>Y</td>
<td>N</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Current Sharing</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>N</td>
<td>Y</td>
<td>Y</td>
<td>N</td>
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<tr>
<td>Adj Soft-start</td>
<td>N</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Power Good</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
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<tr>
<td>Ext Components</td>
<td>5</td>
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<td>6</td>
<td>5</td>
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<td>7</td>
<td>6</td>
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<tr>
<td>WEBENCH</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Package (mm)</td>
<td>3.5x3.5x1.75</td>
<td>2.8x3.0x1.3</td>
<td>9x11x2.8</td>
<td>3.5x3.5x1.75</td>
<td>3x2.8x1.5</td>
<td>9x15x2.8</td>
<td>10x10x4.3</td>
<td>15x16x5.8</td>
</tr>
<tr>
<td>Alternative Regulator</td>
<td>TPS54218 (2A)</td>
<td>TPS62084 (2A)</td>
<td>TPS54218 (2A)</td>
<td>TPS54478 (4A)</td>
<td>TPS62150 (1A)</td>
<td>TPS54320 (3A)</td>
<td>TPS53513 (8A)</td>
<td>TPS53353 (15A)</td>
</tr>
<tr>
<td></td>
<td>TPS62085 (3A)</td>
<td>TPS54478 (4A)</td>
<td>TPS54678 (6A)</td>
<td>TPS62130 (3A)</td>
<td>TPS54620 (6A)</td>
<td>TPS53515 (15A)</td>
<td>TPS53515 (15A)</td>
<td>TPS53355 (25A)</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TPS53355 (25A)</td>
</tr>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TPS56221 (25A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TPS548A20 (15A)</td>
</tr>
</tbody>
</table>
Powering ADC / Data Converter

• The electrical performance of ADC’s and data converters depends on the cleanliness of their supply voltages, particularly the analog domain supply.

• Linear regulators (LDOs) are widely used to lower the input supply voltage to the various voltages needed by the data converter but the Efficiency is fairly low.

• Using a TPS6223x DCDC converter is a good choice to combine highest Efficiency with good performance of the ADC/Data Converter.
Powering ADC / Data Converter

Reference Design: Efficient, LDO-free Power Supply for a 12-bit 500-MSPS ADC

Test Results: [http://www.ti.com/lit/ug/tidubb0/tidubb0.pdf](http://www.ti.com/lit/ug/tidubb0/tidubb0.pdf)

Schematic:
Powering ADC / Data Converter

Reference Design Test Results:

- **SNR**
  - Bars showing SNR (dB) at different signal frequencies (5, 170, 230 MHz) for LDOs and SMPSs.

- **SFDR**
  - Bars showing SFDR (dB) at different signal frequencies (5, 170, 230 MHz) for LDOs and SMPSs.

- **Input Current Consumption**
  - Bars showing input current consumption in mA at 5V input voltage for LDOs and SMPSs.

- **Efficiency**
  - Bars showing efficiency (%) for LDOs and SMPSs.
Online Resources

TI Modules
• www.ti.com/modules

TI Power Products:
• TI Power – www.ti.com/power
• LDOs – www.ti.com/ldo

Power and Analog Resources for FPGAs
• Xilinx: www.ti.com/xilinx
• Altera: www.ti.com/altera

Design Resources
• TI WEBENCH® FPGA Power Architect Tool Overview
• TI Designs Search “FPGA”:
  http://www.ti.com/general/docs/refdesignsearch.tsp
Thank you!