

Building the SAR ADC Simulation Model

TIPL 4403

TI Precision Labs – ADCs

Created by Tim Green, Art Kay

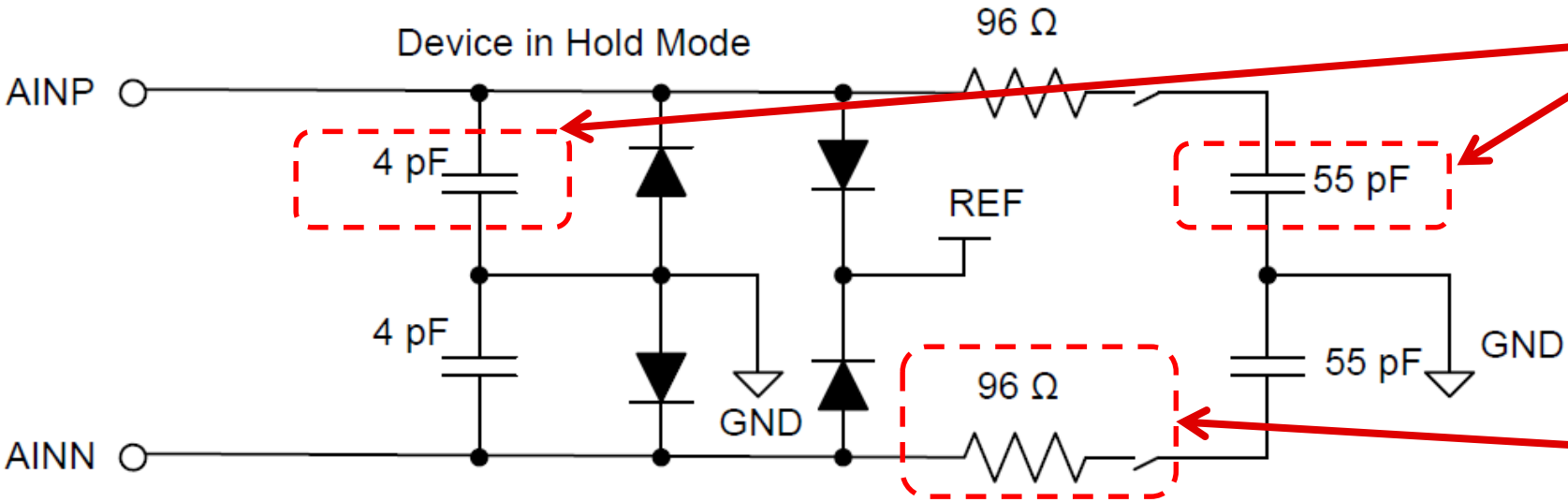
Presented by Peggy Liska

Agenda

1. SAR Operation Overview
2. Select the data converter
3. Use the Calculator to find amplifier and RC filter
4. Find the Op Amp
5. Verify the Op Amp Model
6. **Building the SAR Model**
7. Refine the Rfilt and Cfilt values
8. Final simulations
9. Measured Results
10. SAR Drive Calculator Algorithm

Equivalent Circuit: Translate to TINA

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Full-scale input span ⁽¹⁾	AINP – AINN	0		V _{REF}	V
Operating input range ⁽¹⁾	AINP	-0.1		V _{REF} + 0.1	V
	AINN	-0.1		+ 0.1	V
C _i Input capacitance	AINP and AINN terminal to GND		59		pF
Input leakage current	During acquisition for dc input		5		nA



59pF = 55pF + 4pF

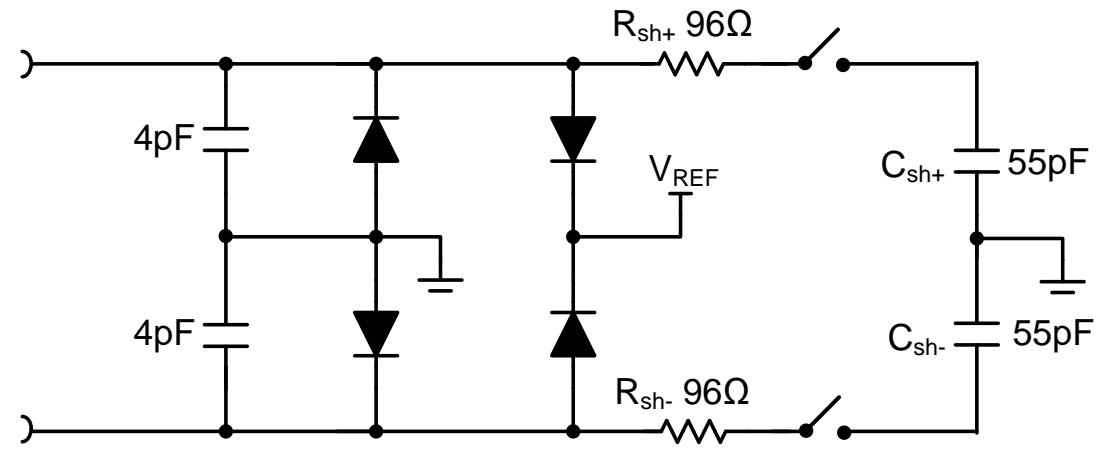
$$R_{sh} \approx \frac{t_{acq_min}}{100 \cdot C_{sh}}$$

$$R_{sh} \approx \frac{290ns}{100 \cdot 55pF} = 53\Omega$$

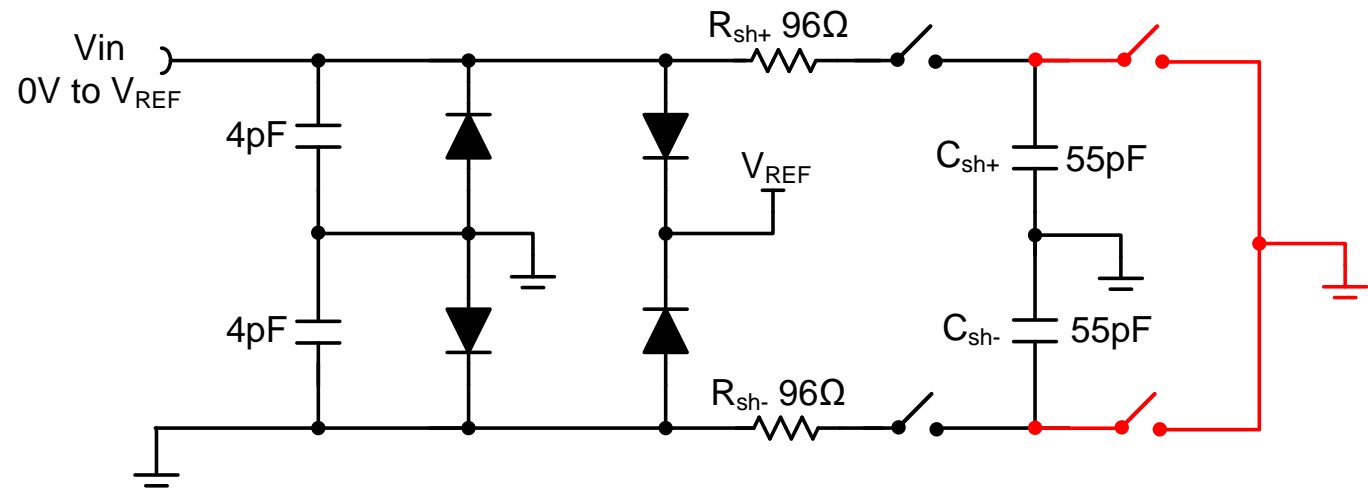
Figure 45. Input Sampling Stage Equivalent Circuit

Simplifying the input model

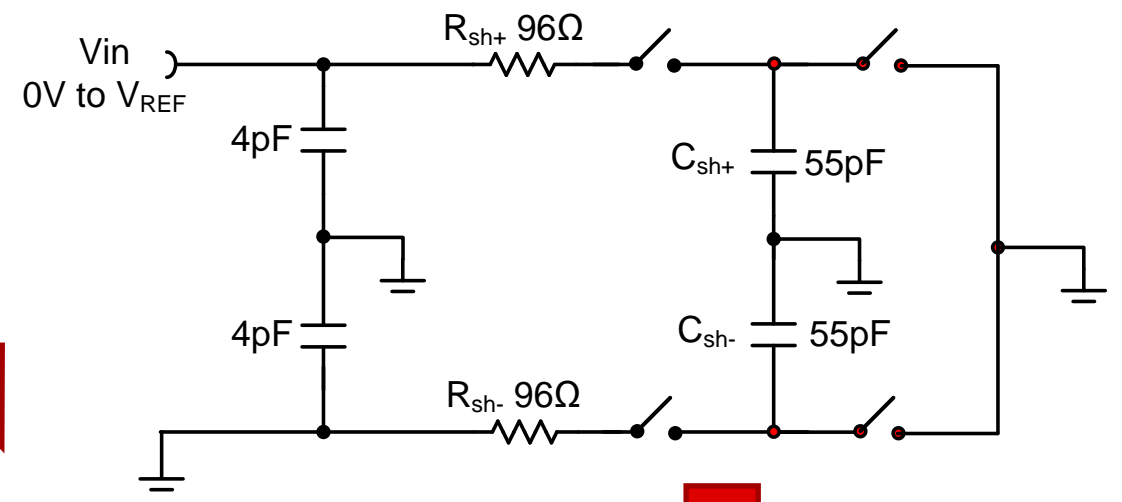
1) Input Circuit from the data sheet



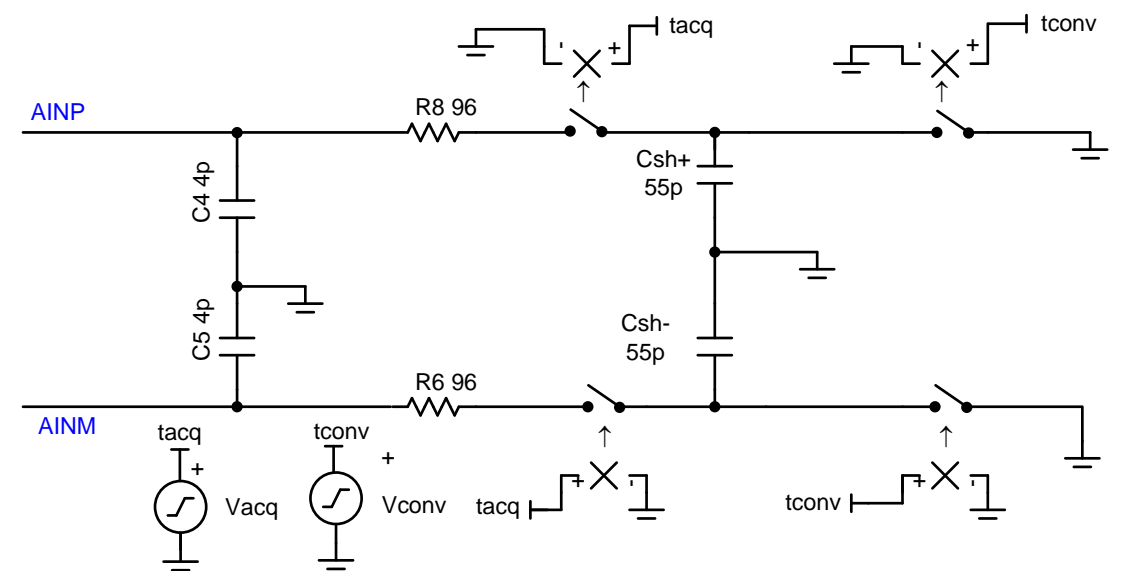
2) Add the sample and hold reset circuit



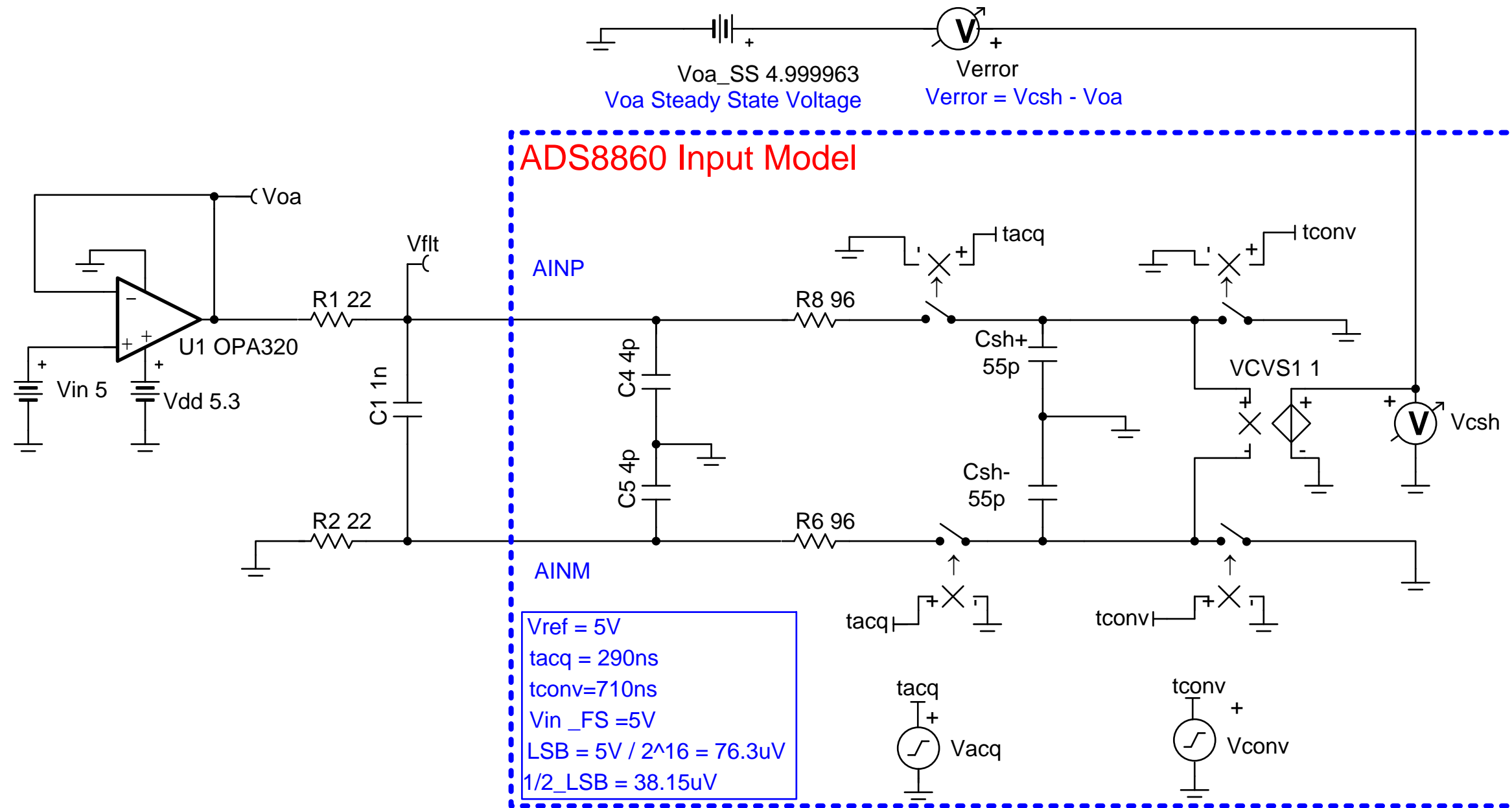
3) Diodes are reverse bias



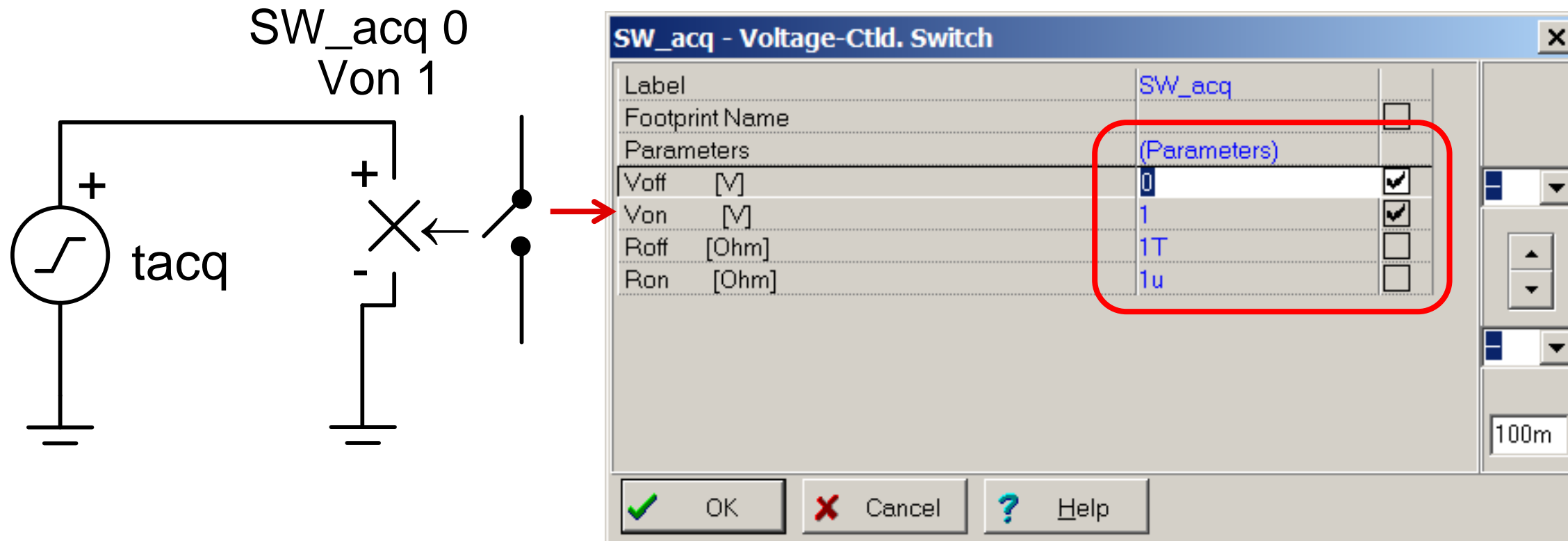
4) TINA Spice Model



TINA SPICE Equivalent Model



Configure the voltage controlled switch



The image shows a circuit diagram on the left and a configuration dialog box on the right. The circuit diagram features a voltage source labeled 'tacq' connected to a switch component labeled 'SW_acq 0' with a threshold voltage 'Von 1'. A red arrow points from the switch in the circuit to the configuration dialog box.

The dialog box, titled 'SW_acq - Voltage-Ctld. Switch', contains the following parameters:

Parameter	Value	Checked
Label	SW_acq	<input type="checkbox"/>
Footprint Name		<input type="checkbox"/>
Parameters	(Parameters)	
Voff [V]	0	<input checked="" type="checkbox"/>
Von [V]	1	<input checked="" type="checkbox"/>
Roff [Ohm]	1T	<input type="checkbox"/>
Ron [Ohm]	1u	<input type="checkbox"/>

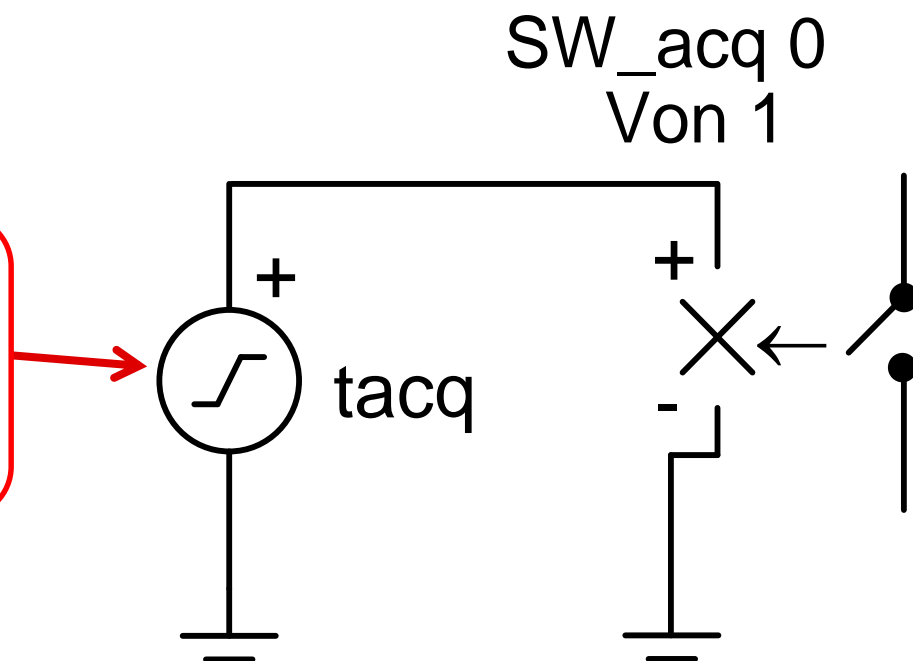
Buttons at the bottom of the dialog include 'OK', 'Cancel', and 'Help'. A '100m' scale factor is visible in the bottom right corner of the dialog.

Set all parameters as shown.

Default Roff=1GΩ and Ron=0Ω will impact accuracy.

Configure the signal source to control the switch

1. Click on source to select and edit switch control signal



3. Select "Piecewise linear"

Label	tacq
Footprint Name	L9802 (VG)
Parameters	(Parameters)
DC Level [V]	0
Signal	Piecewise linear
Internal resistance [Ohm]	0
IO state	Input
Fault	None

2. Under signal, click here to edit.

Max: 1

Min: 0 Max: 1u

```
REPEAT FOREVER
0.000E+00      0.000E+00
1.000E-09      1.000E+00
2.890E-07      1.000E+00
2.900E-07      0.000E+00
1.000E-06      0.000E+00
ENDREPEAT
```

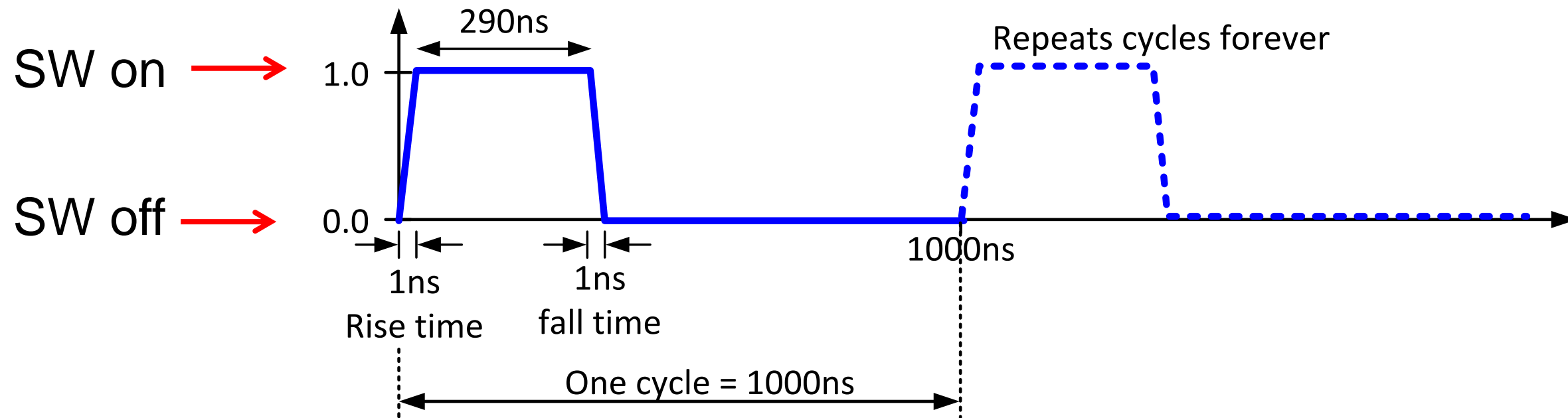
Successfully compiled

Line: 1 Col: 1

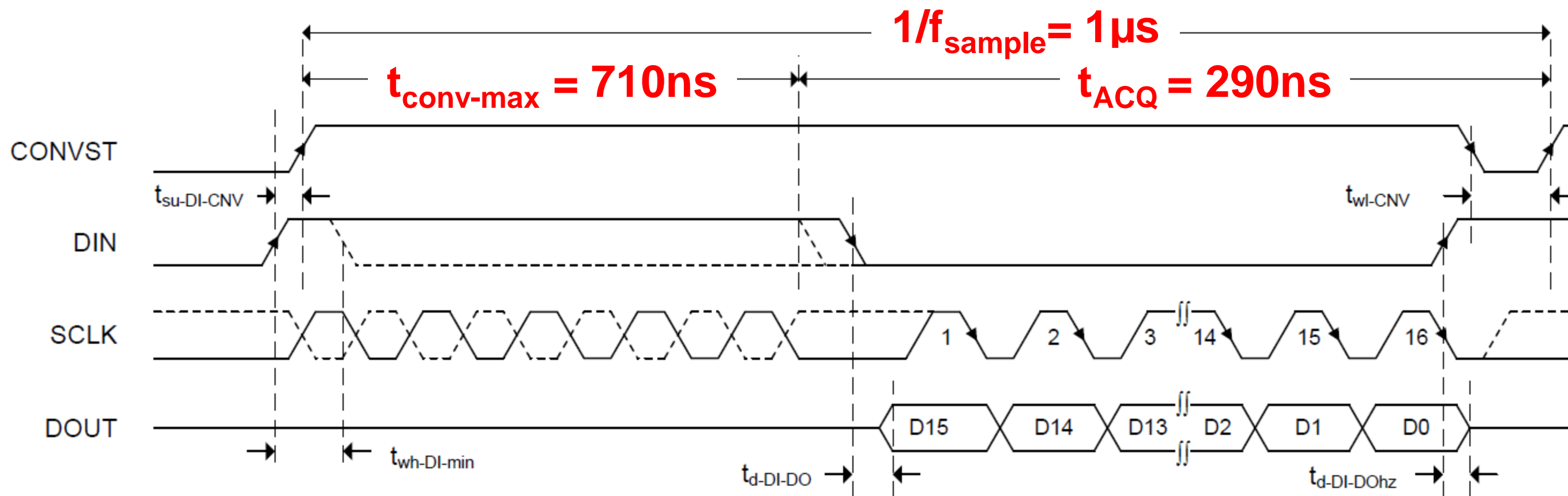
Configure the signal source to control the switch

Time

Voltage levels
On: $V \geq 1V$
Off: $V \leq 0V$



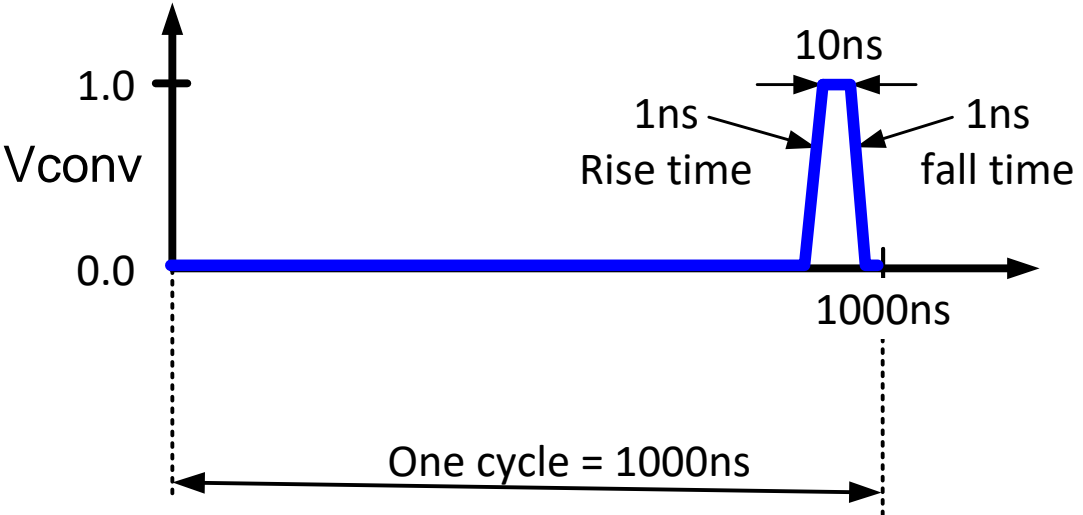
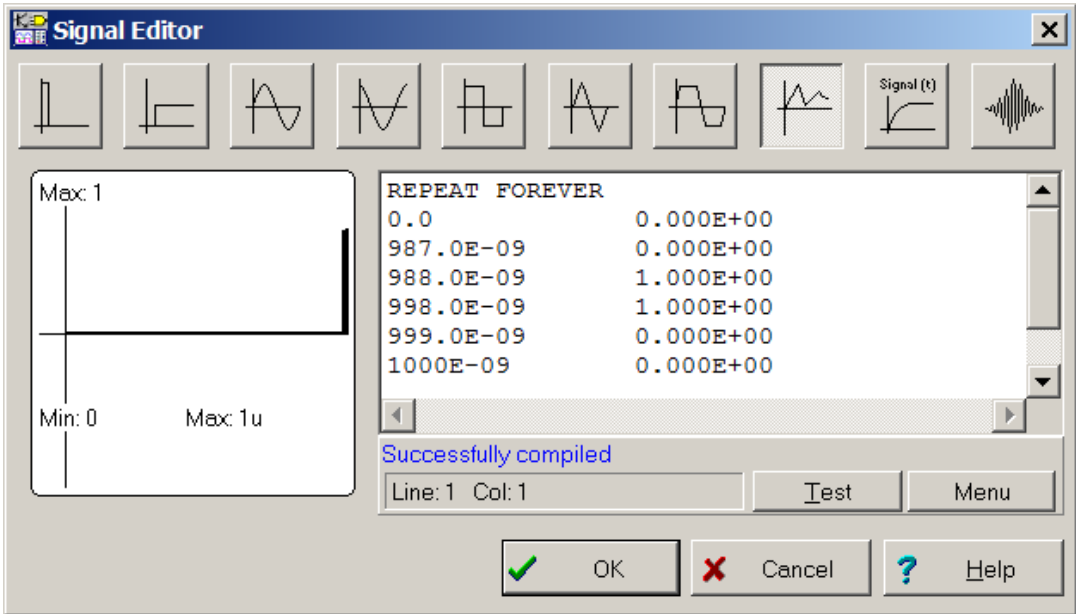
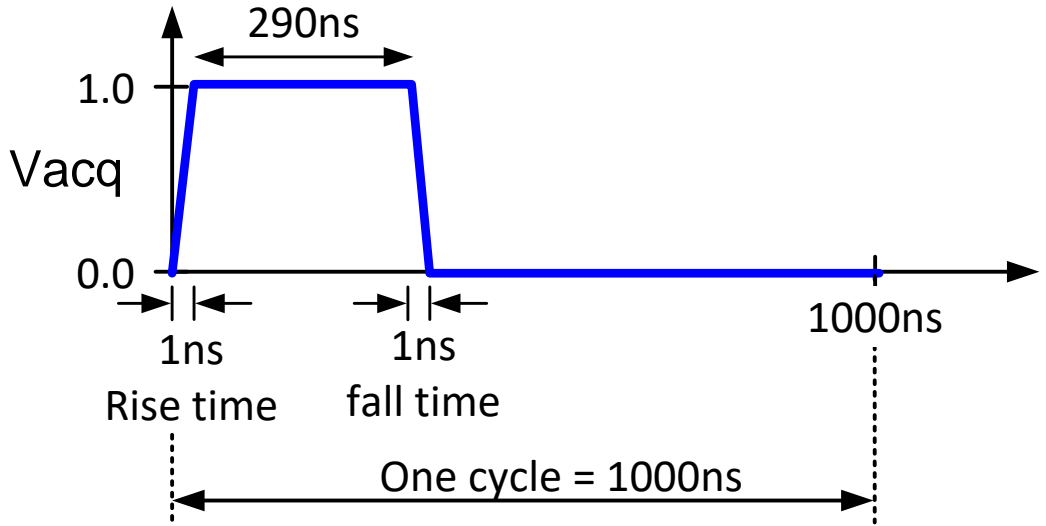
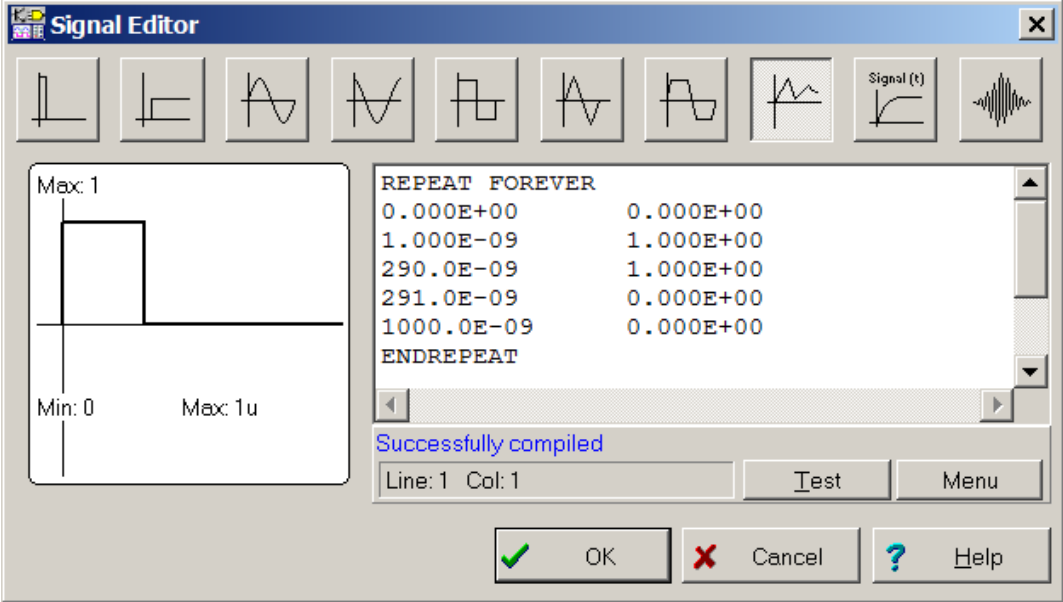
Timing diagram



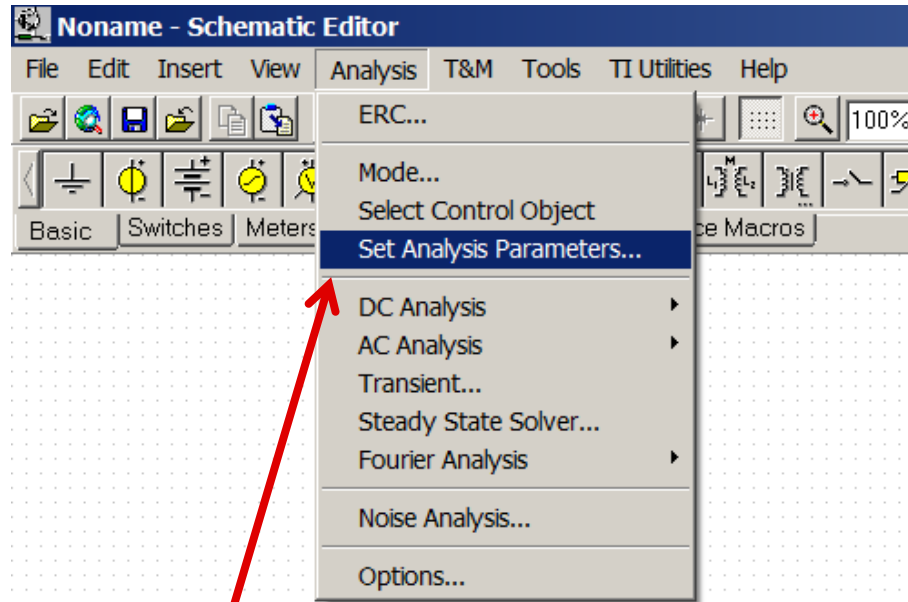
Parameter	MIN	TYP	MAX	UNIT
t_{acq} Acquisition time	290			ns
t_{conv} Conversion time	500		710	ns

$1/f_{\text{sample}} = 290\text{ns} + 710\text{ns}$
 $1/f_{\text{sample}} = 1\mu\text{s}$
 $f_{\text{sample}} = 1\text{MHz}$

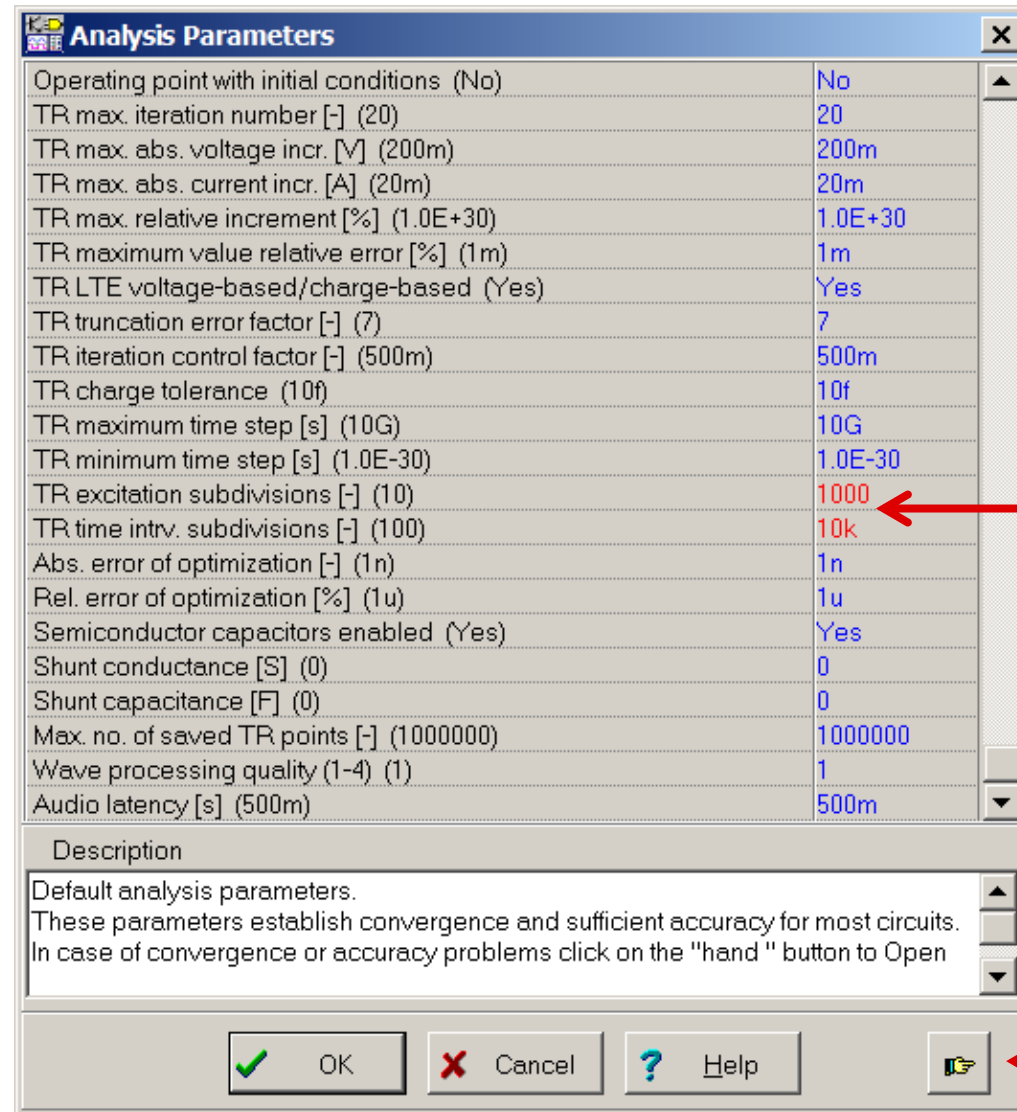
Example simulation: simulator settings



Optimizing Simulation Results



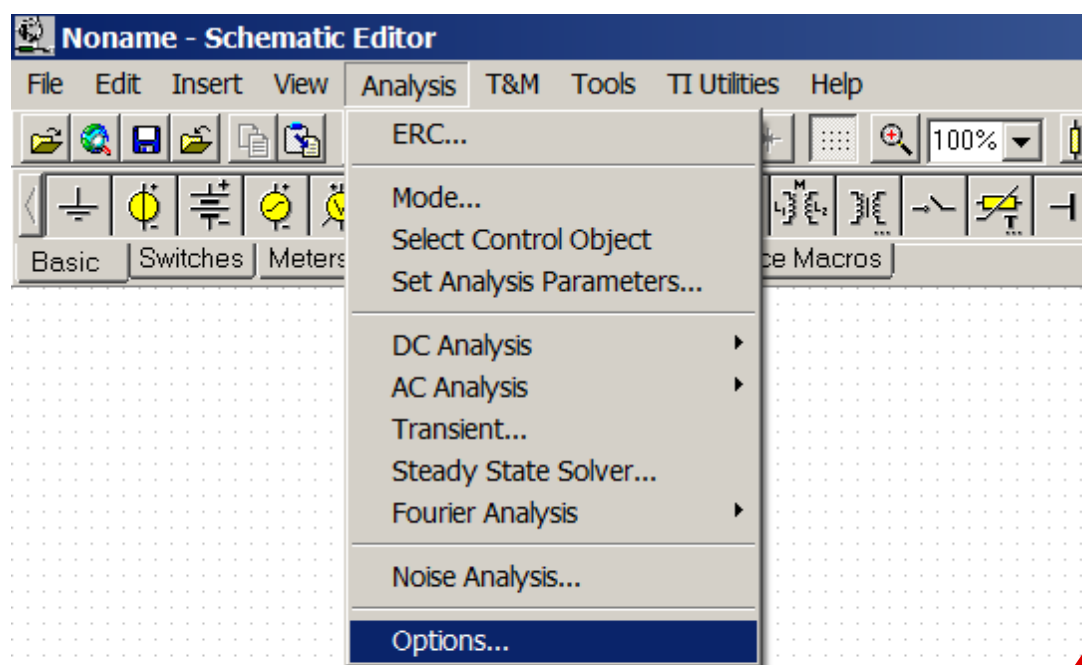
“Set Analysis Parameters”
adjusts how the simulator math
engine operates.



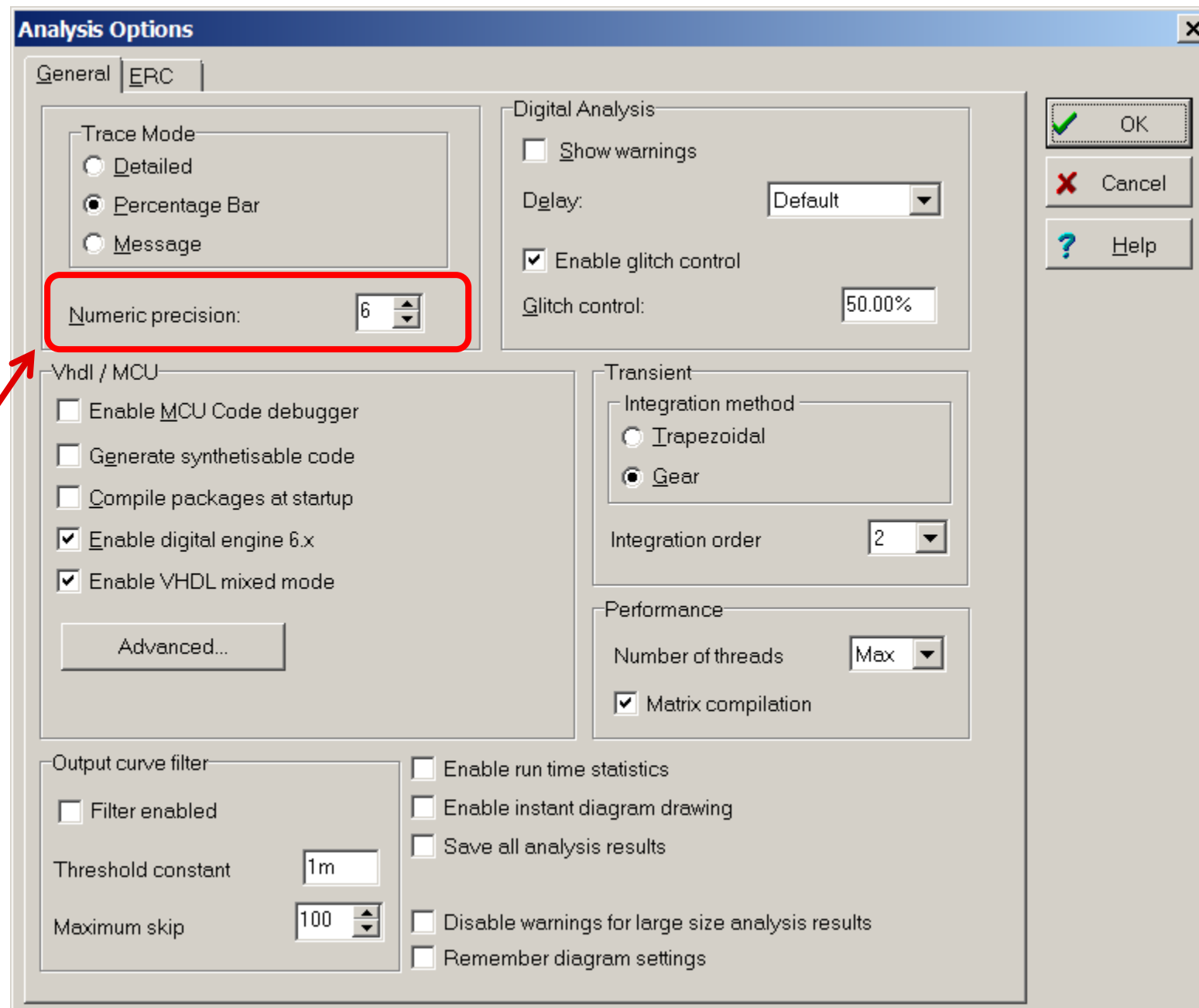
TR excitation subdivisions = 1000
TR time intrv. subdivisions = 10k
This increases the number of
points vs time so that transient
behaviors aren't obscured.

Press this button to
expand the list.

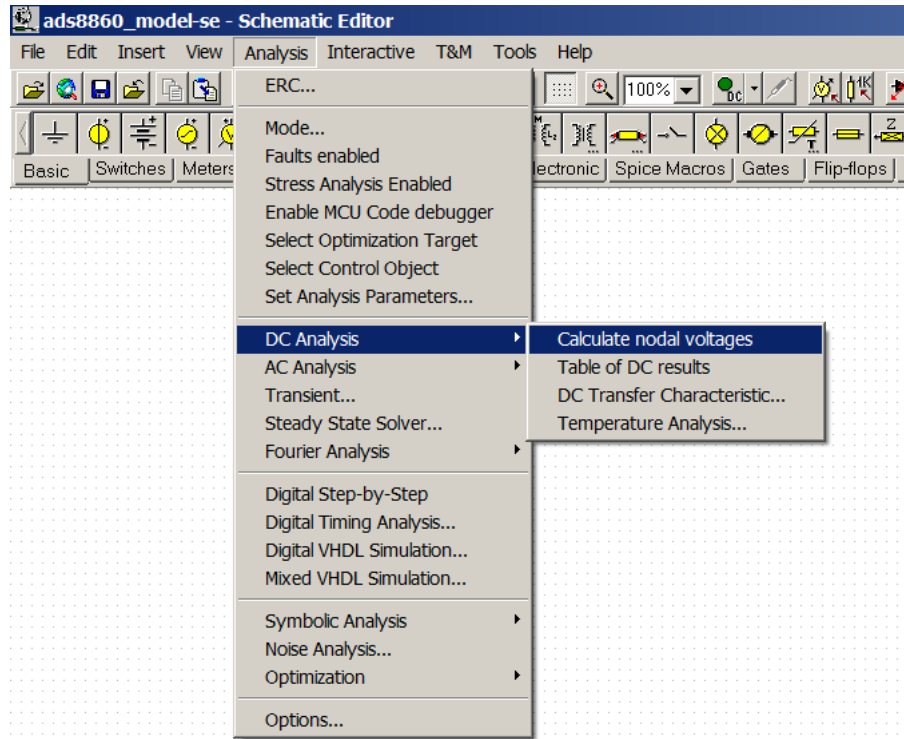
Optimizing Simulation Results



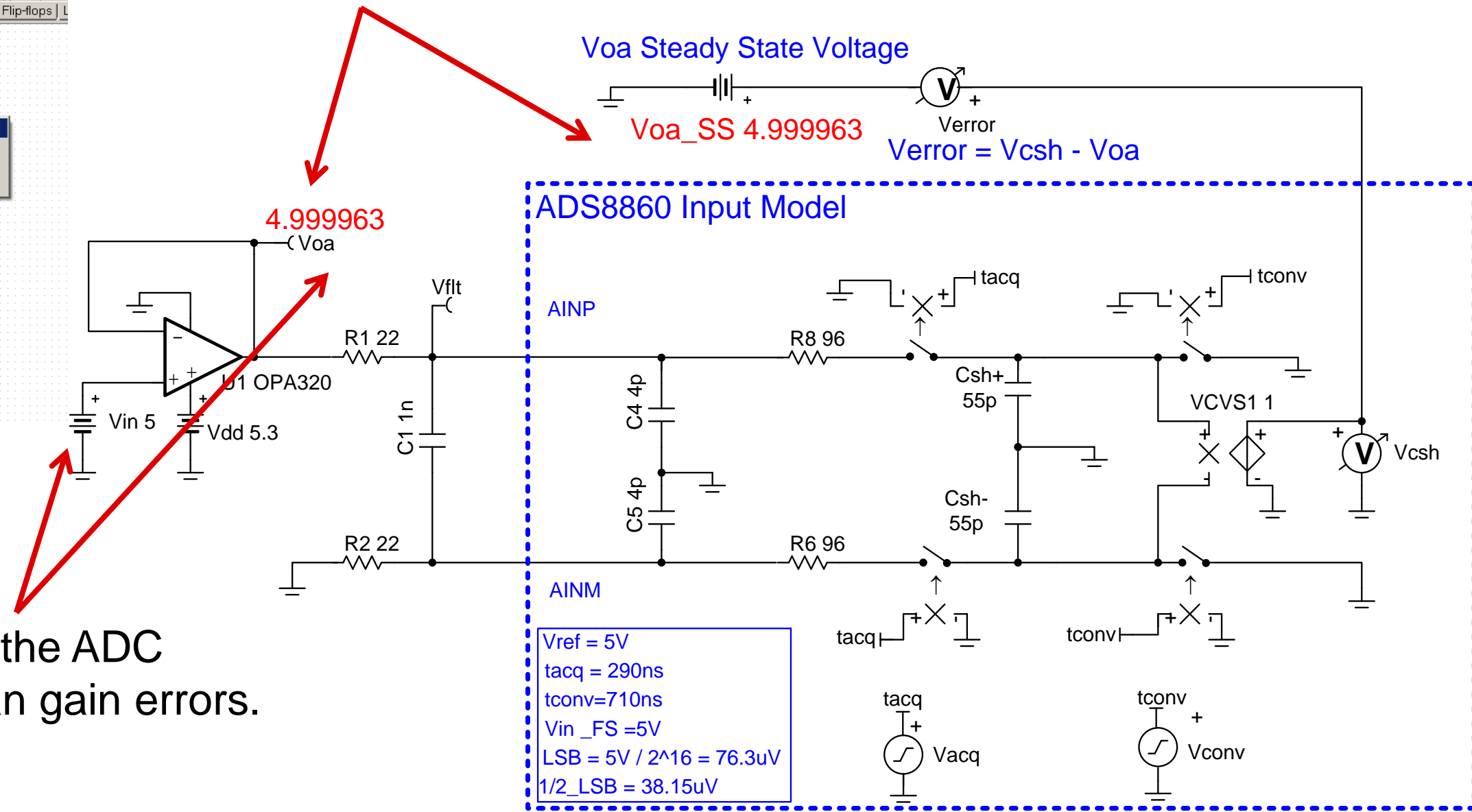
Set the “numeric precision” to 6 digits. This will allow us to see dc operating points to six digits. The importance of this is highlighted on the next slide.



Steady State Simulation Results

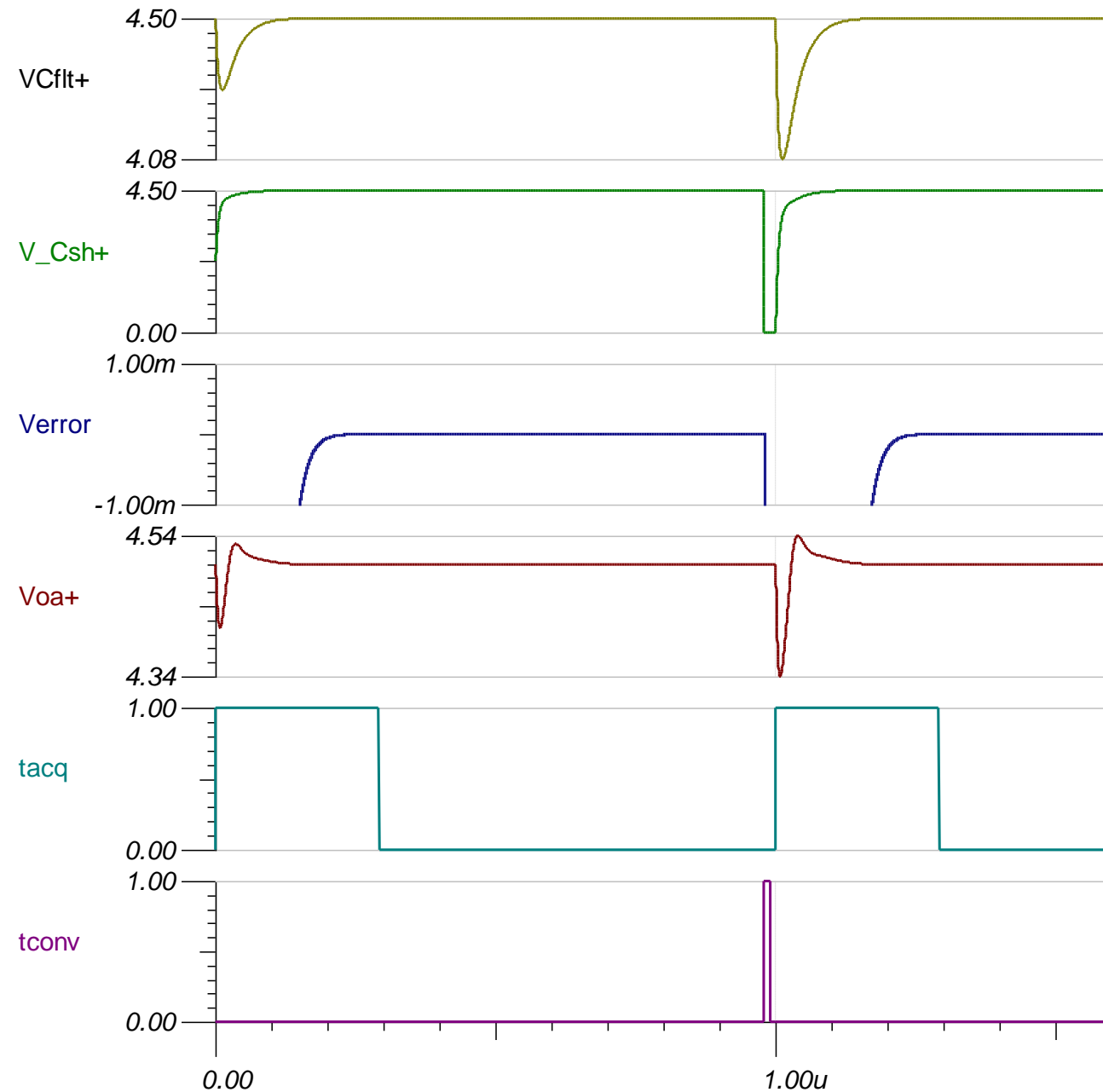
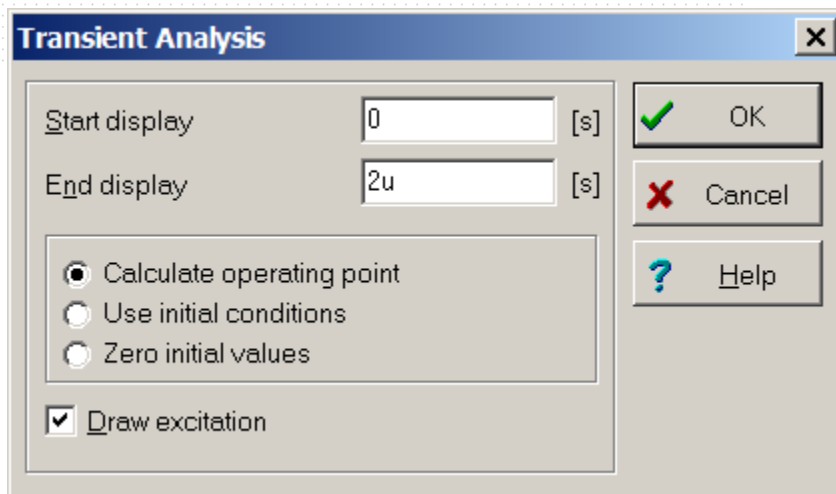
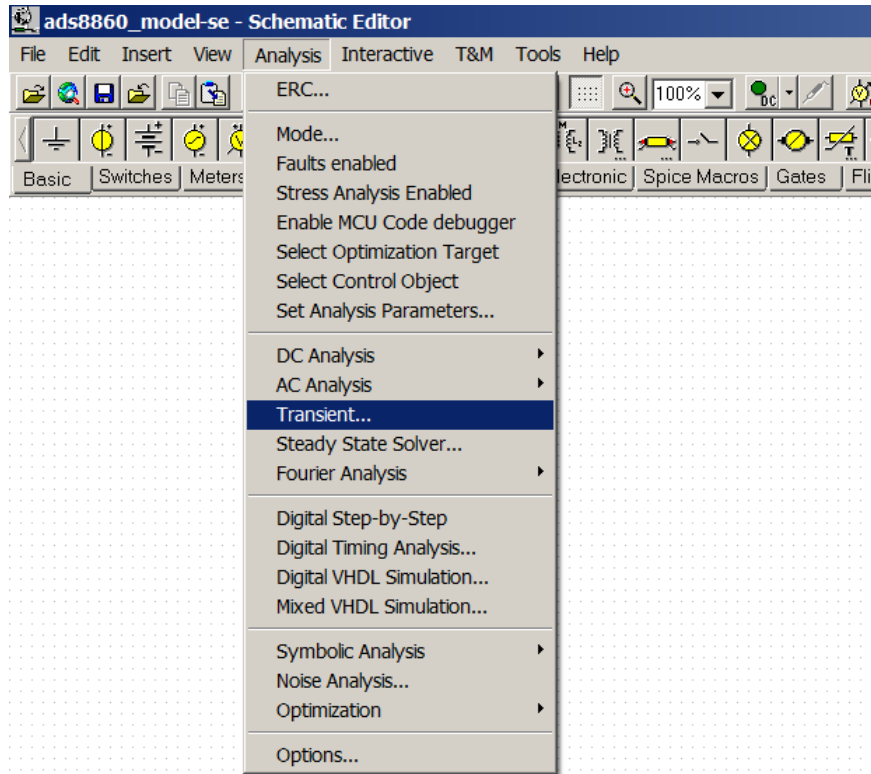


Set the output source to match the steady state ADC input.



The steady state input to the ADC includes amplifier offset and gain errors.

Example simulation: simulator results



Input to ADC across Charge bucket filter

Internal ADC sample and hold capacitor

Error in ADC settling sampled signal

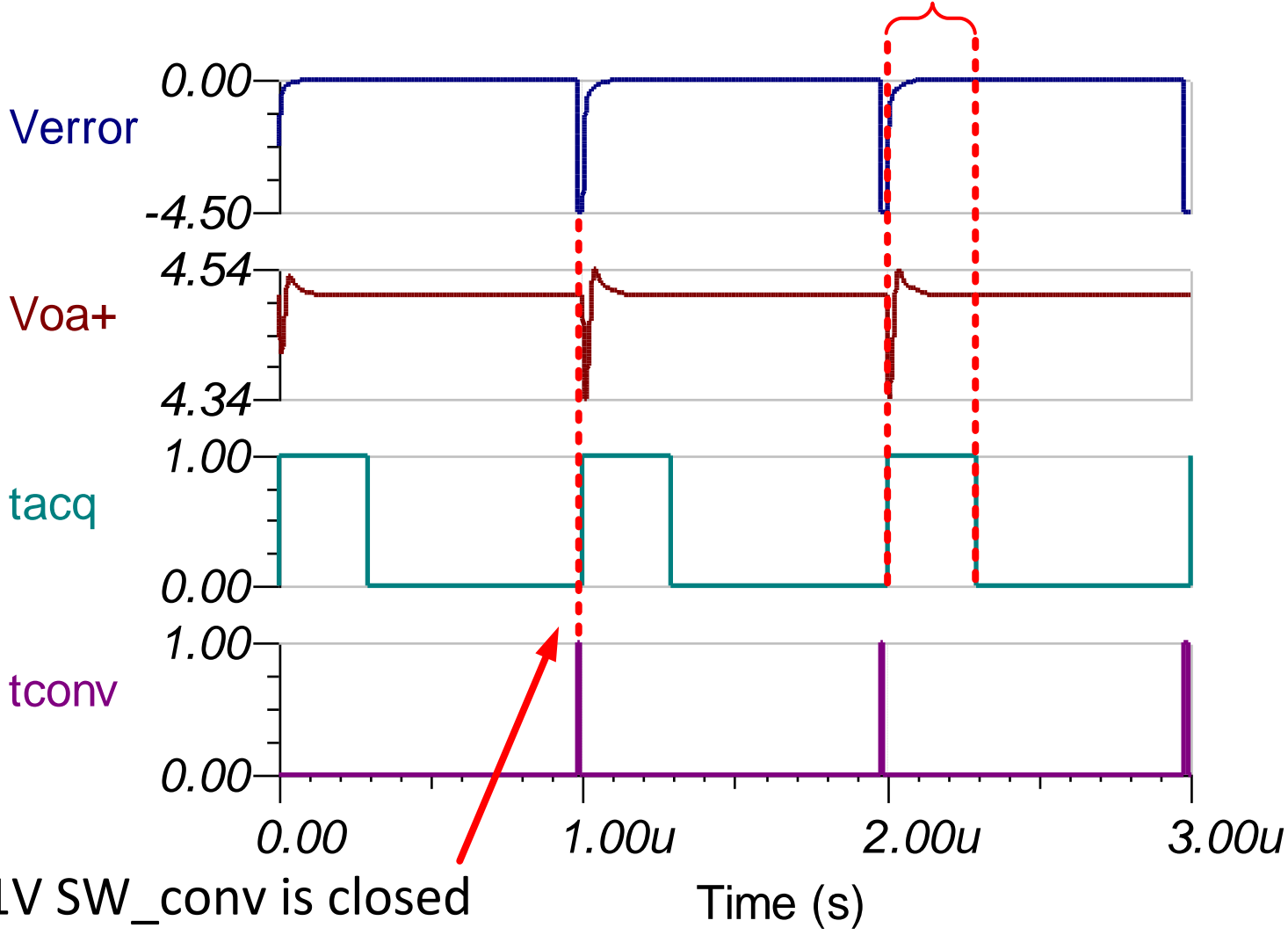
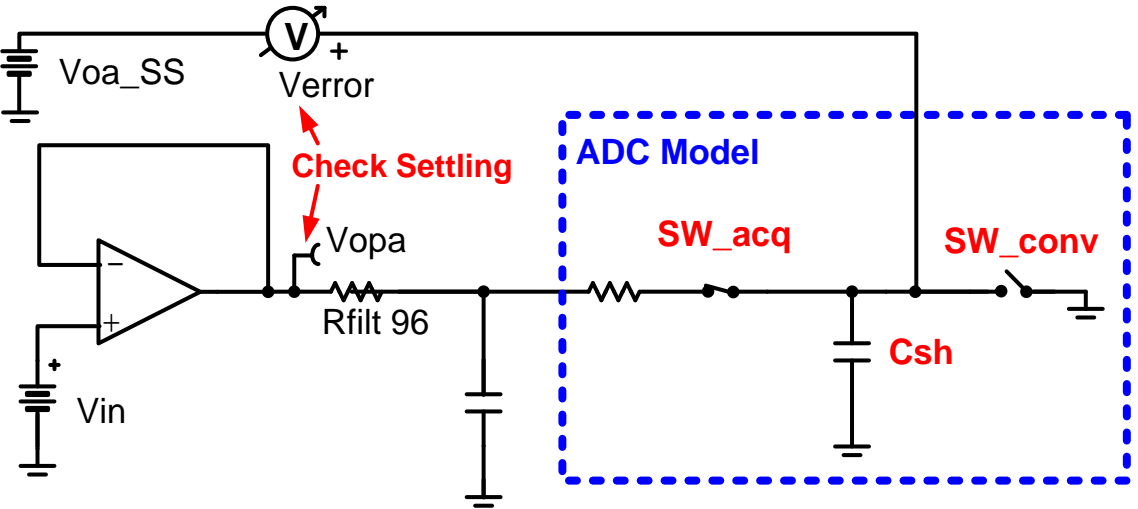
Op amp output

Acquisition switch control

Conversion switch control

Key Result: Error Signal

When $t_{acq} = 1V$ SW_acq is closed
 Verror and Vopa must settle in this window



When $t_{conv} = 1V$ SW_conv is closed
 This resets the internal S &H Capacitor Csh

Zoom in on Error Signal

$$N = 16$$

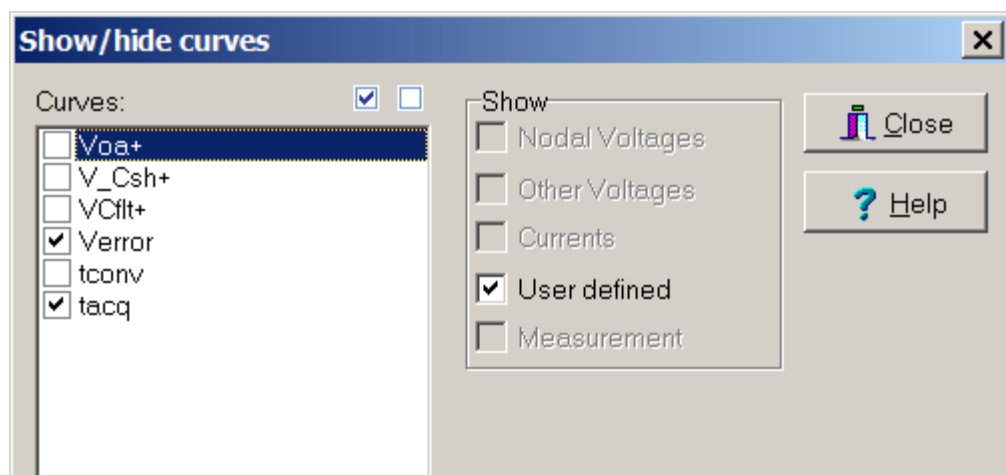
$$\text{LSB} = \frac{\text{FSR}}{2^N} = \frac{5.0\text{V}}{2^{16}} = 76.3\mu\text{V}$$

$$0.5 \cdot \text{LSB} = 38.1\mu\text{V}$$

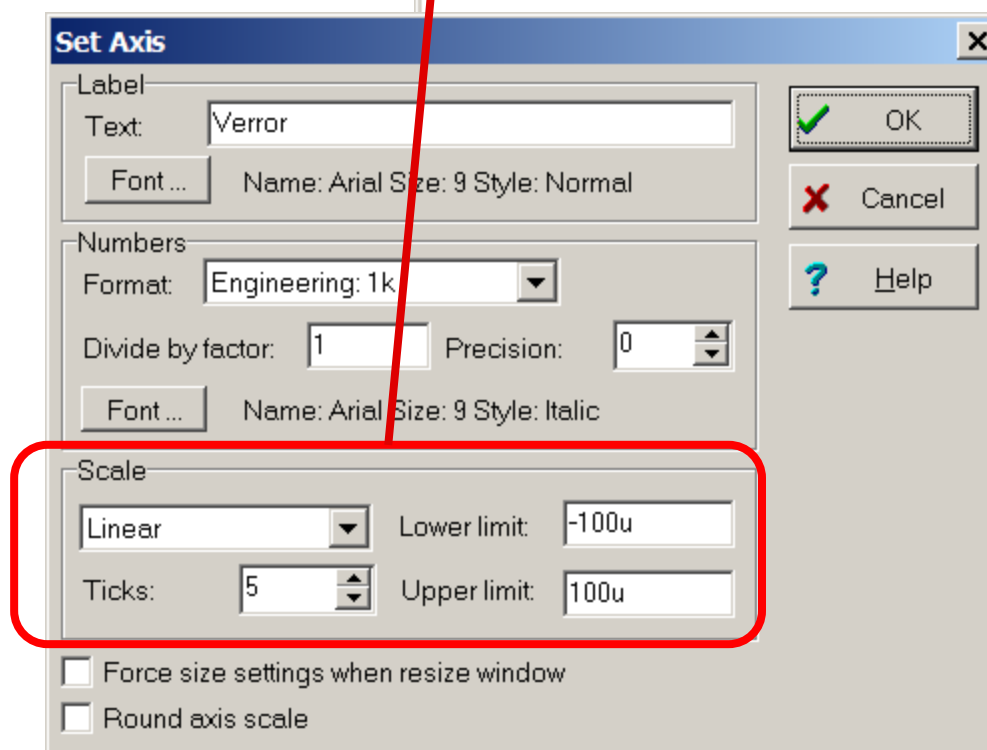
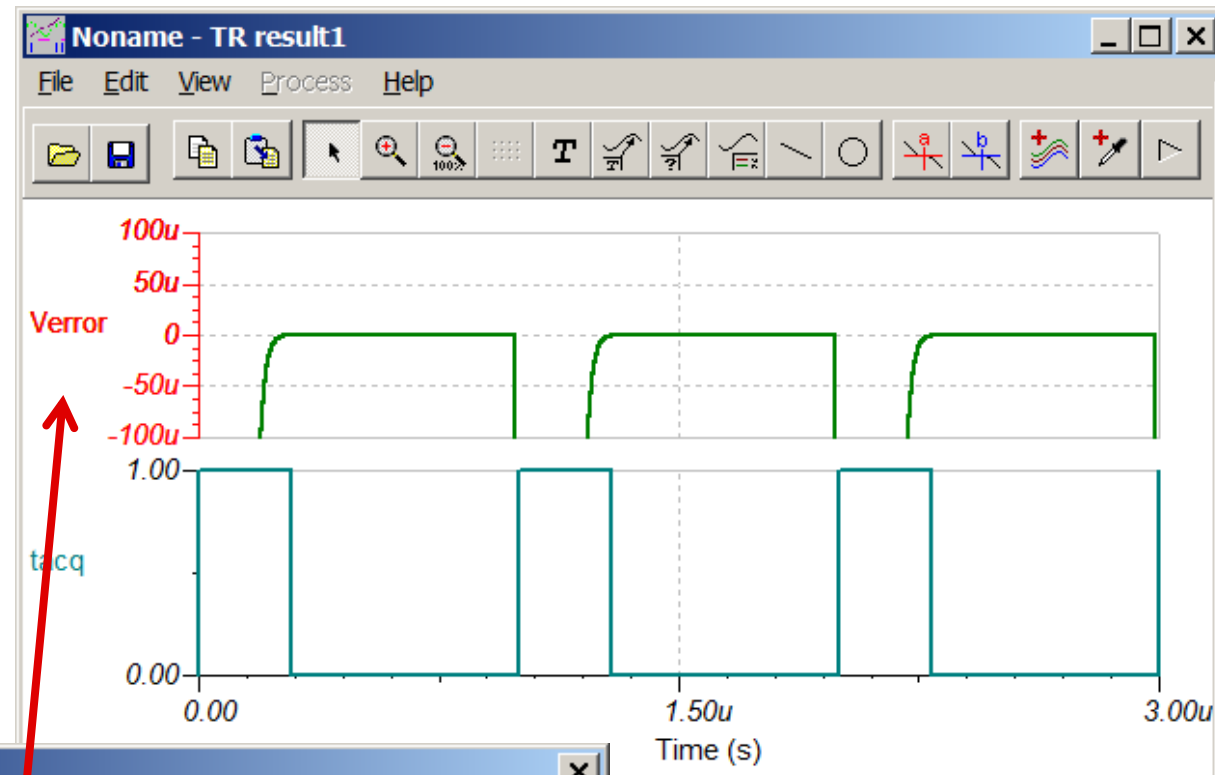
Number of bits

Resolution

Target Error



Use “view>show / hide curves” to focus on most important curves.



Click on axis and adjust the scale relative to LSB resolution.

Agenda – next video...

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Thanks for your time!
Please try the quiz.



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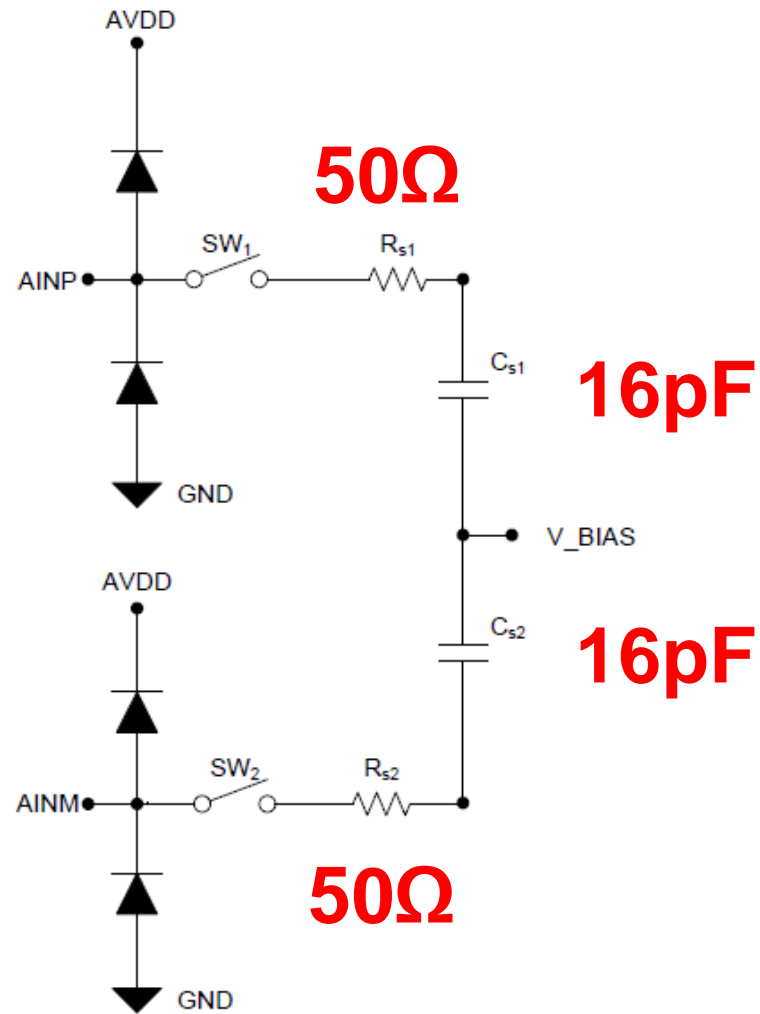
Quiz: Building the SAR ADC Simulation Model

1. Build the model for ADS7056.

Solutions

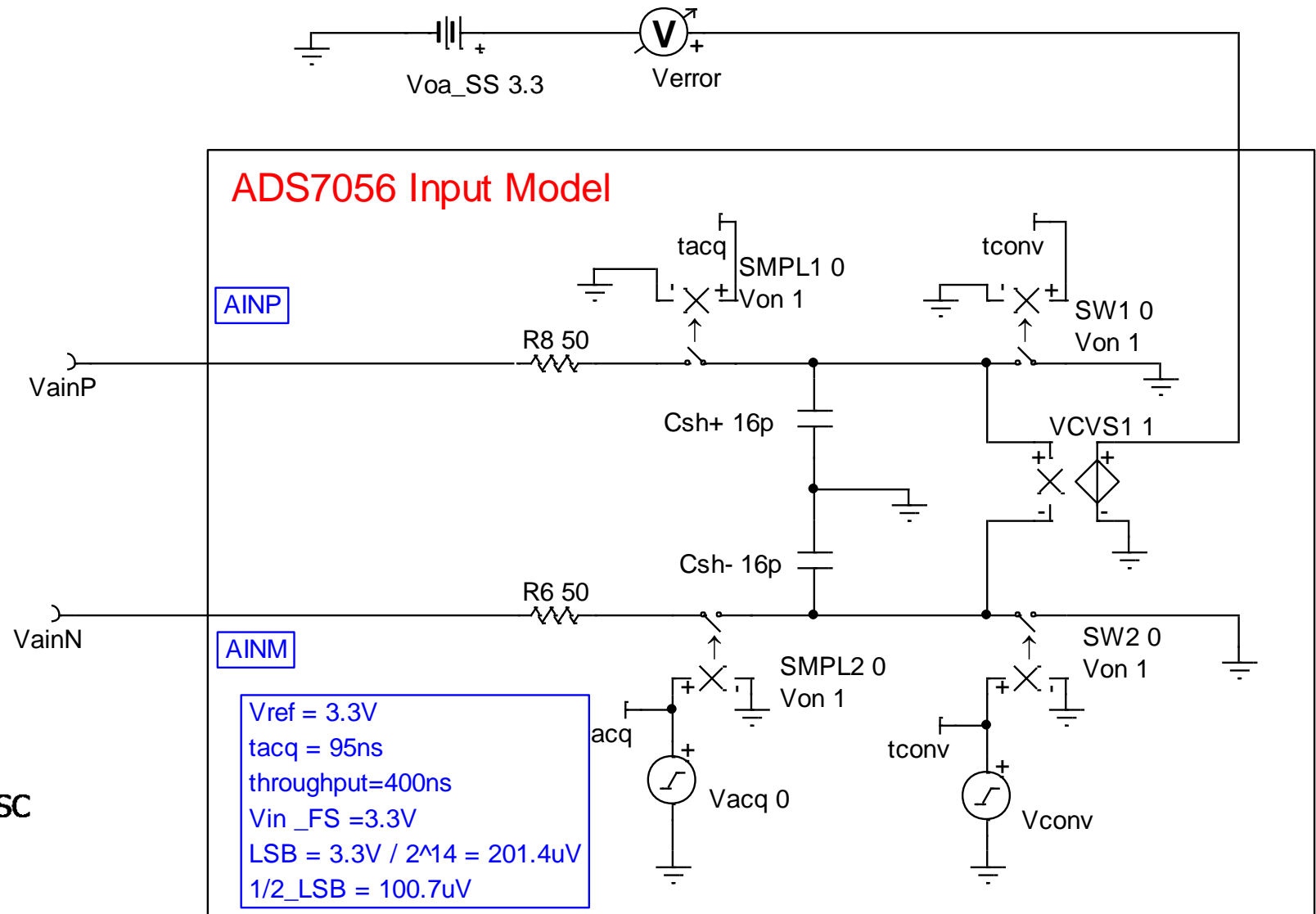
Quiz: Building the SAR ADC Simulation Model

1. Build the model for ADS7056.



ads7056 model.TSC

Click here for the TINA file



Quiz: Building the SAR ADC Simulation Model

1. Build the model for ADS7056.

