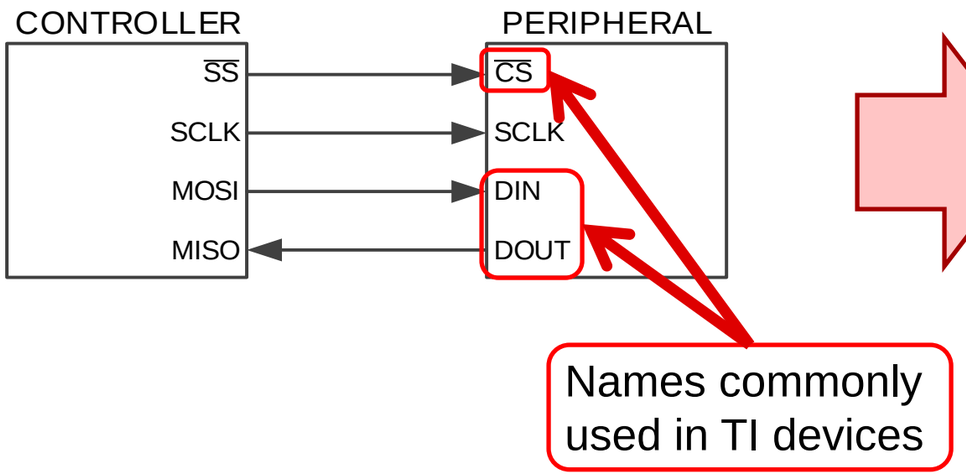
# Basics of SPI: Timing Requirements and Switching Characteristics

## TIPL 6002
## TI Precision Labs – Digital Communications

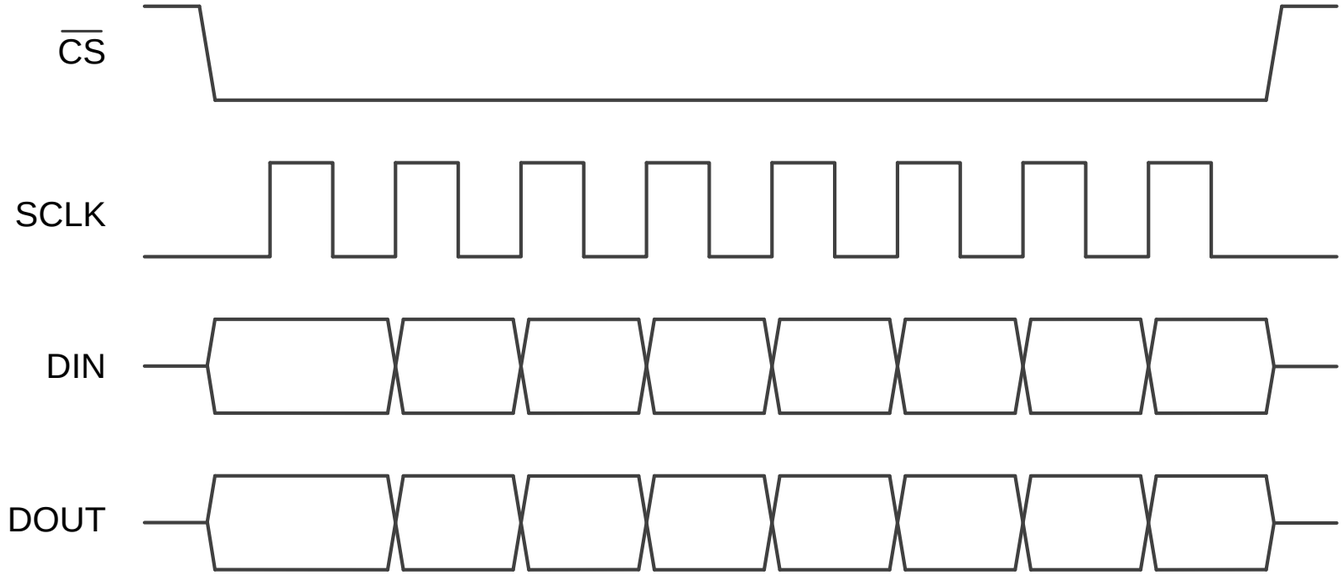
**Presented by Alex Smith**

**Prepared by Joseph Wu**

# SPI Communication




**A timing diagram shows the specifications and the timing relationship between the SPI digital lines**



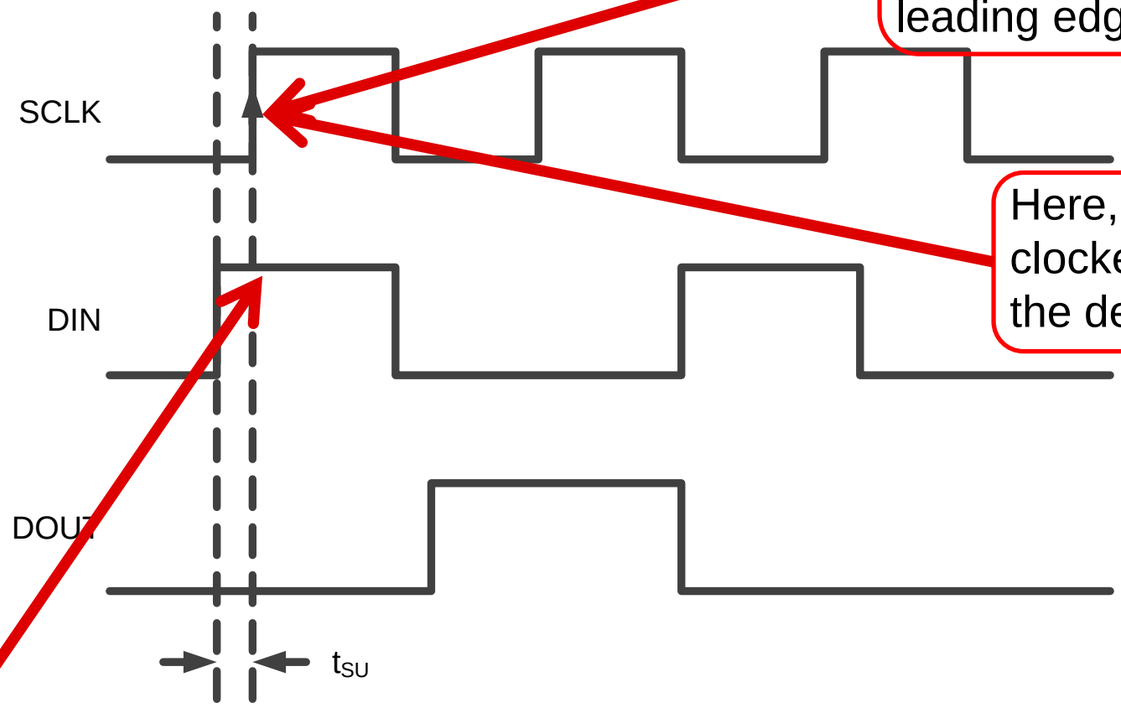

**Violating a timing specification can cause a failure to read the data and may cause unexpected results.**

# SPI Timing: Setup Time

Setup time

Hold time

Propagation Delay




Example is SPI mode 0: SCLK idles low and data is clocked in on the leading edge of SCLK

Here, a 1 is clocked into the device

The state of DIN is read into the device at the rising edge of SCLK. To ensure the data is correctly read, DIN must be at the correct state for a setup time **before** the SCLK rises

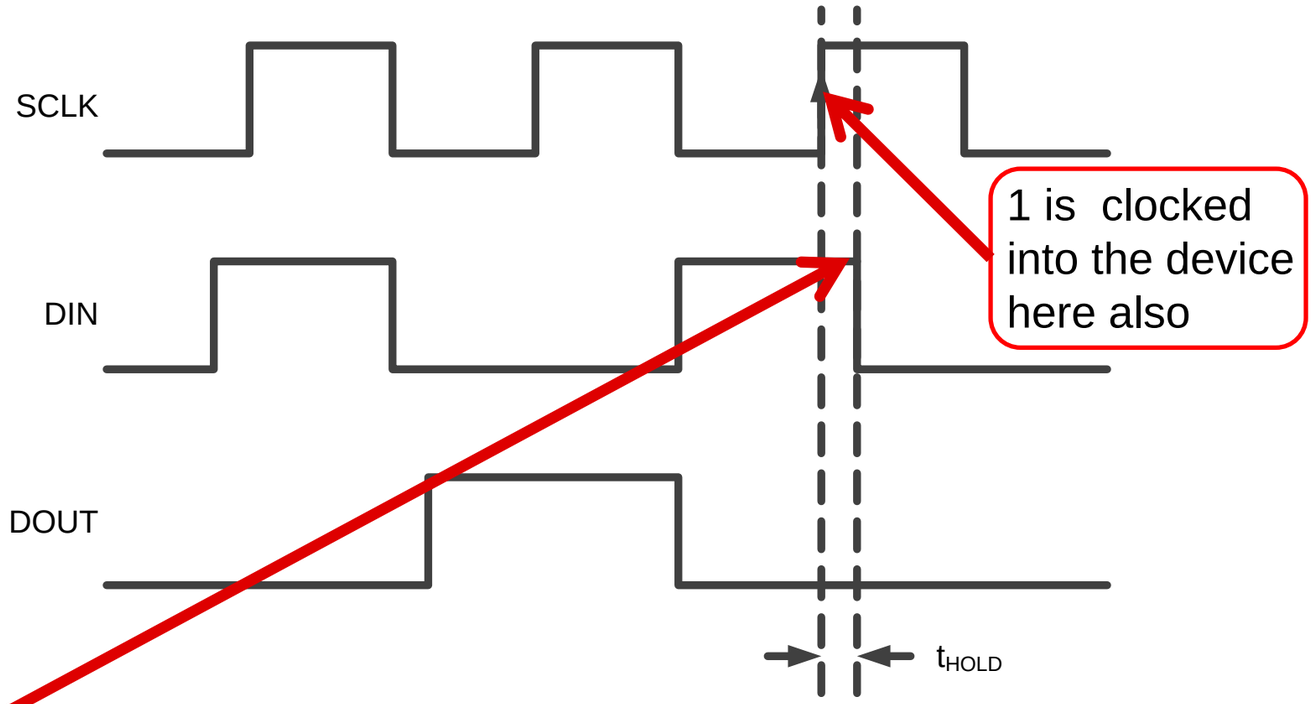
**Setup time is the minimum time required before the clocking edge for which the data must be stable to be latched correctly**

# SPI Timing: Hold Time

Setup time

Hold time

Propagation Delay




Again, the state of DIN is read into the device at the rising edge of SCLK. DIN must be held at the correct state for a hold time **after** the SCLK rises

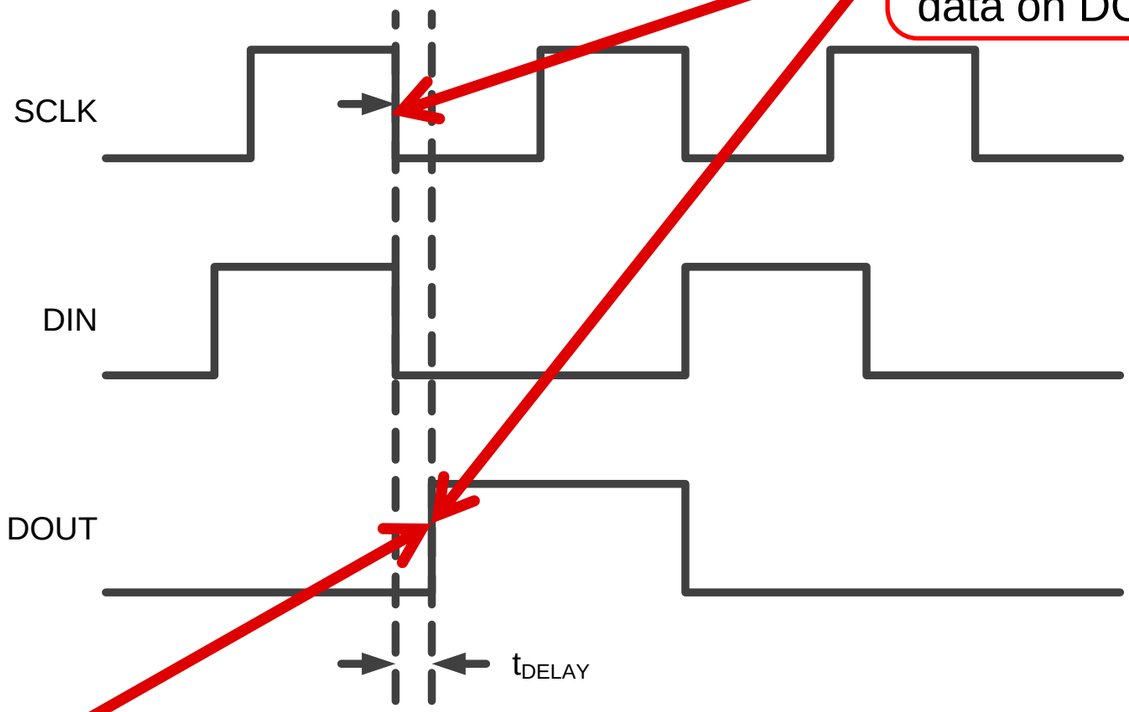
**Hold time is the minimum time required after the clocking edge for which the data must be stable to be latched correctly**

# SPI Switching: Propagation Delay

Setup time

Hold time

Propagation Delay




The falling edge of SCLK sets up the data on DOUT

DOUT is read by the controller at the rising edge of SCLK. However, the peripheral sets the output at the previous falling edge of SCLK. This delay from one clock event to the response is a propagation delay.

**Propagation delay is the time required for an input change to cause an output change through the digital circuitry**

# SPI Timing

**Timing Requirements and Switching Characteristics example from the ADS1118**

Timing Requirements are typically setup times and hold times

### 7.6 Timing Requirements: Serial Interface

Over operating ambient temperature range and VDD = 2 V to 5.5 V (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{CSSC}$ | Delay time, $\overline{CS}$ falling edge to first SCLK rising edge(1) | 100 | | ns |
| $t_{SCCS}$ | Delay time, final SCLK falling edge to $\overline{CS}$ rising edge | 100 | | ns |
| $t_{CSH}$ | Pulse duration, $\overline{CS}$ high | 200 | | ns |
| $t_{SCLK}$ | SCLK period | 250 | | ns |
| $t_{SPWH}$ | Pulse duration, SCLK high | 100 | | ns |
| $t_{SPWL}$ | Pulse duration, SCLK low(2) | 100 | | ns |
| | | | 28 | ms |
| $t_{DIST}$ | Setup time, DIN valid before SCLK falling edge | 50 | | ns |
| $t_{DIHD}$ | Hold time, DIN valid after SCLK falling edge | 50 | | ns |
| $t_{DOHD}$ | Hold time, SCLK rising edge to DOUT invalid | 0 | | ns |

(1) $\overline{CS}$ can be tied low permanently in case the serial bus is not shared with any other device.
(2) Holding SCLK low longer than 28 ms resets the SPI interface.

Switching Characteristics are typically propagation delays

### 7.7 Switching Characteristics: Serial Interface

Over operating ambient temperature range (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{CSDOD}$ | Propagation delay time, $\overline{CS}$ falling edge to DOUT driven | DOUT load = 20 pF \|\| 100 kΩ to GND | | | 100 | ns |
| $t_{DOPD}$ | Propagation delay time, SCLK rising edge to valid new DOUT | DOUT load = 20 pF \|\| 100 kΩ to GND | 0 | | 50 | ns |
| $t_{CSDOZ}$ | Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance | DOUT load = 20 pF \|\| 100 kΩ to GND | | | 100 | ns |

# SPI Timing Diagram

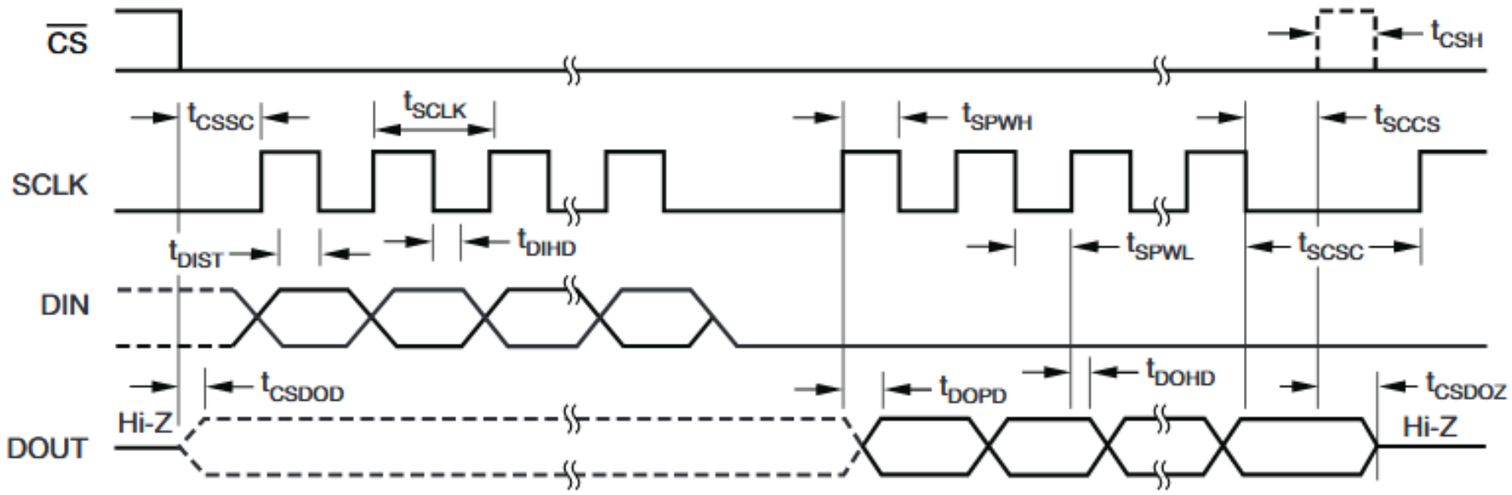



**Figure 1. Serial Interface Timing**

**Timing diagram for the ADS1118**

Device uses SPI Mode 1: SCLK idles low, data clocked in at falling edge of SCLK

Boxes for DIN and DOUT are high or low data

Arrows enclose timing specifications

# SPI Timing Diagram

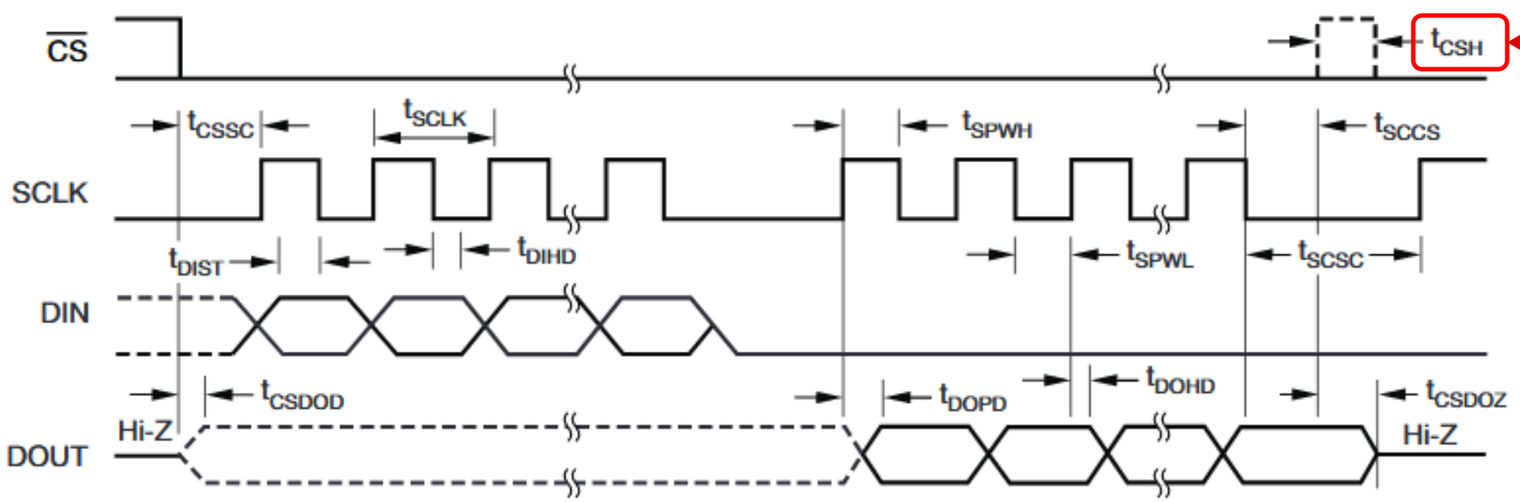



**Figure 1. Serial Interface Timing**

**$t_{CSH}$**

Minimum pulse duration, CS high

This time defines the time required for the CS to stay high to ensure that the device has reset the SPI communications.

# SPI Timing Diagram

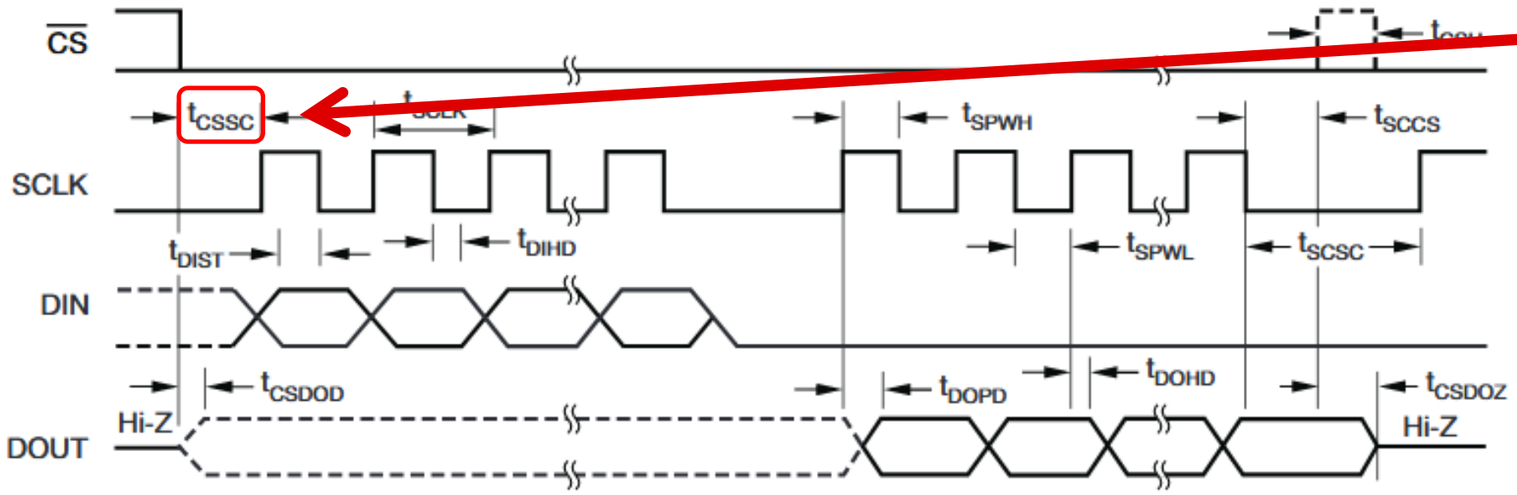



**Figure 1. Serial Interface Timing**

**$t_{CSSC}$**

CS low to first SCLK high

This time defines the time required for the CS to stay high to ensure that the device recognizes it is the peripheral.

A violation may cause the device to miss the first SCLK pulse

# SPI Timing Diagram

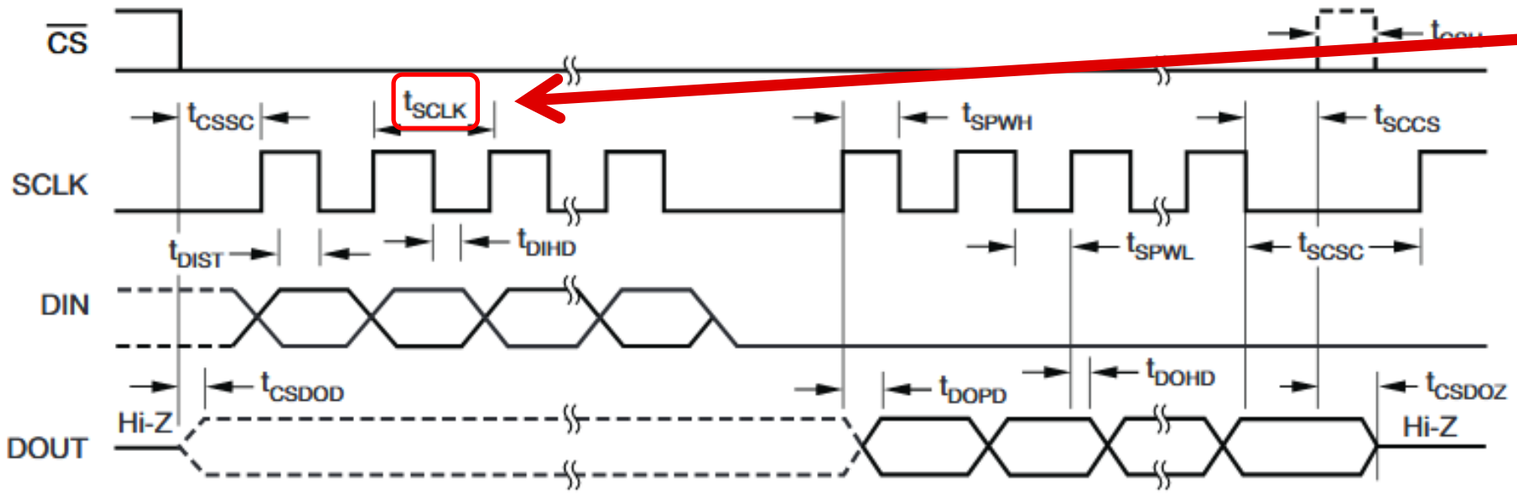



**Figure 1. Serial Interface Timing**

**$t_{SCLK}$**

The minimum time for an SCLK period

SCLKs can be sent to a device only so fast before the device fails to recognize it. This defines the minimum time for SCLK.

$1/t_{SCLK}$ is the SCLK frequency

# SPI Timing Diagram

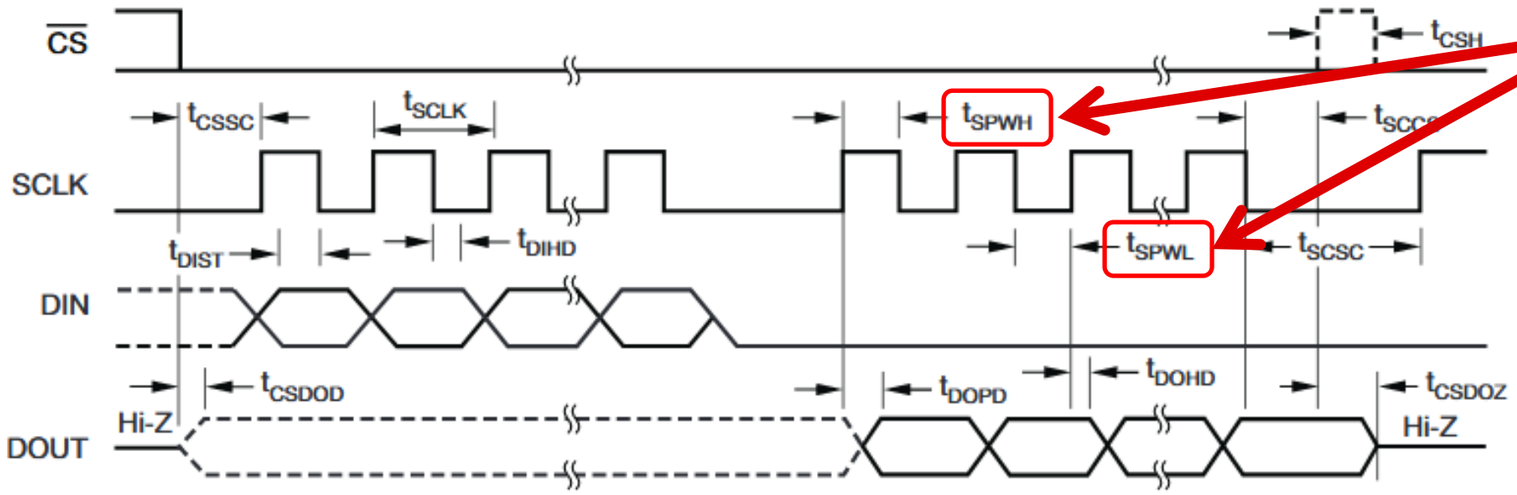



**Figure 1. Serial Interface Timing**

**$t_{SPWH}$, $t_{SPWH}$**

The minimum time for an SCLK high and the minimum time for an SCLK low

These two times with $t_{SCLK}$ define how much skew in the SCLK duty cycle is allowed

For this device, there is a maximum $t_{SPWL}$ for SPI timeout

# SPI Timing Diagram

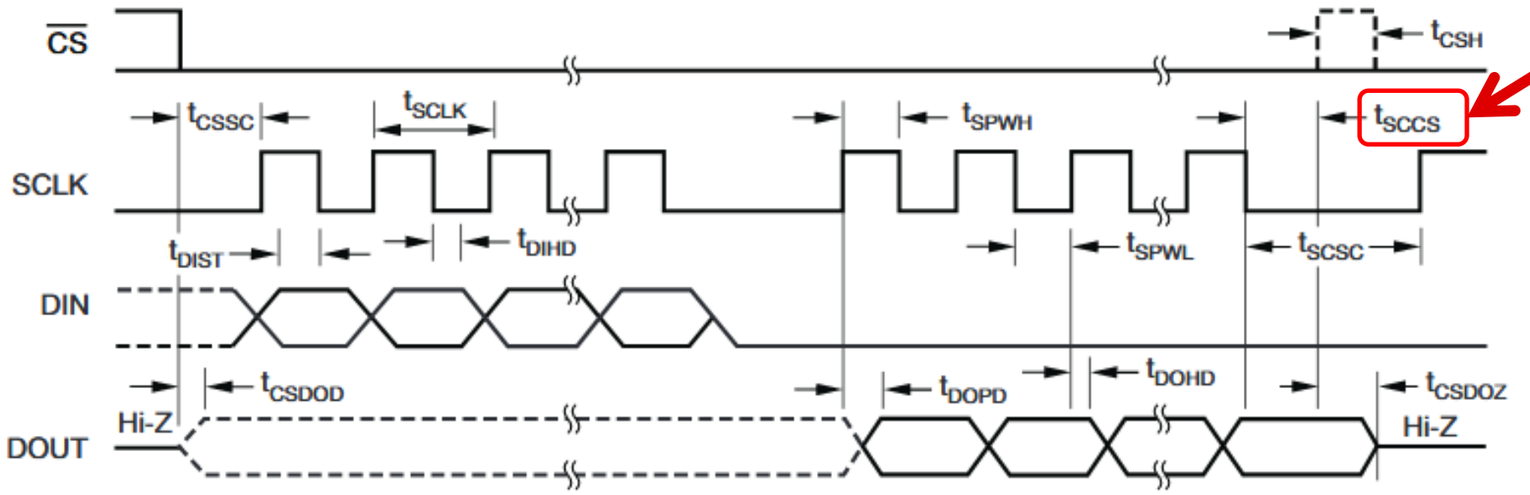



**Figure 1. Serial Interface Timing**

**$t_{SCCS}$**

Time from the falling edge of SCLK to the rising edge of CS

Because CS disables the SPI, ensure that the device receives the last bit of data before shutting down SPI communication

A violation of this could cause the device to miss the last data transmission

# SPI Timing Diagram

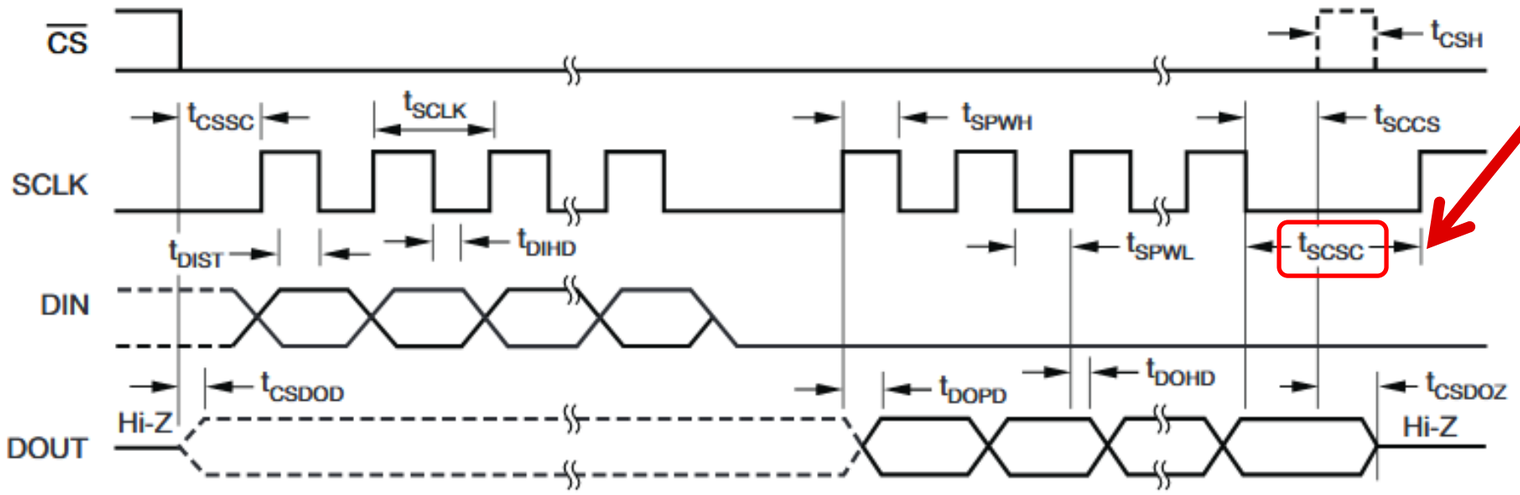



**Figure 1. Serial Interface Timing**

**$t_{SCSC}$**

Time from the falling edge of SCLK to the rising edge of SCLK in the next CS

This time is required to execute the command from one CS period, to start a new command in another CS period

# SPI Timing Diagram

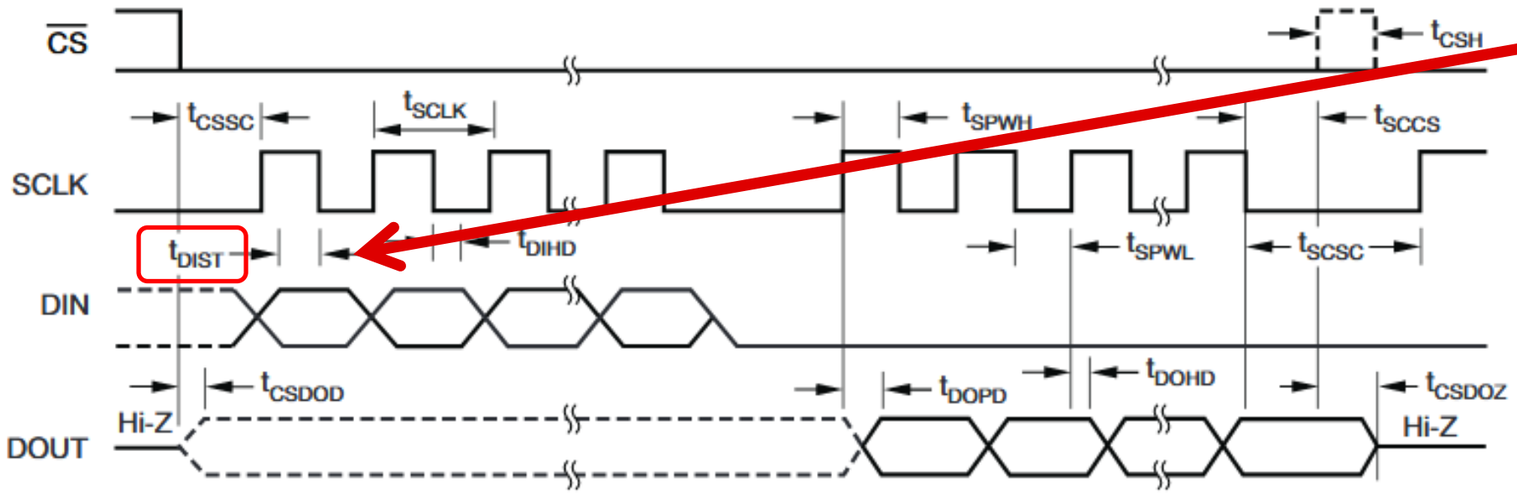



**Figure 1. Serial Interface Timing**

**$t_{DIST}$**

Setup time from the rising edge of DIN to the falling edge of SCLK

For data to be read into the device, the DIN must first be established for a time period before the SCLK falling edge.

# SPI Timing Diagram

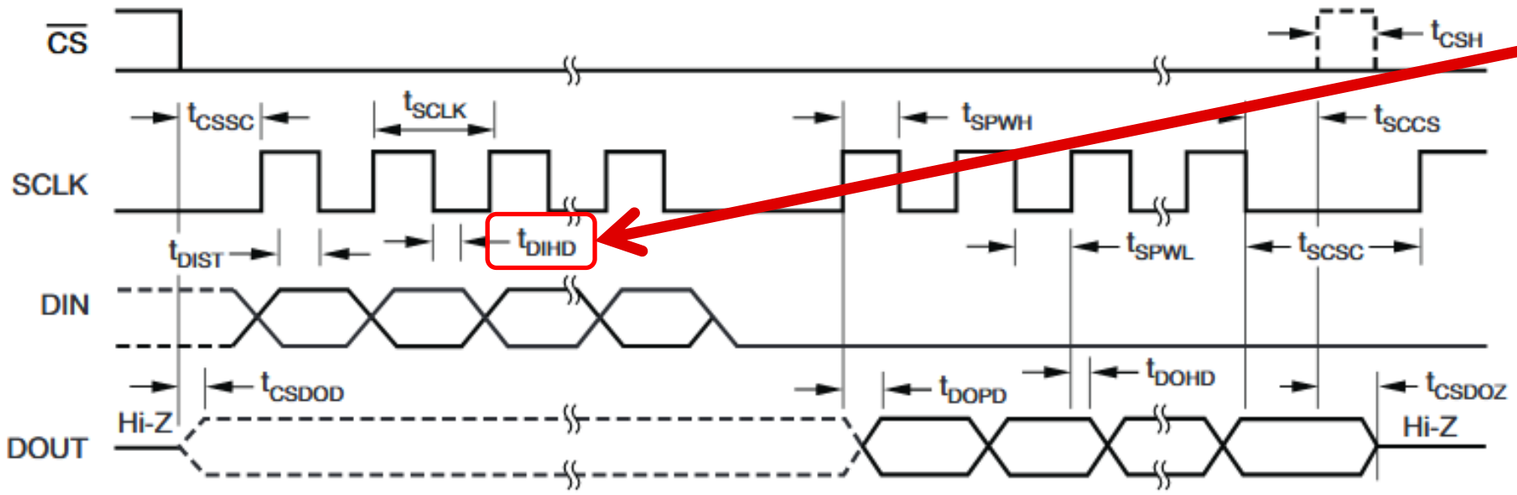



**Figure 1. Serial Interface Timing**

**$t_{DIHD}$**

Hold time from the falling edge of SCLK to the falling edge of DIN.

Once the data is set onto the DIN line, the SCLK falling edge latches the data into the device. However, there is a required time for the data to be held after the SCLK falling edge

# SPI Timing Diagram

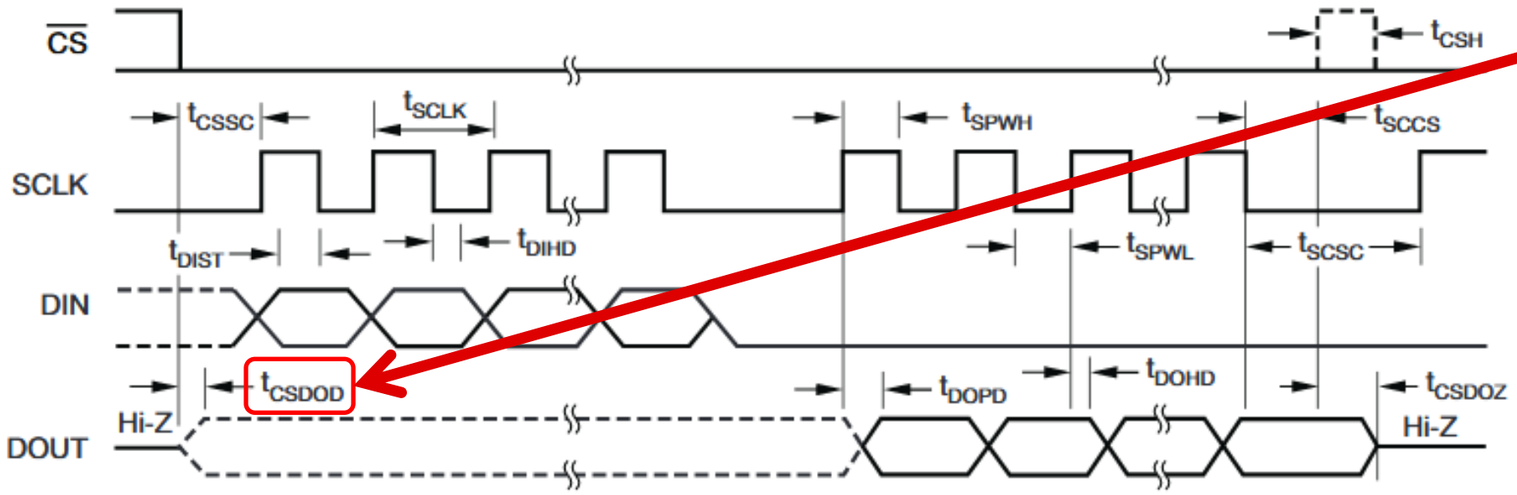



**Figure 1. Serial Interface Timing**

**$t_{CSDOD}$**

Propagation delay time from CS falling to DOUT actively driven

When CS is high, the DOUT is high impedance or Hi-Z, allowing for multiple devices on the bus to drive DOUT a device at a time.

When CS goes low, DOUT is actively driven

# SPI Timing Diagram

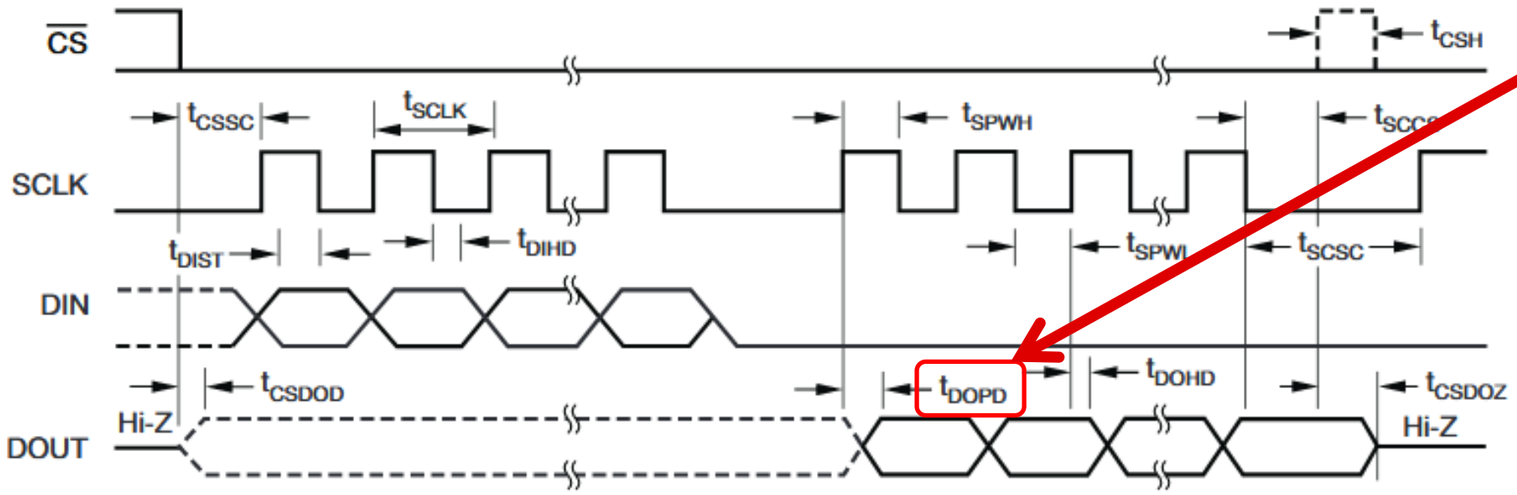



**Figure 1. Serial Interface Timing**

**$t_{DOPD}$**

Propagation delay time from rising edge of SCLK to data appearing on DOUT

SCLK is used to clock out data from the device. When SCLK is driven high, this signals to the device that data should be put on DOUT that can be clocked out on the falling edge of DOUT

# SPI Timing Diagram

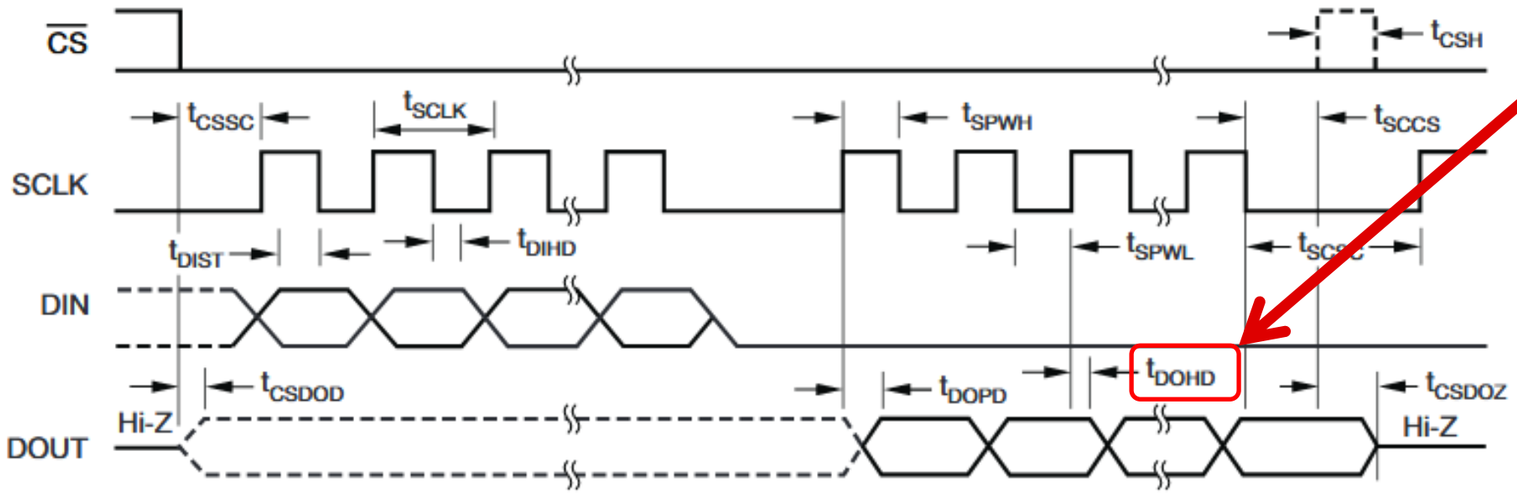



**Figure 1. Serial Interface Timing**

**$t_{DOHD}$**

Propagation delay time from rising edge of SCLK to data changing on DOUT

This defines the time for which the last data is still valid once the rising edge of SCLK occurs

# SPI Timing Diagram

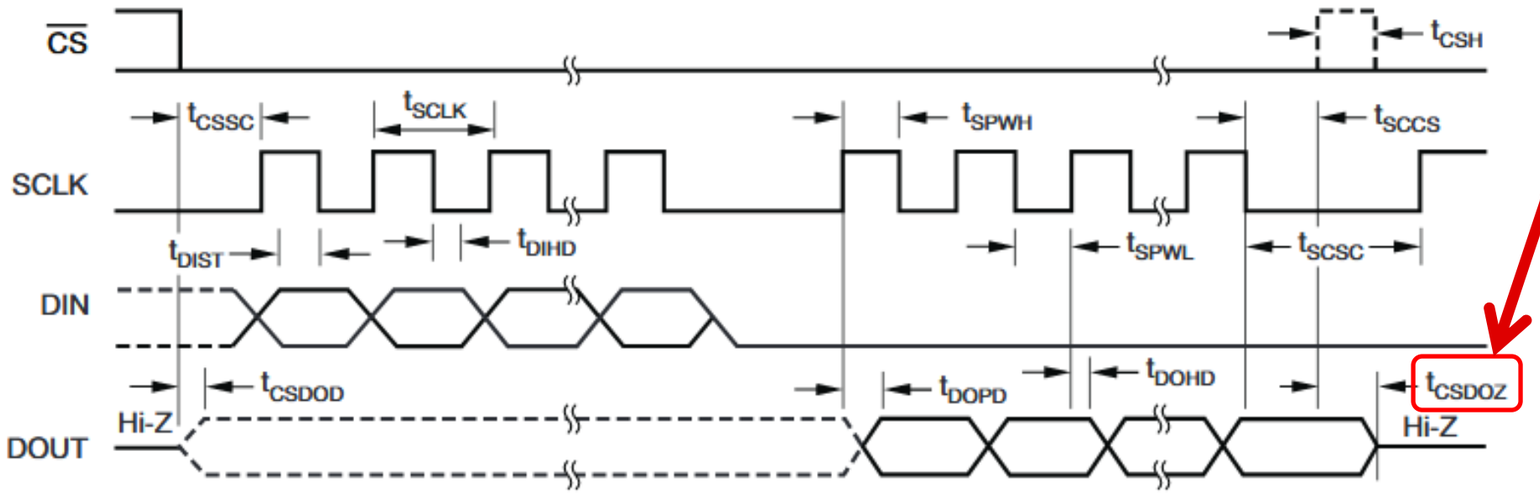



**Figure 1. Serial Interface Timing**

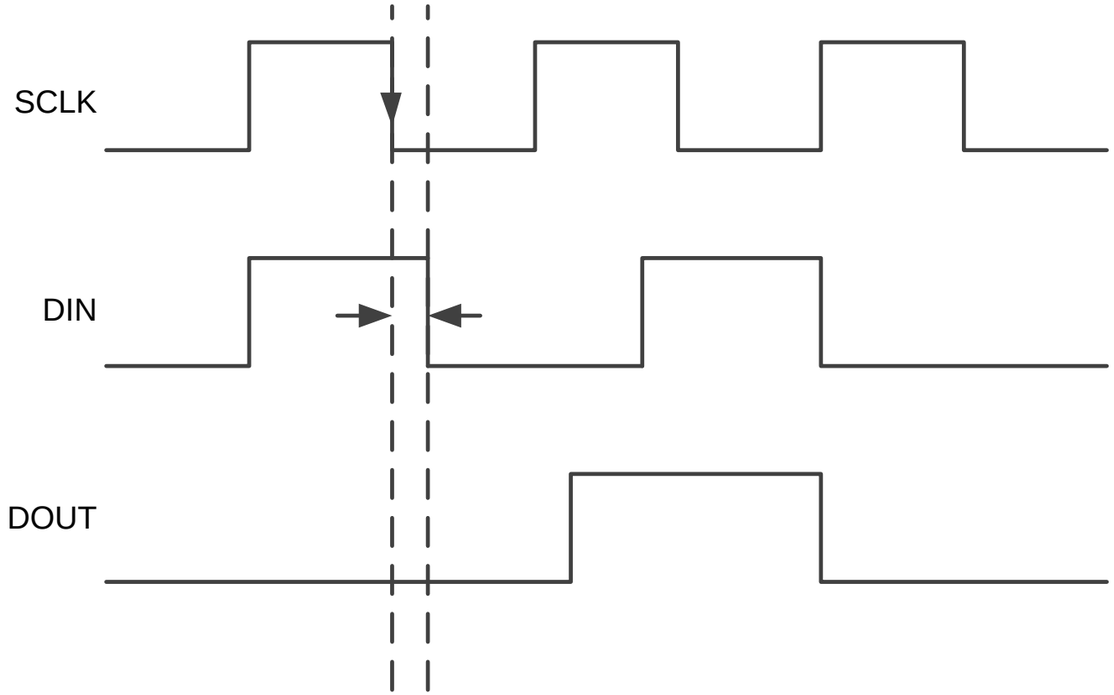
**$t_{CSDOZ}$**

Propagation delay time from rising edge of CS to DOUT becoming Hi-Z

# Thanks for your time!
# Please try the quiz.

# Quiz: Basics of SPI: Timing Diagram

1. The following diagram is CPOL = 0, CPHA = 1. Data is clocked in on the falling edge of SCLK. DIN must be stable for a time after the SCLK falling edge. This timing is an example of which timing requirement?
   a. Setup time
   b. Hold time
   c. Propagation delay
   d. None of the above



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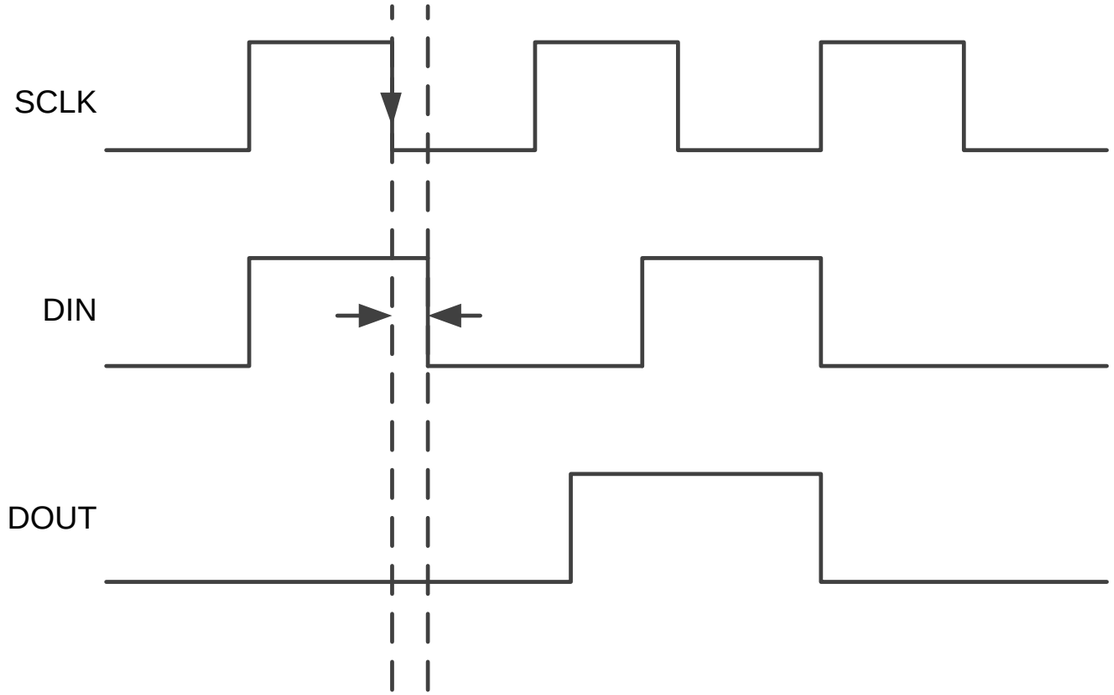

# Quiz: Basics of SPI: Timing Diagram

2. The following diagram is CPOL = 0, CPHA = 1. DIN and DOUT are read on the falling edge of SCLK. However, DOUT is set up on the rising edge of SCLK, and there may be time required for the data to arrive on DOUT. This timing is an example of which timing requirement?

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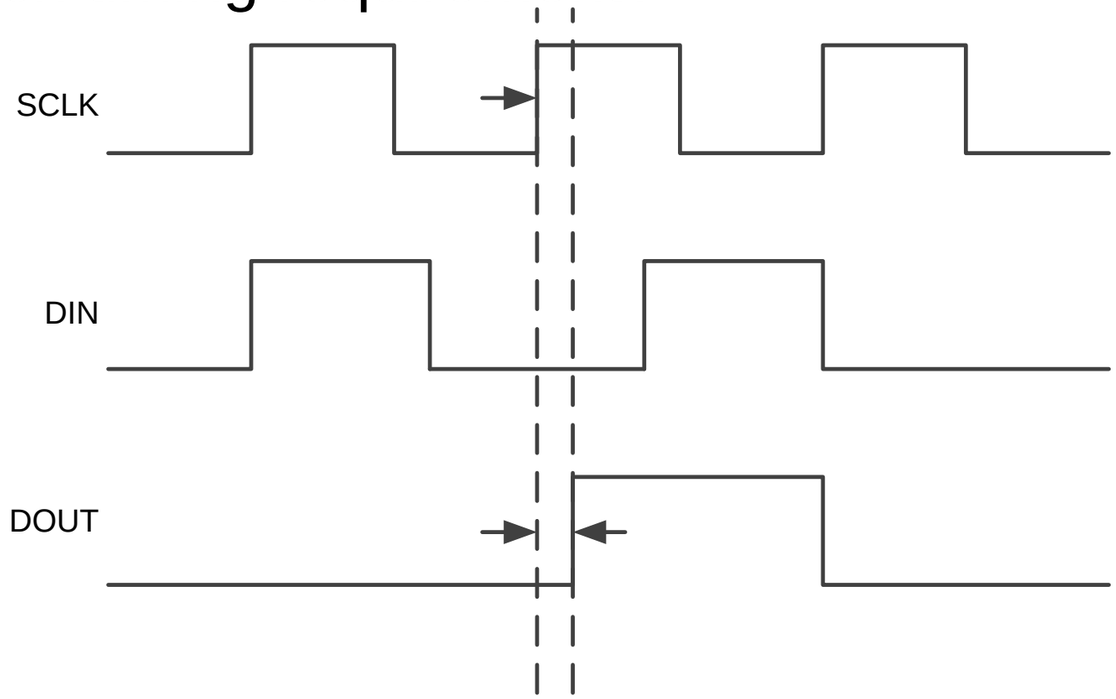

# Quiz: Basics of SPI: Timing Diagram

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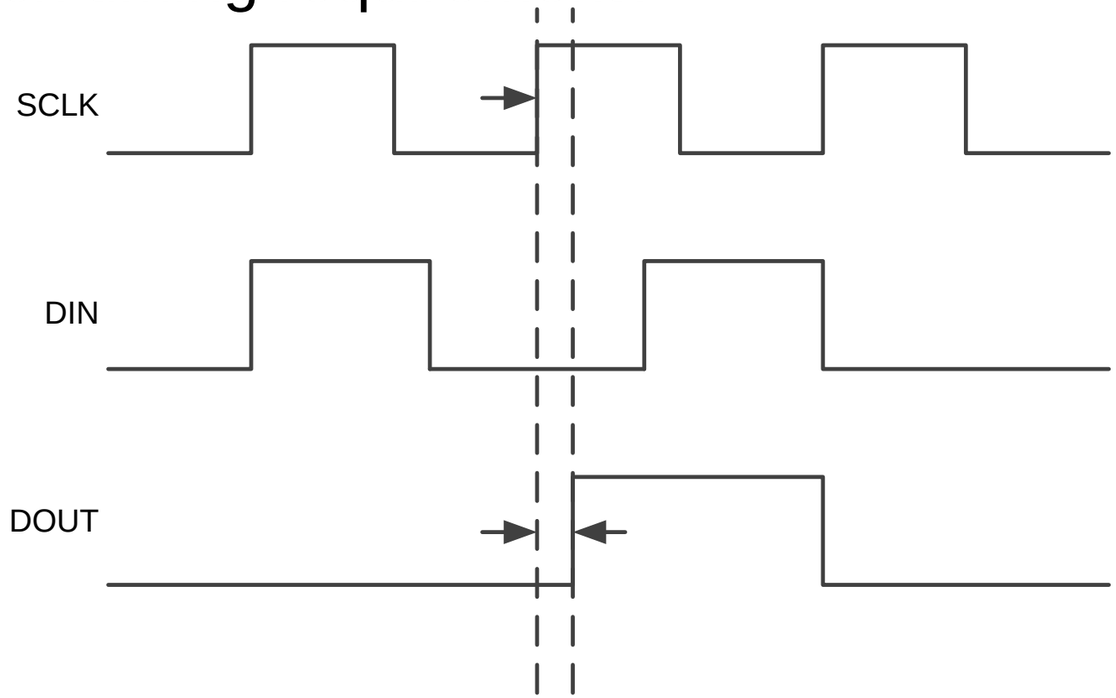
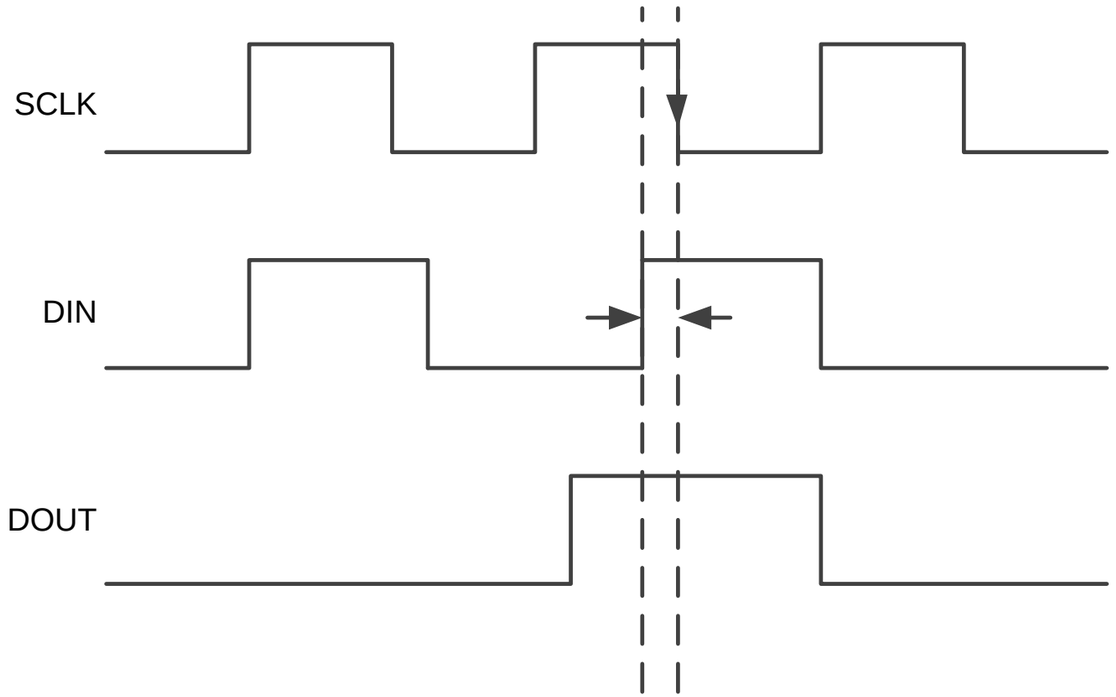


# Quiz: Basics of SPI: Timing Diagram

3. The following diagram is CPOL = 0, CPHA = 1. Data is clocked in on the falling edge of SCLK. DIN must be stable for a time before the falling edge of SCLK. This timing is an example of which timing requirement?
   a. Setup time
   b. Hold time
   c. Propagation delay
   d. None of the above



# Quiz: Basics of SPI: Timing Diagram

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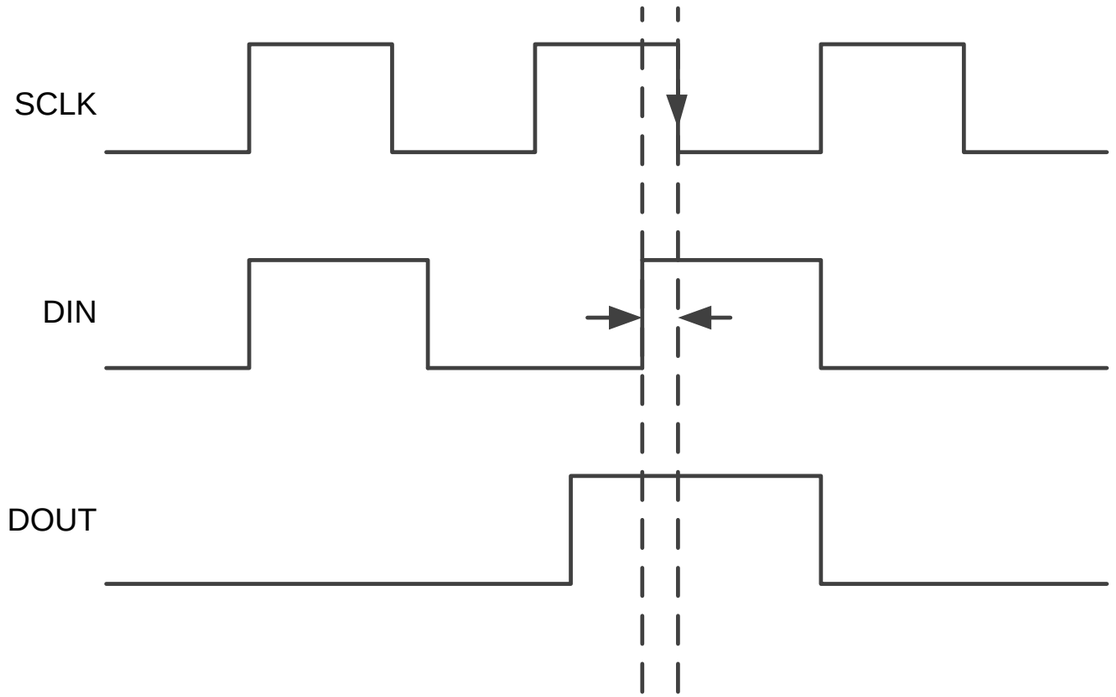
   d. None of the above



# Thanks for your time!

# Basics of SPI: Timing Requirements and Switching Characteristics

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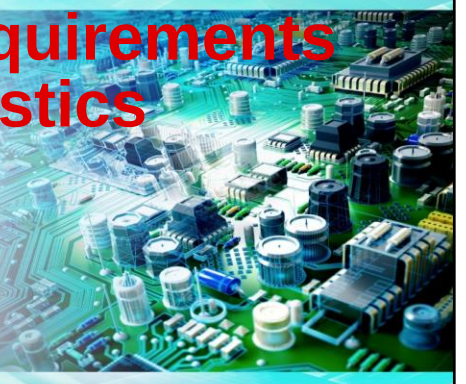
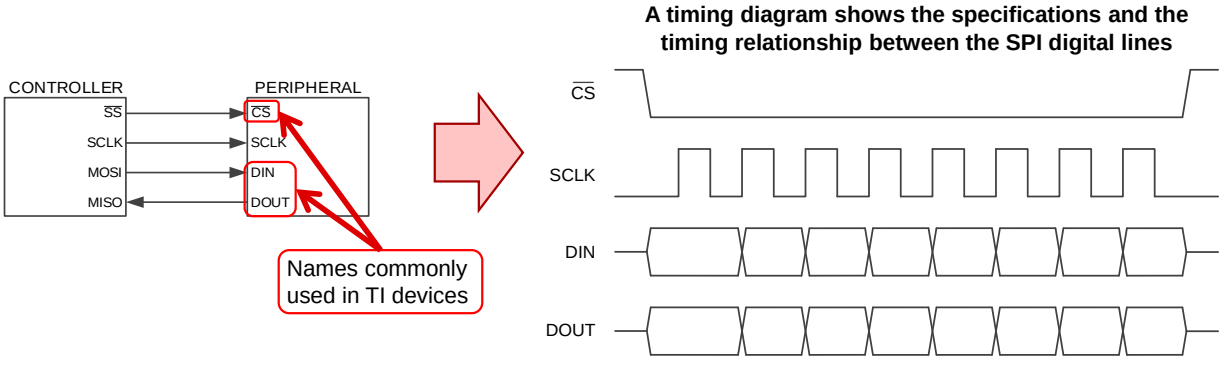




Hello, and welcome to our in-depth look at communications with precision data converters. In this video, we describe the timing requirements and switching characteristics between digital lines associated with Serial Peripheral Interface or SPI communication. We'll discuss timing and switching specifications that you may see in a datasheet. Then we'll describe an example of the timing diagram for one of TI's precision data converters.

# SPI Communication




**Violating a timing specification can cause a failure to read the data and may cause unexpected results.**



In a previous video, we discussed how data is clocked into and out of precision data converters using the four digital lines of SPI. An active low peripheral select line, commonly known as Chip Select is used to select the device for communication. A serial clock of SCLK clocks data in and out of the peripheral device to the controller. Finally data lines of MOSI and MISO, commonly named DIN and DOUT for the peripheral device are used to send the data.

For all of these digital lines, there are specifications that define the time required from the change of one digital line to another. Many of these specifications are related to the time between the changes in the data of the DIN and DOUT lines to SCLK. These specifications ensure that the data is properly clocked into and out of the digital sections of the controller and peripheral device.

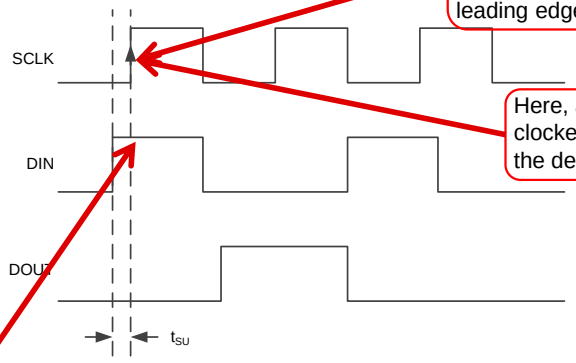
Regardless, all timing specifications must be followed to ensure that the controller and peripheral device are properly sending and receiving data. Violating a timing specification can cause failure to read the data and may cause unexpected results.

# SPI Timing: Setup Time

Setup time

Hold time

Propagation Delay




Example is SPI mode 0: SCLK idles low and data is clocked in on the leading edge of SCLK

Here, a 1 is clocked into the device

The state of DIN is read into the device at the rising edge of SCLK. To ensure the data is correctly read, DIN must be at the correct state for a setup time **before** the SCLK rises

**Setup time is the minimum time required before the clocking edge for which the data must be stable to be latched correctly**



Most timing specifications can be categorized into one of three categories. They are setup times, hold times, or propagation delays. Using this timing diagram, we show the SCLK, DIN, and DOUT of a peripheral device. Using SPI mode 0, the SCLK idles low and the data is clocked in on the rising edge of the SCLK.

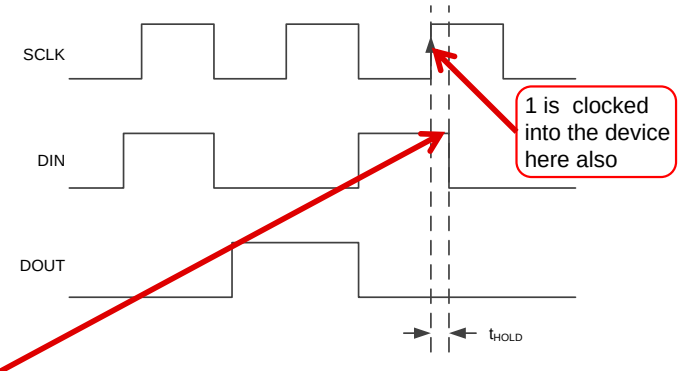
First, setup time is the time required for a data input to be stable *before* the edge of the clocking signal to be latched correctly. In the diagram, the example is SPI mode 0, where SCLK idles low and the data is clocked in on the rising edge of SCLK. DIN is set high so that at the rising edge of SCLK a 1 is clocked into the peripheral device. DIN must be set high first and it must stay high for a specific setup time so that the 1 is properly received.

# SPI Timing: Hold Time

Setup time

Hold time

Propagation Delay




Again, the state of DIN is read into the device at the rising edge of SCLK. DIN must be held at the correct state for a hold time **after** the SCLK rises

**Hold time is the minimum time required after the clocking edge for which the data must be stable to be latched correctly**



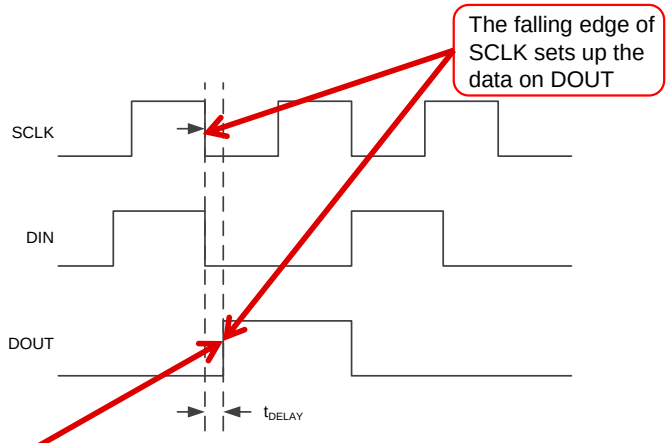
Second, hold time is the time required for a data input to be held at the proper level *after* the clocking signal. In the diagram, DIN is already set high, and then the SCLK rises to clock in the signal. DIN must stay high for a hold time *after* the clock rises to ensure that the 1 again is properly received.

# SPI Switching: Propagation Delay

Setup time

Hold time

Propagation Delay




DOUT is read by the controller at the rising edge of SCLK. However, the peripheral sets the output at the previous falling edge of SCLK. This delay from one clock event to the response is a propagation delay.

**Propagation delay is the time required for an input change to cause an output change through the digital circuitry**



Lastly, there are propagation delays. This term describes the time required for the signal from one line to change the signal from another.

In the diagram, the SCLK comes into the device, and the controller reads DOUT on the rising edge of the clock. For the peripheral device, the falling edge of the clock sets up the next data bit so that by the rising edge of the clock when the controller reads the device, the correct data is on DOUT. This delay time describes how long it takes from the SCLK falling edge to place the data on the DOUT line.

# SPI Timing

**Timing Requirements and Switching Characteristics example from the ADS1118**

Timing Requirements are typically setup times and hold times

### 7.6 Timing Requirements: Serial Interface

Over operating ambient temperature range and VDD = 2 V to 5.5 V (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{CSSC}$ | Delay time, $\overline{CS}$ falling edge to first SCLK rising edge(1) | 100 | | ns |
| $t_{SCCS}$ | Delay time, final SCLK falling edge to $\overline{CS}$ rising edge | 100 | | ns |
| $t_{CSH}$ | Pulse duration, $\overline{CS}$ high | 200 | | ns |
| $t_{SCLK}$ | SCLK period | 250 | | ns |
| $t_{SPWH}$ | Pulse duration, SCLK high | 100 | | ns |
| $t_{SPWL}$ | Pulse duration, SCLK low(2) | 100 | | ns |
| | | | 28 | ms |
| $t_{DIST}$ | Setup time, DIN valid before SCLK falling edge | 50 | | ns |
| $t_{DIHD}$ | Hold time, DIN valid after SCLK falling edge | 50 | | ns |
| $t_{DOHD}$ | Hold time, SCLK rising edge to DOUT invalid | 0 | | ns |

(1) $\overline{CS}$ can be tied low permanently in case the serial bus is not shared with any other device.
(2) Holding SCLK low longer than 28 ms resets the SPI interface.

Switching Characteristics are typically propagation delays

### 7.7 Switching Characteristics: Serial Interface

Over operating ambient temperature range (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{CSDOD}$ | Propagation delay time, $\overline{CS}$ falling edge to DOUT driven | DOUT load = 20 pF \|\| 100 kΩ to GND | | | 100 | ns |
| $t_{DOPD}$ | Propagation delay time, SCLK rising edge to valid new DOUT | DOUT load = 20 pF \|\| 100 kΩ to GND | 0 | | 50 | ns |
| $t_{CSDOZ}$ | Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance | DOUT load = 20 pF \|\| 100 kΩ to GND | | | 100 | ns |



Here we can take an in-depth look at SPI timing from an example datasheet. Using the ADS1118 precision ADC, two tables show the Timing Requirements and the Switching Characteristics. Typically, timing requirements show setup and hold times for the SPI communications and the switching characteristics will show propagation delays. These tables will give minimum and maximum times for different characteristics shown in a timing diagram.

# SPI Timing Diagram

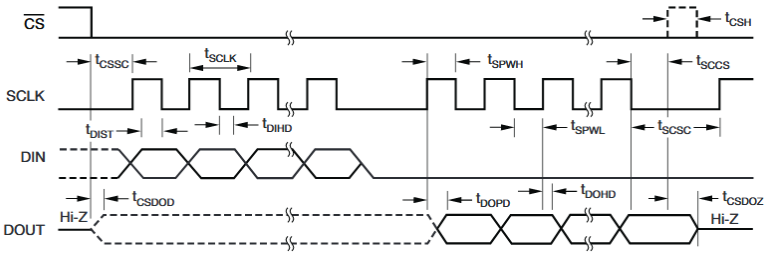



**Figure 1. Serial Interface Timing**

| Timing diagram for the ADS1118 |
| --- |
| Device uses SPI Mode 1: SCLK idles low, data clocked in at falling edge of SCLK |
| Boxes for DIN and DOUT are high or low data |
| Arrows enclose timing specifications |



Continuing with the example, here is the timing diagram. We can go through the specifications and explain how to read them. The timing diagram shows specific timing requirements between the different digital lines. For all digital communications, this timing must be followed, or the device may not recognize commands, fail to understand the configuration settings, or properly output data.

We'll cover each of these specifications, and explain what they mean.

# SPI Timing Diagram

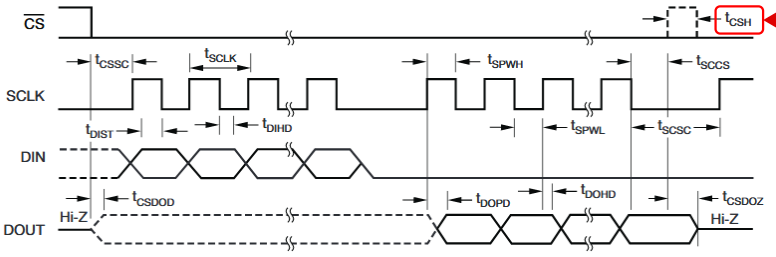



**Figure 1. Serial Interface Timing**

**$t_{CSH}$**

Minimum pulse duration, CS high

This time defines the time required for the CS to stay high to ensure that the device has reset the SPI communications.



tCSH is the hold time of chip select. This is the minimum amount of time that chip select can be held high that ensures that the device recognizes that the chip select has been set high and low again. Here, it does not appear to be a hold time because it does not come before a clock signal in the diagram. However, this timing is internal and defines a hold time based on latching the CS signal to an internal clock.

# SPI Timing Diagram

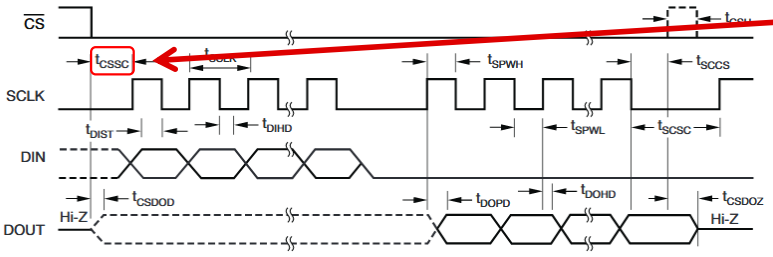



**Figure 1. Serial Interface Timing**

**tcssc**

CS low to first SCLK high

This time defines the time required for the CS to stay high to ensure that the device recognizes it is the peripheral.

A violation may cause the device to miss the first SCLK pulse



tCSSC is the minimum time required between chip select transitioning low and the first SCLK. As chip select is taken low, it still takes a small amount of time for the device to determine that it is the active peripheral. This also allows for time to setup data that the device needs to send out on DOUT at the first SCLK rising edge pulse.

# SPI Timing Diagram

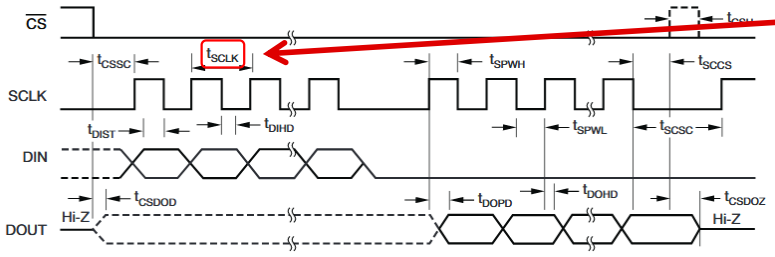



**Figure 1. Serial Interface Timing**

| $t_{SCLK}$ |
| --- |
| The minimum time for an SCLK period |
| SCLKs can be sent to a device only so fast before the device fails to recognize it. This defines the minimum time for SCLK. |
| $1/t_{SCLK}$ is the SCLK frequency |



tSCLK is the SCLK period. SCLK must have a minimum period to ensure proper digital timing. Transistors and logic gates can't be clocked infinitely fast, so there is a limit to how fast data can be clocked out.

# SPI Timing Diagram

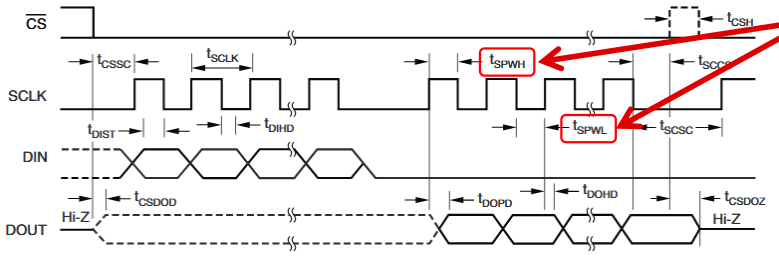



**Figure 1. Serial Interface Timing**

**$t_{SPWH}$, $t_{SPWH}$**

The minimum time for an SCLK high and the minimum time for an SCLK low

These two times with $t_{SCLK}$ define how much skew in the SCLK duty cycle is allowed

For this device, there is a maximum $t_{SPWL}$ for SPI timeout



tSPWH and tSPWL are the minimum time periods for the SCLK pulse high and low. This is similar to the total minimum SCLK period, but it really describes the acceptable duty cycle and skew of the SCLK signal.

For this timing specification, there is an additional limit. The timing requirement table lists a maximum tSPWL time of 28ms. This maximum time comes from a timeout built into the SPI communications of this device.

# SPI Timing Diagram

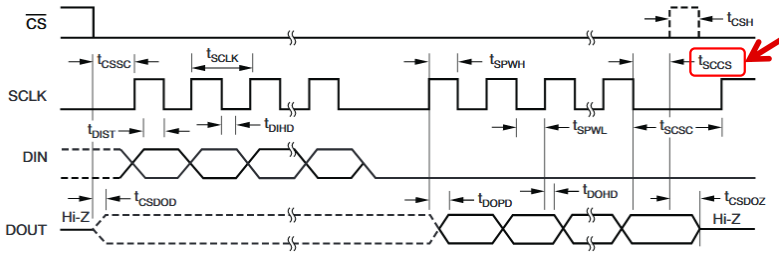



**Figure 1. Serial Interface Timing**

**tSCCS**

Time from the falling edge of SCLK to the rising edge of CS

Because CS disables the SPI, ensure that the device receives the last bit of data before shutting down SPI communication

A violation of this could cause the device to miss the last data transmission



tSCCS is the minimum time from the last SCLK falling edge to the rising edge of chip select. This is a specification required for clocking in data to the device. Because chip select disables the SPI communication, any data must be clocked into the device with the falling edge of SCLK before chip select rises. It is a hold time for the data with SCLK and a setup time for the chip select to the device's internal clock.

# SPI Timing Diagram

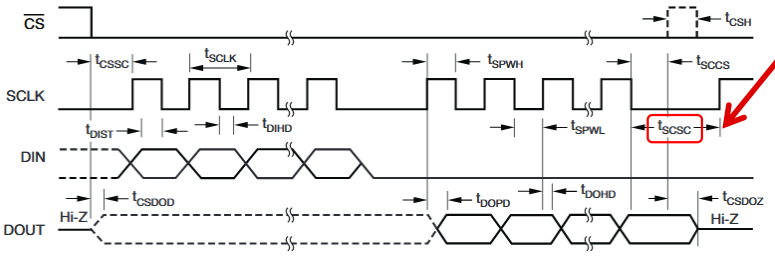



**Figure 1. Serial Interface Timing**

**tscsc**

Time from the falling edge of SCLK to the rising edge of SCLK in the next CS

This time is required to execute the command from one CS period, to start a new command in another CS period



tSCSC is the time required between the last falling edge of SCLK from one command to the next rising edge of SCLK for the next command. For the device, there is some time required to parse and execute a command in one chip select frame before being able to take another command from another chip select frame.

# SPI Timing Diagram

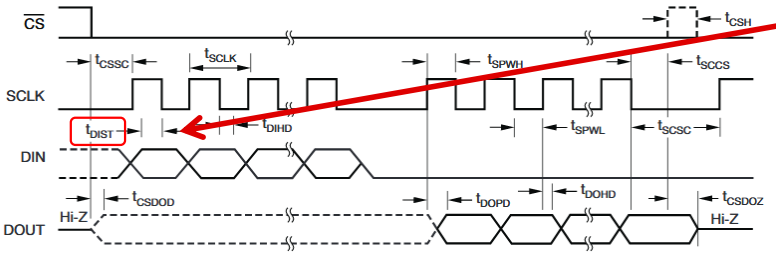



**Figure 1. Serial Interface Timing**

**$t_{DIST}$**

Setup time from the rising edge of DIN to the falling edge of SCLK

For data to be read into the device, the DIN must first be established for a time period before the SCLK falling edge.



tDIST is the setup time for the DIN data. In this diagram, the communication uses SPI mode 1, where the SCLK idles low and data are clocked in on the falling edge of SCLK. Here, the DIN is typically set up on the rising edge of SCLK, but this defines a minimum time that DIN must be valid before the falling edge of SCLK.

Again, this device is SPI mode 1, where the data is clocked in at the falling edge of SCLK. The setup time is the time required for DIN to be stable, before the active falling SCLK edge.

# SPI Timing Diagram

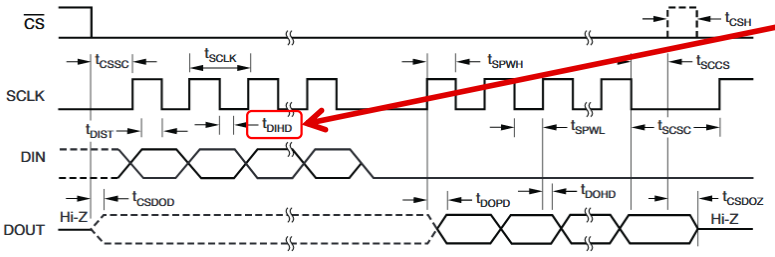



**Figure 1. Serial Interface Timing**

**$t_{DIHD}$**

Hold time from the falling edge of SCLK to the falling edge of DIN.

Once the data is set onto the DIN line, the SCLK falling edge latches the data into the device. However, there is a required time for the data to be held after the SCLK falling edge



tDIHD is the hold time for the DIN data. When the data is clocked in on the falling edge of SCLK, DIN must be stable from the setup time before and the hold time after the SCLK falling edge.

# SPI Timing Diagram

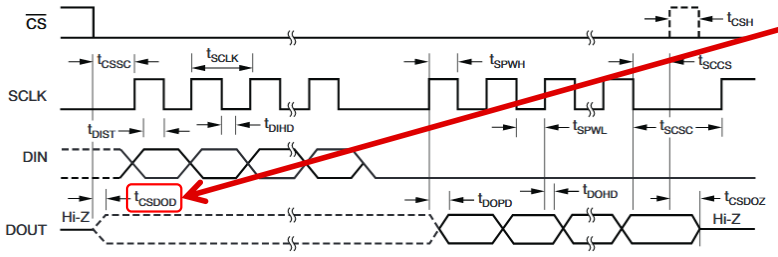



**Figure 1. Serial Interface Timing**

| $t_{CSDOD}$ |
| --- |
| Propagation delay time from CS falling to DOUT actively driven |
| When CS is high, the DOUT is high impedance or Hi-Z, allowing for multiple devices on the bus to drive DOUT a device at a time. |
| When CS goes low, DOUT is actively driven |



tCSDOD is the time from the falling edge of chip select to the enabling of DOUT. When chip select is high, the DOUT of the peripheral device is high impedance, or Hi-Z. This prevents an inactive peripheral device from trying to drive the DOUT line. When chip select is driven low, DOUT is driven by the active peripheral. tCSDOD shows the propagation delay from the chip select going low to when the DOUT is active.

# SPI Timing Diagram

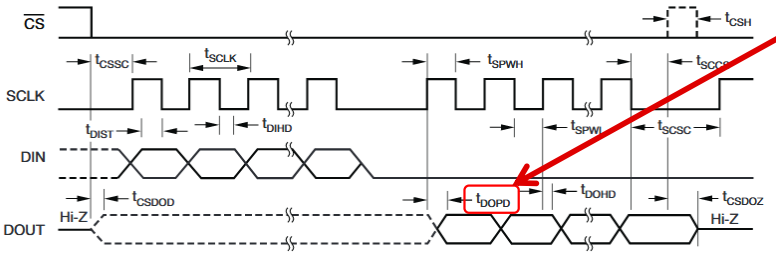



**Figure 1. Serial Interface Timing**

**$t_{DOPD}$**

Propagation delay time from rising edge of SCLK to data appearing on DOUT

SCLK is used to clock out data from the device. When SCLK is driven high, this signals to the device that data should be put on DOUT that can be clocked out on the falling edge of DOUT



tDOPD is the maximum propagation delay time from the rising edge of SCLK to the data appearing on DOUT. Again, data is clocked out by the controller on the falling edge of SCLK, so the rising edge of SCLK is used by the device to send data to DOUT.

# SPI Timing Diagram

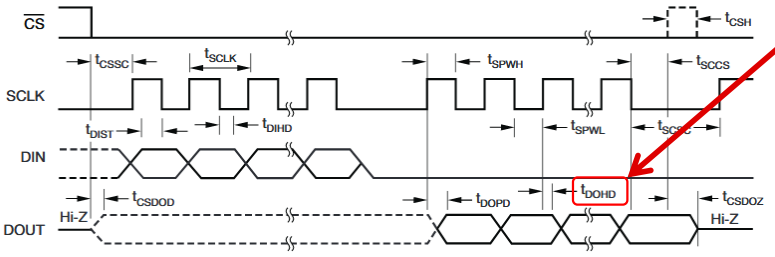



**Figure 1. Serial Interface Timing**

**$t_{DOHD}$**

Propagation delay time from rising edge of SCLK to data changing on DOUT

This defines the time for which the last data is still valid once the rising edge of SCLK occurs



tDOHD is the propagation delay time from the SCLK rising edge to when DOUT becomes invalid. Again, DOUT is set up on the rising edge of SCLK so that it can be read out on the falling edge of SCLK. However, if you choose to read the data, you have until tDOHD after the next rising edge of SCLK to read the data.

This specification isn't important if the data is read on the falling edge of SCLK.

# SPI Timing Diagram

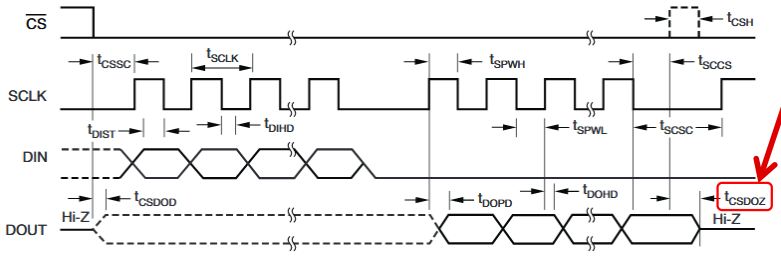


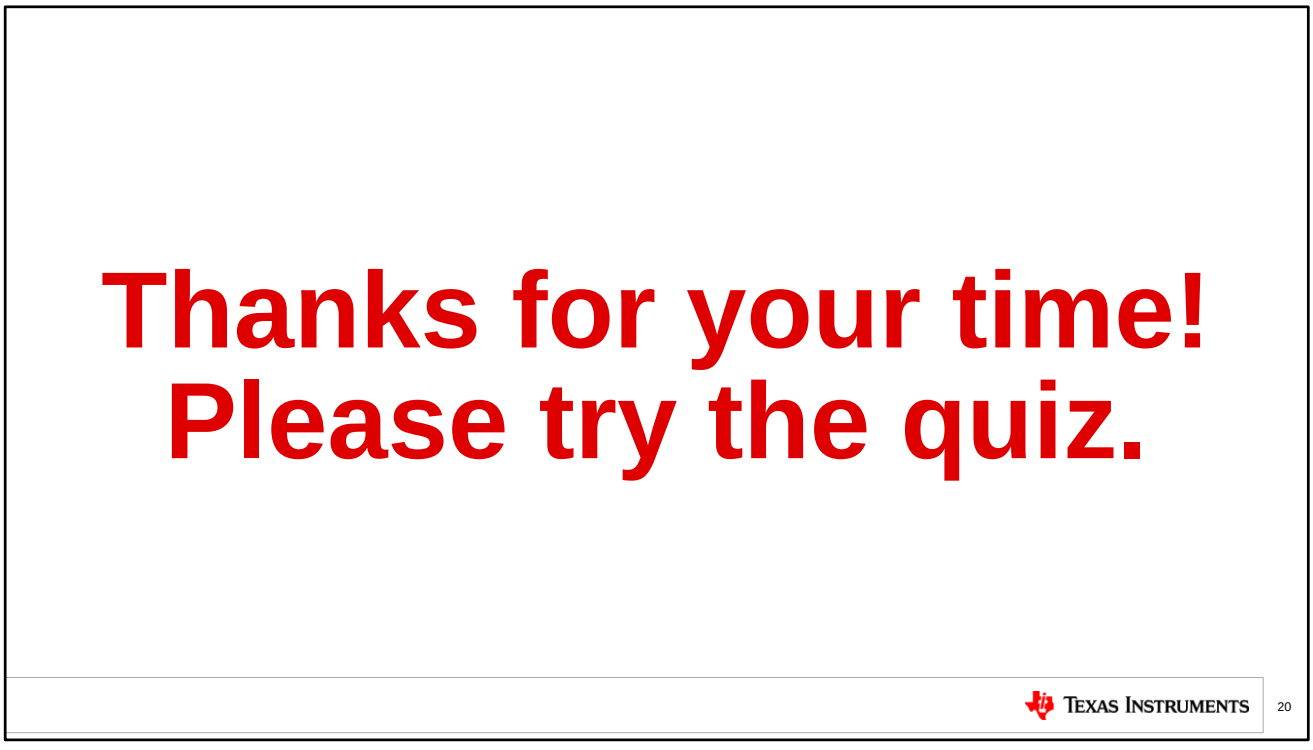

**Figure 1. Serial Interface Timing**

**$t_{CSDOZ}$**

Propagation delay time from rising edge of CS to DOUT becoming Hi-Z



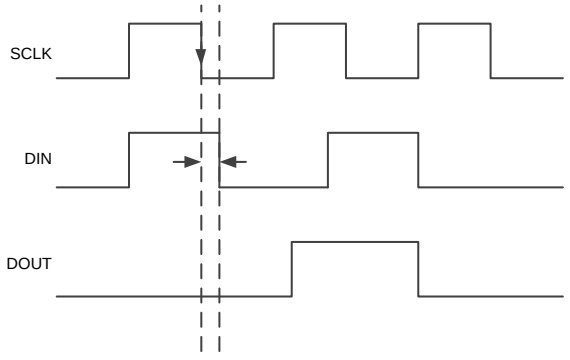
tCSDOZ is the time from the rising edge of chip select to when DOUT returns to high impedance. Similar to tCSDOD, this is important when there are peripheral multiple devices on the SPI bus.




That concludes this video – thank you for watching! Please try the quiz to check your understanding of this video's content.

# Quiz: Basics of SPI: Timing Diagram

1. The following diagram is CPOL = 0, CPHA = 1. Data is clocked in on the falling edge of SCLK. DIN must be stable for a time after the SCLK falling edge. This timing is an example of which timing requirement?
   a. Setup time
   b. Hold time
   c. Propagation delay
   d. None of the above



# Quiz: Basics of SPI: Timing Diagram

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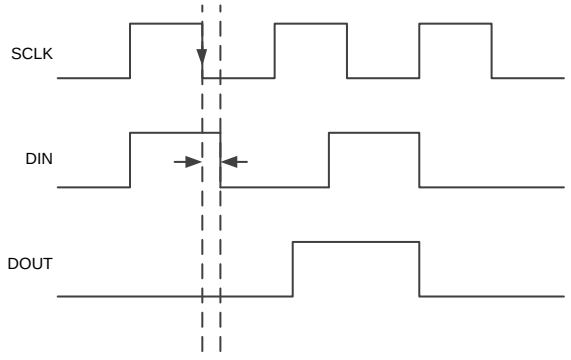
   a. Setup time
   b. Hold time
   c. Propagation delay
   d. None of the above

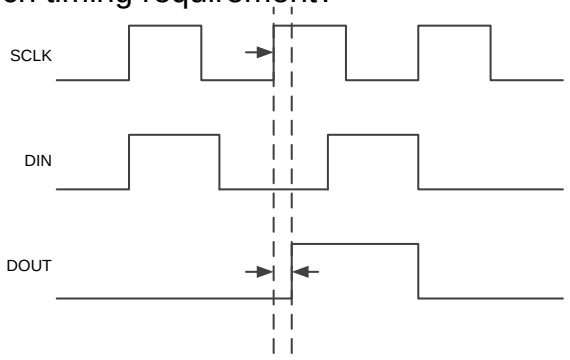





B. Hold time. The SCLK is clocks in data on a falling edge. Here we see that we want to clock in DIN to the peripheral on the SCLK falling edge. This timing diagram shows the amount of time that is required to hold DIN after the falling edge of SCLK.

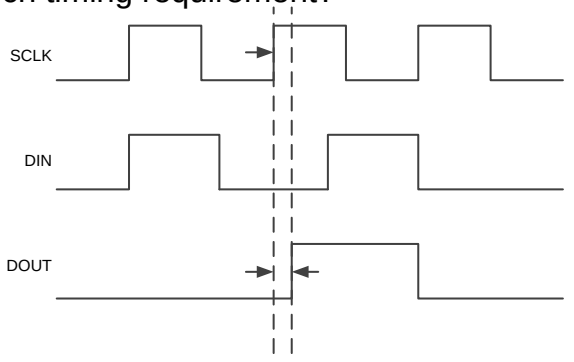
# Quiz: Basics of SPI: Timing Diagram

2. The following diagram is CPOL = 0, CPHA = 1. DIN and DOUT are read on the falling edge of SCLK. However, DOUT is set up on the rising edge of SCLK, and there may be time required for the data to arrive on DOUT. This timing is an example of which timing requirement?
   a. Setup time
   b. Hold time
   c. Propagation delay
   d. None of the above



# Quiz: Basics of SPI: Timing Diagram

2. The following diagram is CPOL = 0, CPHA = 1. DIN and DOUT are read on the falling edge of SCLK. However, DOUT is set up on the rising edge of SCLK, and there may be time required for the data to arrive on DOUT. This timing is an example of which timing requirement?
   a. Setup time
   b. Hold time
   c. Propagation delay
   d. None of the above

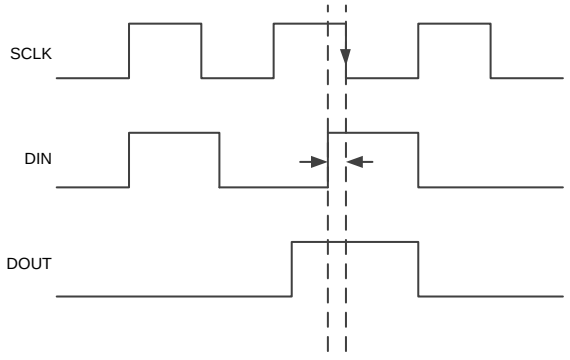





C. Propagation delay. In this diagram data is set up on the rising edge of the SCLK and clocked in the peripheral or controller on the falling edge. Here, the SCLK rising edge tells the peripheral to get the data out to DOUT so that it can be latched into the controller on the falling edge. This is a propagation delay showing the amount of time required from the rising edge of SCLK to get data out on DOUT.

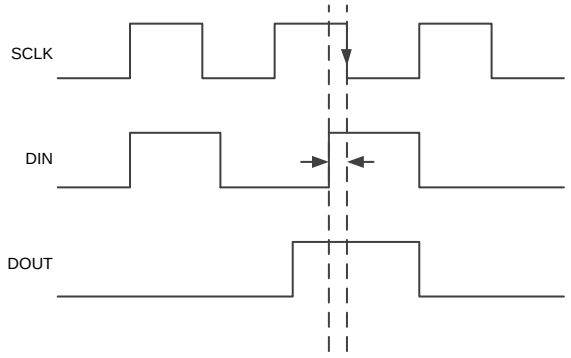
# Quiz: Basics of SPI: Timing Diagram

3. The following diagram is CPOL = 0, CPHA = 1. Data is clocked in on the falling edge of SCLK. DIN must be stable for a time before the falling edge of SCLK. This timing is an example of which timing requirement?
   a. Setup time
   b. Hold time
   c. Propagation delay
   d. None of the above



# Quiz: Basics of SPI: Timing Diagram

3. The following diagram is CPOL = 0, CPHA = 1. Data is clocked in on the falling edge of SCLK. DIN must be stable for a time before the falling edge of SCLK. This timing is an example of which timing requirement?
   a. Setup time
   b. Hold time
   c. Propagation delay
   d. None of the above






A. Setup time. Data is latched on the falling edge of SCLK. This setup time defines how much time is required to that the DIN is set and stable before the falling edge of SCLK.

# Thanks for your t