

# Amplifier Designer

**Stealth Release**

# WEBENCH® Amplifier Designer

- Currently in Stealth Release
- Design OpAmp circuits in a few minutes
- Currently supporting Non-inverting and Inverting topologies (more planned)
- Access from <http://webench.ti.com/> and click on the Amplifier Designer link

## Signal Chain and Clock Design

Clock Architect

Filter Designer

Amplifier Designer

Temp SensorEval Software

Voltage Reference Selector

Capacitive Sensing Designer

Interface Designer

Inductive Sensing Designer

Sensor AFE & Sensor Designer

Medical AFE Designer

Sensor AFE Tools

WEBENCH® Designer *My Designs*

Filters Amps

Amplifier Topology

Non-inverting

Inverting

Expected Temperature Range

Temp Min  °C

Temp Max  °C

Start Design

# WEBENCH® Amplifier Designer

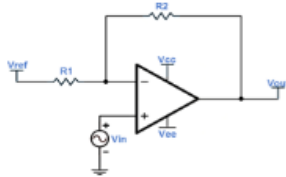
- Access from the Product Folder
- Choose the topology
- Choose the power supply requirements, including tolerances
- Select the  $V_{in}$  requirements
- Select the  $V_{out}$  requirements
- Click on Open Design – Launches directly into the design for the product
- Over 600 products currently available

WEBENCH® OPA348

Amplifier Topology

Non-inverting

Inverting



Desired Power Supply Voltage

Positive Supply (Vcc):	<input type="text" value="5.0"/>	V
Positive Supply Tolerance:	<input type="text" value="5"/>	%
Negative Supply (Vee):	<input type="text" value="0.0"/>	V
Negative Supply Tolerance:	<input type="text" value="5"/>	%

Allowable Power Supply (Vcc-Vee) = 2.1 to 5.5 V

Desired Input and Output Requirements

	Min		Max	
$V_{in}$	<input type="text" value="2.0"/>	V	<input type="text" value="3.0"/>	V
$V_{out}$	<input type="text" value="1.5"/>	V	<input type="text" value="3.5"/>	V

Minimum Temperature = -40.0 °C  
Maximum Temperature = 125.0 °C

[Open Design](#)

[What are WEBENCH tools?](#)

# WEBENCH® Amplifier Designer



New

## AMPLIFIER DESIGNER REQUIREMENTS

Power LED LED Architect Power Architect FPGA/µP HotSwap Simple Switcher Filters Clocks Load Switch Interface DDR Power Sequencers Battery Chargers Amplifiers

Select a topology and supply option and specify temperature range. Click on the 'Start Amplifier Design' button to create a design.

Start Amplifier Design

### Topology

- General Inverting Amplifier
- General Non-Inverting Amplifier

### Supply Option

- Dual Supply
- Single Supply

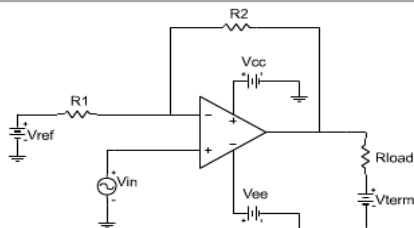
### Expected Temperature Range

Min: -20 C

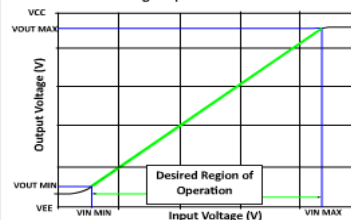
Max: 70 C

### General Non-Inverting Amplifier

The NonInverting Amplifier multiplies the input voltage ( $V_{in}$ ) by the desired positive gain, and subtracts a voltage proportional to the applied reference voltage.



### Noninverting Amplifier Transfer Characteristic



$$V_{out} = V_{in} \left(1 + \frac{R_2}{R_1}\right) - V_{ref} \left(\frac{R_2}{R_1}\right)$$

Start Amplifier Design

Click on Start Amplifier Design to launch the tool

# WEBENCH® Amplifier Designer



## AMPLIFIER DESIGNER REQUIREMENTS

### Desired Power Supply Voltage

Dual Supply     Single Supply

Positive Supply(Vcc):  V    Positive Supply Tolerance:  %

Negative Supply(Vee):  V    Negative Supply Tolerance:  %

### Desired Input and Output Requirements

Input Voltage Limits, Output Voltage Limits    Vin Min:  V

Input Voltage Limits, Gain    Vin Max:  V

Input Voltage Range, Output Voltage Range    Vout Min:  V

Input Voltage Range, Gain    Vout Max:  V

---

Vin Min:	-2 V	Vout Min:	-4 V
Vin Max:	2 V	Vout Max:	4 V
Vin pk-pk:	4 V	Vout pk-pk:	8 V
Vin Midpoint:	0 V	Vout Midpoint:	0 V

Closed Loop Gain: 2 V/V    Recommended Vref: 0 V

### Output Load

Output Current    Max Sink Current:  mA

Resistive Load    Max Source Current:  mA

### Desired Closed Loop Bandwidth

Small signal:  kHz

[Create Amplifier Design](#)

### General Non-Inverting Amplifier

### DC Transfer Characteristic

Enter your Desired Input and Output Requirements

Enter your Output Load and Closed Loop Bandwidth

Information will update as changes are made.

Click on Create Amplifier Design

# WEBENCH® Amplifier Designer

A list of choices is shown

Choices can be updated by changing Design Criteria, Optimizer, or Refine Results

Solutions may be searched by part number or ordered by column sorting.

Once a choice is made, click on Open Design

Back New Visualizer

### AMPLIFIER DESIGNER VISUALIZER

**Design Criteria**

Topology: Non-inverting

Vin Min: -2 V    Vout Min: -4 V  
 Vin Max: 2 V    Vout Max: 4 V

Closed Loop Gain: 2 V/V  
 Voltage Reference: 0 V  
 Closed Loop Bandwidth: 10 KHz

Edit Inputs

**Schematic**

**Components**

OpAmp IC: OPA2188AID  
 R1: 7699 ohms  
 R2: 7699 ohms

**Optimizer**

Very Important: Precision  
 Important: Noise  
 Less Important: Temp Drift

**Refine Results**

Package Group: All  
 No. of Channels: All  
 Shutdown Pin:

---

Solutions

Part	Create	Simulation	No. of Channels	Package	Amplifier Gain Bandwidth Product (MHz)	Small Signal Bandwidth (MHz)	Full Power Bandwidth (kHz)	Precision (mVrms)	Total Output Noise (uVrms)	Output Temperature Delta (typ, mV)	IC Supply Current(mA)	Output Offset (mV)	Max Power Supply (V)	Min Power Supply (V)	1k Price (USD)
OPA2188AID	Open Design		2	SOIC	2	1	12.73	0.05	29.55	0.00539	0.385	0.012	36	4	\$1.70
OPA2188AIDGKT	Open Design		2	MSOP	2	1	12.73	0.05	29.55	0.00539	0.385	0.012	36	4	\$1.65
OPA2188AIDR	Open Design		2	SOIC	2	1	12.73	0.05	29.55	0.00539	0.385	0.012	36	4	\$1.40
OPA2234U	Open Design		2	SOIC	0.35	0.17	3.18	0.43	27.54	0.09	0.25	0.08	36	2.7	\$3.02
OPA234U	Open Design		1	SOIC	0.35	0.17	3.18	0.43	27.54	0.09	0.25	0.08	36	2.7	\$1.91
OPA234E/250	Open Design		1	MSOP	0.35	0.17	3.18	0.53	27.54	0.09	0.25	0.2	36	2.7	\$1.85
OPA2234UA	Open Design		2	SOIC	0.35	0.17	3.18	0.89	27.54	0.09	0.25	0.08	36	2.7	\$2.52
OPA4234UA	Open Design		4	SOIC	0.35	0.17	3.18	0.89	27.54	0.09	0.25	0.08	36	2.7	\$4.64
OPA234UA	Open Design		1	SOIC	0.35	0.17	3.18	0.89	27.54	0.09	0.25	0.08	36	2.7	\$1.40
OPA234EA/250	Open Design		1	MSOP	0.35	0.17	3.18	1.09	27.54	0.09	0.25	0.2	36	2.7	\$1.34
OPA2209AIDGKT	Open Design		2	MSOP	18	9	101.85	0.3	23.48	0.18	2.2	0.07	36	4.5	\$1.90
OPA2209AID	Open Design		2	SOIC	18	9	101.85	0.3	23.48	0.18	2.2	0.07	36	4.5	\$2.00
OPA209AID	Open Design		1	SOIC	18	9	101.85	0.3	23.48	0.18	2.2	0.07	36	4.5	\$1.32
OPA209AIDBVT	Open Design		1	SOT-23	18	9	101.85	0.3	23.48	0.18	2.2	0.07	36	4.5	\$1.27
OPA4209AIFW	Open Design		4	TSSOP	18	9	101.85	0.3	23.48	0.18	2.2	0.07	36	4.5	\$3.50
OPA209AIDGKT	Open Design		1	MSOP	18	9	101.85	0.3	23.48	0.18	2.2	0.07	36	4.5	\$1.27
LMP7701MF	Open Design		1	SOT-23	2.5	1.25	15.91	0.4	26.47	0.18	0.79	0.074	12	2.7	\$1.40
LMP7701MA/NOPB	Open Design		1	SOIC	2.5	1.25	15.91	0.4	26.47	0.18	0.79	0.074	12	2.7	\$1.34
LMP7701MF/NOPB	Open Design		1	SOT	2.5	1.25	15.91	0.4	26.47	0.18	0.79	0.074	12	2.7	\$0.99
LMP7704MT	Open Design		4	TSSOP	2.5	1.25	15.91	0.44	26.47	0.18	0.8	0.074	12	2.7	\$2.88
LMP7704MA/NOPB	Open Design		4	SOIC	2.5	1.25	15.91	0.44	26.47	0.18	0.8	0.074	12	2.7	\$2.10
LMP7702MM	Open Design		2	MSOP	2.5	1.25	15.91	0.44	26.47	0.18	0.85	0.064	12	2.7	\$1.84
LMP7702MM/NOPB	Open Design		2	VSSOP	2.5	1.25	15.91	0.44	26.47	0.18	0.85	0.064	12	2.7	\$1.30

# WEBENCH® Amplifier Designer


The screenshot displays the WEBENCH Amplifier Designer interface. At the top, a toolbar contains icons for Back, New, Visualizer, Sim, Sim Export, Print, and Share Design, with a red box highlighting these icons and the text "Standard WEBENCH® icons and features". Below the toolbar is the "AMPLIFIER DESIGNER SUMMARY" section, which includes "Design Criteria" (input/output voltages, gains, and bandwidths), "Current Design: #1952", and "Amplifier Topology Specification" (General Non-Inverting Amplifier). The central area shows a circuit diagram of an OPA2188AID Dual device configured as a Dual Supply General Non-Inverting Amplifier with a gain of 2 V/V. The circuit includes resistors R1, R2, and Rload, and is powered by a dual supply (VCC = +5.00 V, VEE = -5.00 V). Below the circuit, there are three tabs: "Calculated Performance Analysis", "Calculated Performance Values", and "Bill of Materials", with a red box highlighting these tabs and the text "Design tabs". The "Calculated Performance Analysis" tab is active, showing a "Select Waveform:" dropdown set to "AC" and a "Plot" button. Below this are input parameters: Input DC Offset (0 Volts), Peak Amplitude (2 Volts), Frequency Min (1 Hz), and Frequency Max (10000000 Hz). Two graphs are displayed: "Input/Output Signal Peak Amplitude" and "Gain versus Frequency". The first graph shows the AC input signal (orange) and AC output signal (green) over a frequency range from 1.00Hz to 100.00MHz. The second graph shows the Gain (dB) versus Frequency (Hz) on a log-log scale, with the gain starting at approximately 20 dB and rolling off at high frequencies.

Supported WEBENCH® features include simulation, Sim Export, PDF report generation, and Share Designs

Design Tabs allow choice of Graphical Performance Analysis, Calculated Performance Values, and the Bill of Materials (BOM)

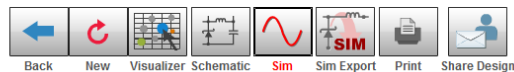
Waveform Analysis allows AC, Sine, and Square wave stimulus.

# WEBENCH® Amplifier Designer – Design Tabs

Calculated Performance Analysis		Calculated Performance Values		Bill of Materials			
Part	Manufacturer	Part Number	Price	Value	Footprint	Top View	Edit
R1	Vishay-Dale	CRCW04027K87FKED	\$0.01	7.870KΩ	3.000 mm <sup>2</sup>	▪	Select Alternate Part
R2	Vishay-Dale	CRCW04027K87FKED	\$0.01	7.870KΩ	3.000 mm <sup>2</sup>	▪	Select Alternate Part
U1	Texas Instruments, Inc.	OPA2188AID (Dual device)	\$1.70 Per Channel:\$0.85	N/A	56.580 mm <sup>2</sup>		Select Alternate Part



# WEBENCH® Amplifier Designer - Simulation



AMPLIFIER DESIGNER SIMULATION

Step 1 Select Simulation Type

Sine Wave Response

Step 2 Start New Simulation

Sine Wave Response Sim ID=1

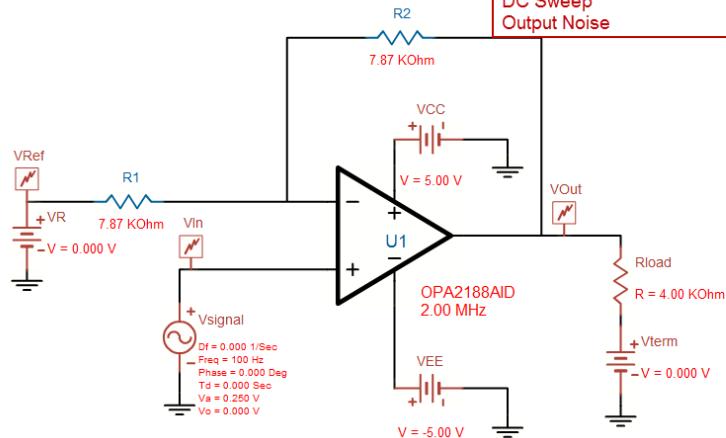
1.1



EDIT

Show Pins

5 Simulations supported  
Sine Wave Response  
Step Response  
Closed Loop Freq Response  
DC Sweep  
Output Noise



Active Design : simId= 1 Sine Wave Response Status = Success

Messages eSim Report Download: DATA FILE .CIR F...

Probes

VIn VOut VRef

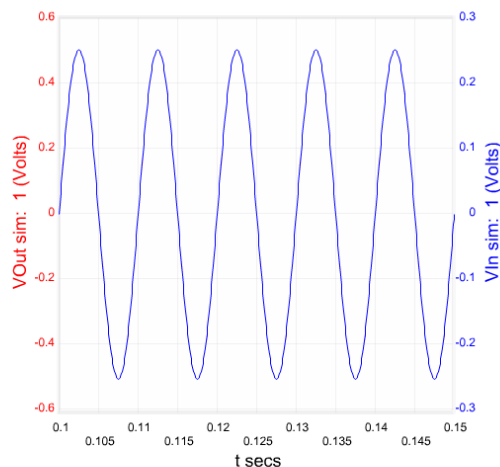
Interactive Waveform

Streaming Waveforms

Waveform Controls

Marker

Ready. Zoom-in: Click and drag downward; Zoom-out: Click and drag upward.



Same interface as other WEBENCH® Tools.

5 supported simulations

Simulations may be added to PDF report or may be shared with the Design

# Hands-on Exercise – Amplifier Designer

Design Problem:	Goals:
<p>The customer would like to design a simple inverting configuration amplifier. The circuit should use either a single (5V) or dual (+/- 5V) supply.</p> <p>The input voltage range is -0.5 to 0.7V and output voltage range is -2 to 4V. Output current max is 10mA.</p> <p>The most important concern is precision, followed by cost and noise.</p>	<p>Test the capabilities of the new Amplifier Designer and show the ease of use.</p> <p>Look at simulation results for impulse response and noise.</p> <p>Examine the tradeoffs for the optimizer cases and see if dual/single voltage supplies impact the solution.</p> <p>Extra credit: Include a shutdown capability</p>

# WEBENCH® Amplifier Designer - Example



New

## AMPLIFIER DESIGNER REQUIREMENTS

Power LED LED Architect Power Architect FPGA/µP HotSwap Simple Switcher Filters Clocks Load Switch Interface DDR Power Sequencers Battery Chargers Amplifiers

Select a topology and supply option and specify temperature range. Click on the 'Start Amplifier Design' button to create a design.

Start Amplifier Design

### Topology

- General Inverting Amplifier
- General Non-Inverting Amplifier

### Supply Option

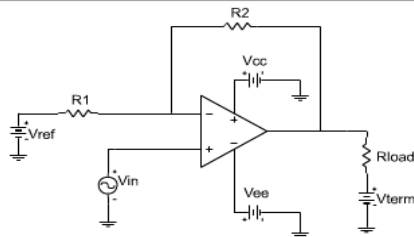
- Dual Supply
- Single Supply

### Expected Temperature Range

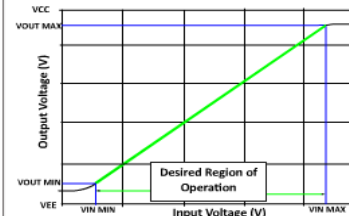
Min: -20 C  
Max: 70 C

### General Non-Inverting Amplifier

The NonInverting Amplifier multiplies the input voltage ( $V_{in}$ ) by the desired positive gain, and subtracts a voltage proportional to the applied reference voltage.



### Noninverting Amplifier Transfer Characteristic



$$V_{out} = V_{in} \left( 1 + \frac{R_2}{R_1} \right) - V_{ref} \left( \frac{R_2}{R_1} \right)$$

Start Amplifier Design

Select Topology and supply

# WEBENCH® Amplifier Designer - Example



Back New

## AMPLIFIER DESIGNER REQUIREMENTS

### Desired Power Supply Voltage

Dual Supply  Single Supply

Positive Supply(Vcc):  V Positive Supply Tolerance:  %

Negative Supply(Vee):  V Negative Supply Tolerance:  %

### Desired Input and Output Requirements

- Input Voltage Limits, Output Voltage Limits
- Input Voltage Limits, Gain
- Input Voltage Range, Output Voltage Range
- Input Voltage Range, Gain

Vin Min:  V

Vin Max:  V

Vout Min:  V

Vout Max:  V

Enter Specifications

Vin Min: -0.5 V Vout Min: -2 V

Vin Max: 0.7 V Vout Max: 4 V

Vin pk-pk: 1.2 V Vout pk-pk: 6 V

Vin Midpoint: 0.099 V Vout Midpoint: 1 V

Closed Loop Gain: -5 V/V Recommended Vref: 0.25 V

### Output Load

Output Current Max Sink Current:  mA

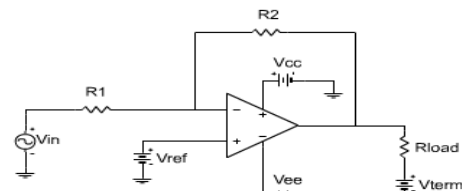
Resistive Load Max Source Current:  mA

Create Amplifier Design

### Desired Closed Loop Bandwidth

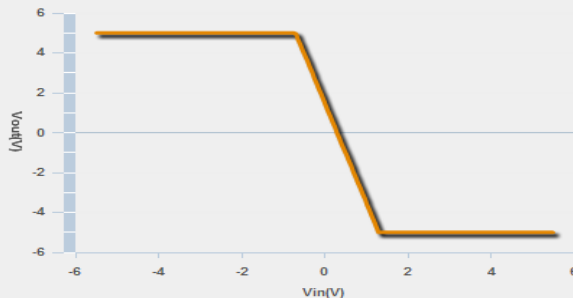
Small signal:  kHz

### General Inverting Amplifier



Notice the DC Characteristics update as specifications are entered

### DC Transfer Characteristic



# WEBENCH® Amplifier Designer - Example

← Back   ↻ New   📊 Visualizer

### AMPLIFIER DESIGNER VISUALIZER

**Design Criteria**

Topology: Inverting

Vin Min: -0.5 V   Vout Min: -2 V  
 Vin Max: 0.7 V   Vout Max: 4 V

Closed Loop Gain: -5 V/V  
 Voltage Reference: 0.25 V  
 Closed Loop Bandwidth: 10 KHz

Edit Inputs

**Schematic**

**Components**

OpAmp IC: LMC7101BIM5/NOPB  
 R1: 333 ohms  
 R2: 1667 ohms

**Optimizer**

Very Important: Precision |  
 Important: Cost |  
 Less Important: Noise |

Choose your optimization order of importance

**Refine Results**

Package Group: All |  
 No. of Channels: All |  
 Shutdown Pin:

**Solutions**

Part	Create	Simulation	No. of Channels	Package	Amplifier Gain Product (MHz)	Small Signal Bandwidth (MHz)	Full Power Bandwidth (kHz)	Precision (mVrms)	Total Output Noise (uVrms)	Output Temperature Delta (typ, mV)	IC Supply Current(mA)	Output Offset (mV)	Max Power Supply (V)	Min Power Supply (V)	1k Price (USD)
LMC7101BIM5/NOPB	Open Design	📈	1	SOT	1.1	0.91	17.5	-35	120.17	0.54	0.5	-0.55	15.5	2.7	\$0.29
LMC7111BIM5/NOPB	Open Design	📈	1	SOT	0.05	0.04	0.42	-34.99	75.81	1.08	0.025	-4.5	11	2.7	\$0.38
LMC7101AIM5/NOPB	Open Design	📈	1	SOT	1.1	0.91	17.5	-15	120.17	0.54	0.5	-0.55	15.5	2.7	\$0.38
TLV2731IDBVR	Open Design	📈	1	SOT-23	2	1.66	25.46	-14.99	71.73	0.27	0.85	-3.5	10	2.7	\$0.46
OPA171AIDBVT	Open Design	📈	1	SOT-23	3	2.5	23.87	-8.99	79.48	0.16199	0.475	-1.25	36	2.7	\$0.46
OPA171AQDBVRQ1	Open Design	📈	1	SOT-23	3	2.5	23.87	-8.99	79.48	0.16199	0.475	-1.25	36	2.7	\$0.47
LMC7101BIM5	Open Design	📈	1	SOT-23	1.1	0.91	17.5	-35	120.17	0.54	0.5	-0.55	15.5	2.7	\$0.42
OPA171AID	Open Design	📈	1	SOIC	3	2.5	23.87	-8.99	79.48	0.16199	0.475	-1.25	36	2.7	\$0.48
TLV271QDBVRQ1	Open Design	📈	1	SOT-23	3	2.5	33.42	-24.99	187.37	1.08	0.55	-2.5	16	2.7	\$0.30
TLV271QDRG4Q1	Open Design	📈	1	SOIC	3	2.5	33.42	-24.99	187.37	1.08	0.55	-2.5	16	2.7	\$0.30
TLV271QDRQ1	Open Design	📈	1	SOIC	3	2.5	33.42	-24.99	187.37	1.08	0.55	-2.5	16	2.7	\$0.30
LMC8101MMX/NOPB	Open Design	📈	1	VSSOP	1	0.83	15.91	-24.99	110.92	2.16	0.7	-3.5	10	2.7	\$0.46
LMC8101MM/NOPB	Open Design	📈	1	VSSOP	1	0.83	15.91	-24.99	110.92	2.16	0.7	-3.5	10	2.7	\$0.46
TLV272QDRQ1	Open Design	📈	2	SOIC	3	2.5	33.42	-24.99	187.37	1.08	0.55	-2.5	16	2.7	\$0.35
TLV272QDRG4Q1	Open Design	📈	2	SOIC	3	2.5	33.42	-24.99	187.37	1.08	0.55	-2.5	16	2.7	\$0.35
TLC081IDR	Open Design	📈	1	SOIC	10	8.33	254.64	-9.49	85.43	0.64799	1.8	-1.95	16	4.5	\$0.53
TLV271IDBVT	Open Design	📈	1	SOT-23	3	2.5	33.42	-24.99	208.51	1.08	0.55	-2.5	16	2.7	\$0.30
OPA171AIDRLT	Open Design	📈	1	SC-70	3	2.5	23.87	-8.99	79.48	0.16199	0.475	-1.25	36	2.7	\$0.54
LMC7111BIM5	Open Design	📈	1	SOT-23	0.05	0.04	0.42	-34.99	75.81	1.08	0.025	-4.5	11	2.7	\$0.54
TLV271ID	Open Design	📈	1	SOIC	3	2.5	33.42	-24.99	208.51	1.08	0.55	-2.5	16	2.7	\$0.31
TLV272IDR	Open Design	📈	2	SOIC	3	2.5	33.42	-24.99	208.51	1.08	0.55	-2.5	16	2.7	\$0.32
LMC8101TP/NOPB	Open Design	📈	1	DSBGA	1	0.83	15.91	-24.99	110.92	2.16	0.7	-3.5	10	2.7	\$0.52
LMC7101AIM5	Open Design	📈	1	SOT-23	1.1	0.91	17.5	-15	120.17	0.54	0.5	-0.55	15.5	2.7	\$0.52

# WEBENCH® Amplifier Designer - Example



## AMPLIFIER DESIGNER SUMMARY

**Design Criteria**

VinMin	-0.5 V
VinMax	0.7 V
VoutMin	-2 V
VoutMax	4 V
Closed Loop Gain	-5 V/V
Voltage Reference	0.25 V
Positive Supply	5 V
Negative Supply	-5 V
Closed Loop Bandwidth	10 KHz

Current Design: #1996

Name: **Your LMC7101BIM5/NOPB Inverting Am**

Notes:

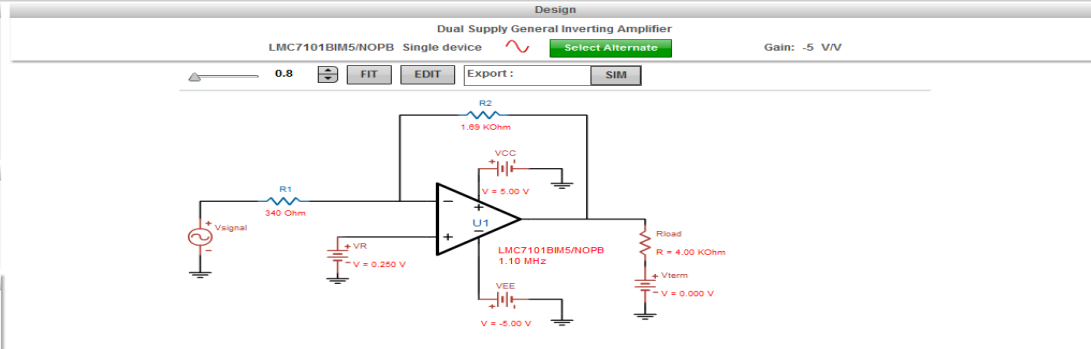
**Save Name & Notes**

**Amplifier Topology Specification**

Topology: General Inverting Amplifier

Res Tolerance: E96(1%)

**Update**



**Calculated Performance Analysis** | Calculated Performance Values | Bill of Materials

**View the Performance Analysis and Values**

Select Waveform:  AC  Sine  Square

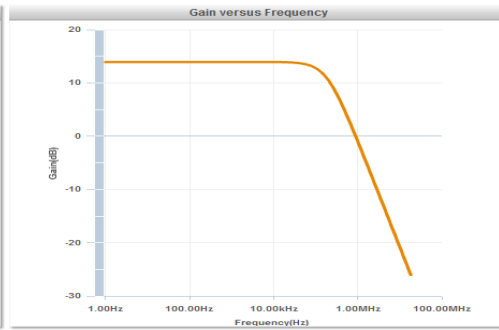
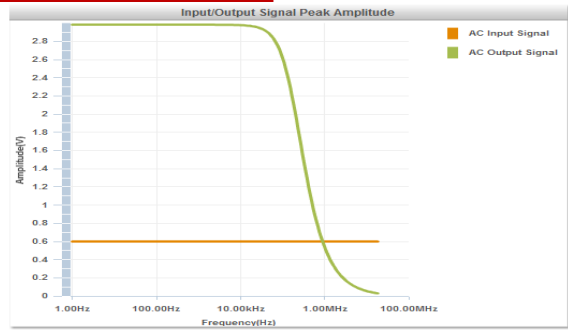
Input DC Offset: 0.099 Volts

Peak Amplitude: **0.6** Volts

Frequency Min: **1** Hz

Frequency Max: **18423645.32** Hz

**Plot**



# WEBENCH® Amplifier Designer - Example

Select the desired simulation

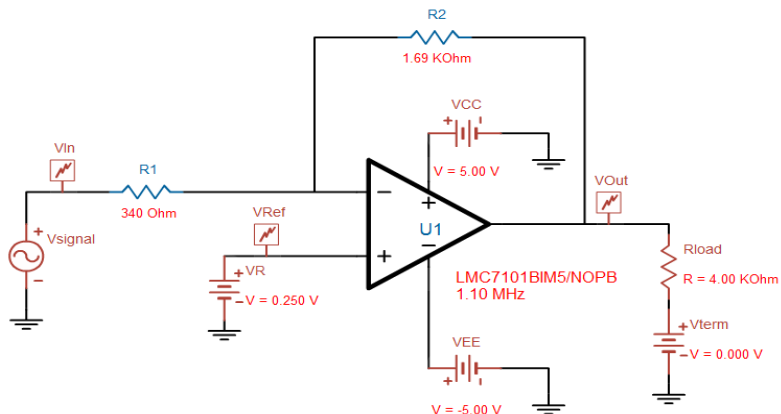


AMPLIFIER DESIGNER SIMULATION

Step 1 Select Simulation Type **Output Noise** Design : 1996

Step 2 **Start New Simulation** Output Noise Sim ID=1

1.1 FIT EDIT Show Pins



Active Design : simId= 1 Output Noise : 2016-05-12 13:52 Status = Success

Messages eSim Report Download: DATA FILE .CIR F...

Probes

VIn VOut VRef

Interactive Waveform Streaming Waveforms

Waveform Controls

Marker

Ready. Zoom-in: Click and drag downward; Zoom-out: Click and drag upward.

