Bucks: What are all these features?

Buck Switching Regulators
Katelyn Wiggenhorn
Summary

• Monitor Operating Voltages
  – EN/UVLO
  – RESET/PGOOD
  – Soft Start

• 2) Operation Considerations
  – Operation over $I_{\text{OUT}}$: PFM, Auto Freq. Foldback, Current Limit & Hiccup
  – Operation over $V_{\text{IN}}$: Dropout, Freq Foldback
  – Light-load efficiency and calculations: $I_q$

• 3) EMI
  – Package and Pinout
  – Spread Spectrum Feature
Basic Features:
EN/UVLO, Soft Start, Reset/PGOOD
UVLO

• **UVLO** – Disables IC at Under-Voltage Conditions

• Many types of UVLO may be featured in your converter/controller:
  – Internal LDO UVLO
    • Correlates with VIN Min spec
  – VIN UVLO – Use EN and resistors
    • Discussed in next slide
ENABLE

• **EN** - Used to enable and disable IC

• Options:
  – Connect EN to VIN to turn on the converter/controller when power is applied
  – Connect EN to VIN through a resistor divider to utilize UVLO
  – Connect EN to a controlled signal to externally sequence power-on of the IC.
ENABLE/UVLO Example

- EN Threshold for VOUT = 1.25V_{Max}
- VIN = 36V
- UVLO_{Desired} = 12V

- Choose R_{ENT}=100k
- Calculate R_{ENB} from datasheet
  - V_{EN,VOUT,H} = 1.25V
  - V_{IN_ON,H} = 12V

\[ R_{ENB} = \frac{1.25}{12 - 1.25} \times 100k \]

- R_{ENB}=11.6k

- Larger resistance decreases power loss in resistors
- Smaller resistance decreases noise susceptibility

<table>
<thead>
<tr>
<th>ENABLE (EN PIN)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{EN,VCC,H}</td>
</tr>
<tr>
<td>V_{EN,VCC,L}</td>
</tr>
<tr>
<td>V_{EN,VOUT,H}</td>
</tr>
<tr>
<td>V_{EN,VOUT,L}</td>
</tr>
<tr>
<td>I_{LEAK,EN}</td>
</tr>
</tbody>
</table>

\[ R_{ENT} = 100k \]
\[ R_{ENB} = 11.6k \]
EN/UVLO in Block Diagram
Soft Start

- Soft start limits peak inrush current at startup
- Internal Soft Start
  - Leave SS pin floating
- External Soft Start
  - Connect capacitor
  - Larger capacitor → Slower rise-time

![Diagram of LM73605/LM73606](image)

- Fast Ramp – Internal SS
- Slow Ramp – External SS
Soft Start Example

- VIN = 12V
- Desired rise time = 50ms (>internal soft start)

- Check datasheet – find equation: \( C_{SS} = I_{SSC} \times t_{SS} \)
  - \( I_{SSC} = 2\mu A \)
  - \( t_{SS} = 50\text{ms} \) desired
  - \( C_{SS} = 100\text{nF} \)

Or derive the equation with datasheet specs
**RESET/PGOOD**

- **RESET/PGOOD** - Used to signal when the output of the converter/controller is at the desired level

- Prevents false RESET flags with:
  - Hysteresis
  - Glitch Protection

- Connect to external circuitry to signify when it is okay to rely on this regulated voltage
RESET/PGOOD in Block Diagram

Diagram of LM73605/LM73606 showing PGOOD, OV/UV Detector, and other components.
Advanced Features:

PFM, Automatic Frequency Foldback, Clock Control, Current Limit, Hiccup
Comp Curve

- Rules of Operation
  - 1. Inductor current ($I_L$) will not go above Peak Current Command in normal operation
  - 2. $I_L$ will always drop to at least Valley Current Command
PFM

• Light load
  • SW is HIGH (HS FET ON, LS FET OFF)
    – Current goes up to $I_{\text{peak-min}}$
  • SW is LOW (HS FET OFF, LS FET ON)
    – Current goes down to 0A
  • SW is OFF (HS and LS FETs OFF)
    – DCM Ringing
• Start next switch when FB ($V_{\text{OUT}}$) hits low threshold
• DCM Pulse frequency increases as $I_{\text{OUT}}$ increases
• Good light load efficiency
CCM Auto Frequency Foldback

- SW is HIGH until Inductor Current hits Peak Current Command
- SW is LOW until $I_L$:  
  - Reaches Valley Current Command  
  - Or goes below Valley Current Command

- Auto foldback improves efficiency with lower switching frequency
Clock Control

- SW is HIGH until Inductor Current hits Peak Current Command
- SW is LOW for time set by Clock

- Constant Frequency
Current Limit Operation

• SW is HIGH until Inductor Current hits Peak Current Command
• SW is LOW for time set by Clock

• If IL has not reached Valley Current Command, SW will stay LOW until it does.

• Frequency folds back
  – Limits current
  – $V_{OUT}$ Droops – used to trigger hiccup
Hiccup Operation

• Hiccup
• Disables converter when $V_{OUT}$ droop detected
  – Usually ~40% $V_{OUT\_NOM}$
  – See datasheet
• Tries again after set time
  – Usually 10’s of ms
  – See datasheet
Hiccup vs No Hiccup

• Advantage of Hiccup
  – Reduces power consumption during short circuit
  – Reduces heat during short circuit
Benefits and Drawbacks of each Region

- Good light load efficiency
- Higher ripple on VOUT

+ Higher efficiency when folding back
+ Can have constant frequency at higher $I_L$ based on design

+ “Normal Operation”
+ Constant Frequency

+ Protects device
+ Will enter hiccup if VOUT droops to datasheet value
**Frequency Foldback Example**

- $V_{IN} = (T_S \times V_{OUT})/t_{ON}$
- LMR33630:
  - $T_S=500\text{ns}$; $V_{OUT} = 5\text{V}$; $T_{ON,\text{MIN\text{(typ)}}}=72\text{ns}$
  - $V_{IN} = (T_S \times V_{OUT})/t_{ON} = (500\text{ns} \times 5\text{V})/72\text{ns} = 35\text{V}$

**Minimum On Time Operation**

- $V_{IN}=35\text{V}$, $I_{Load}=750\text{mA}$, $T_{ON}=72\text{ns}$

**Frequency Foldback**

- $V_{IN}=36\text{V}$, $I_{Load}=0.75\text{A}$, $T_{ON}=60\text{ns}$
Not All switchers are equal: High-VIN output ripple

Competitor has +/-100mV output ripple for high-VIN operation

LM53635 Has smooth frequency foldback at high input voltage.
**T\textsubscript{ON\_MIN} Datasheet Specs**

**LMR33630**

Foldback by sensing $T\text{ON}$, hits $T\text{ON\_MIN}$

**LM53602**

Foldback by sensing VIN, avoids $T\text{ON\_MIN}$

$V_{OUT} = 3.3V$
**T\textsubscript{ON\_MIN} Frequency Foldback**

- As $V\text{IN}$ Increases:
  - Duty Cycle Decreases
  - $T\text{ON}$ reduces
- $T\text{ON}$ will eventually need to go below $T\text{ON\_MIN}$ (spec'd in datasheet)
- The IC cannot switch HIGH for shorter than $T\text{ON\_MIN}$ so the frequency folds back.
  - Duty cycle reduces
  - $V\text{OUT}$ remains the same
  - $T\text{ON\_MIN}$ is not violated

*Note* Heavy Load Helps!
Key Features for Automotive: Dropout

- $V_{\text{IN-Min}} = (V_{\text{IN}} \times D_{\text{MAX}}) - (R_{\text{DS_ON}} \times I_{\text{IN}}) - (R_{\text{DCR}} \times I_{\text{L RMS}})$
- $V_{\text{OUT}} = (V_{\text{IN}} \times D_{\text{MAX}})$
- $5V/0.98 = V_{\text{IN_MIN_FSW}} = 5.10V$
  - There is significant variation between the calculated value of frequency fold-back and the actual value of frequency fold-back. We recommend providing sufficient margin as necessary.

Minimum Off Time Operation

- $V_{\text{IN}} = 6.1V$, $I_{\text{Load}} = 750mA$, $T_{\text{OFF}} = 52.8ns$

Frequency Foldback

- $V_{\text{IN}} = 5.7V$, $I_{\text{Load}} = 750mA$, $T_{\text{OFF}} = 49ns$
Understanding Quiescent Current Specifications
Key Features for Automotive: Low-Iq

• Always-on automotive applications require power even when car is off
  – Body electronics (keyless entry)
  – Cluster, Infotainment (keep-alive MCU)

• These applications require very low no-load operating current (Iq)

• OEMs set standards for Iq at module level
  – Sometimes < 100uA

• Suppliers will want per DC/DC Iq’s in 10uA to 40uA range
Key Features for Automotive: Low-Iq

Three Measurements for Quiescent Current:

- **Shut Down Current**
  - Part disabled; Enable tied to GND.

- **Non-Switching Iq**
  - Part enabled, feedback tied high. This value can be found in the EC table, and is traditionally measured open loop on the ATE.

- **Switching Iq**
  - Also known as operating quiescent current or no load input current.
Calculating Operating \( I_Q \) Based on EC Table

- \( I_{Q-SW} = I_Q + I_{EN} + (I_B + I_{DIV}) \times (V_{OUT} / (n_{eff} \times V_{IN})) \)
  - \( I_{Q-SW} = I_{VIN} = \) No Load Current
  - \( I_Q = I_{Q-NON-SW} = \) Current Drawn at Input Pin
  - \( I_{EN} = \) Current Drawn at Enable Pin
  - \( I_B = \) Current Drawn at Bias Pin
  - \( I_{DIV} = \) Current Drawn at Feedback Divider
  - \( n_{eff} = \) Light Load Efficiency

- Example (LMS3655):
  - \( I_{Q-SW} = I_{VIN} = 23.2\mu A \)
  - \( I_Q = I_{Q-NON-SW} = 7.5\mu A \)
  - \( I_B = 32\mu A \)
  - \( I_{DIV} = 0\mu A \) (Fixed Output Variant)
  - \( n_{eff} = .85 \)
Wide Input Converters: EMI Optimized
What makes a low EMI Buck

SW node capacitive coupling to the environment

Return path of coupling is over Input wires

-> Now it's source of the Common Mode Noise

\[ C = 7fF \]

EMI Filter

Buck

\[ \text{dV/dt} \]

Near E-Field coupling

Input cable

Low pass

Output cable

Load

DC Source

Input Noise

Output Noise

Examples:

1mV pkpk on PCB trace

140uV pkpk with unshielded Cable similar to CISPR

-12dB/Oct -40dB/Dec
EMI Optimization: Hot Rod Package

Minimize EMI through:
1. No-wirebond VSON packaging
2. Symmetric pinout
3. Spread spectrum feature

Die is flipped and placed directly onto the lead frame

Standard wirebond QFN package

Flip chip on lead frame QFN

Wirebond QFN

No-Wirebond QFN

LMS3655
EMI Optimization: Symmetric Pinout

Minimize EMI through:
1. No-wirebond VSON packaging
2. **Symmetric pinout**
3. Spread spectrum feature
EMI Optimization: Spread Spectrum Feature

Minimize EMI through:
1. No-wirebond VSON packaging
2. Symmetric pinout
3. **Spread spectrum feature**

Spread spectrum makes it easier to design and meet OEM standards for conducted and radiated EMI

LMS3655 without spread spectrum

LMS3655 with spread spectrum

Up to 10dB reduction
Design Tools
Design Tools

• WEBENCH
  – Every part in our portfolio is on WEBENCH
• Tina/PSpice
  – Every part in our portfolio has simulation files
• Design Guidelines
  – Every datasheet has an example circuit and design details
  – Every IC has an EVM
• Debugging
  – E2E