Get Your Clocks in Sync!

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Signal Measurement and Source Generation & Test and Measurement Sector
Agenda

• Applications
• Benefits of JESD204B
• Reference design overview
• Reference design results
• Future Investigations
The industry is moving towards millimeter wave

Trends:

• Multiple industries quickly moving beyond 6GHz carrier frequency range
• Need for higher data rates pushing instantaneous BW to ≥1GHz
• High performance clocking solutions needed to maintain system level performance
JESD204B Benefits

- Reduced/simplified PCB area
- Reduced package size
- Comparable power for large throughput
- Scalable to higher frequencies
- Simplified interface timing
- Standard interface
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**Speed limited** by setup/hold due to PVT variation

**Speed scalable** using SERDES/CDR techniques
JESD204B Benefits

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- Reduced package size
- Comparable power for large throughput
- Scalable to higher frequencies
- Simplified interface timing
- Standard interface
Multi-Channel JESD204B 15 GHz Clocking Reference Design for DSO, Radar and 5G Wireless Testers
TIDA-01021

Features

- 15 GHz Multi-channel JESD204B complaint clocking solution,
- Device clock frequency – LMX2594 (max – 15 GHz)
- SYSREF provided for JESD204B interface – LMX2594
- Scalable clocking solution, which can generate various DEVCLK by LMX2594 / LMK04828
- FMC connector adaptor boards to interface with TI high speed analog front end EVMs
- Low power and highly integrated multi-channel clocking solution with JESD204B complaint

Target Applications

- Oscilloscope
- Wireless Communication Tester
- Software Defined Radio
- Phased Array Radar

Tools & Resources

- Synchronization of JESD204B Giga-Sample ADCs using Xilinx Platform for Phased Array Radar Systems
- LMX2594
- LMK04828

Benefits

- JESD204B compatible clocking solution for high dynamic range and high SNR multi-channel AFE signal chain
- Configurable phase synchronization to achieve low skew
- 15 GHz clocking solution can be used in multiple end equipments (DSO, Radar, Wireless Test, etc.)
- Supports low latency signal measurement and signal generation systems

Released: 6/17
Full Evaluation System

ADC Eval Board
JESD204B Capture Card
FMC+ Adapter Board
Clock Board
*For LMXs REFin delayed signal, DCLKout0/2 connection (provision) provided to REFin.
*LMXs are bypassed in dotted lines and converters DCLK and SYSREF will be provided through LMK.
FMC Connector Adaptor Board

TIDA-01021

- Provides clock and SYSREF signal to the FPGA on the capture board from the clocking board
- Passes JESD204B serial lanes from the ADC EVM to the FPGA on the capture board
The TIDA-01021 clocking board has multiple power supply options including DC-DC only and high performance RF LDOs.
# Target Subsystem Specifications

**TIDA-01021**

<table>
<thead>
<tr>
<th>Key Feature</th>
<th>Specifications</th>
<th>Conditions</th>
<th>Remarks</th>
</tr>
</thead>
</table>
| **Dev_Clk Phase Noise** | -117.0 dBC/Hz @ 10KHz offset  
-119.7 dBC/Hz @ 100KHz offset  
-130.5 dBC/Hz @ 1MHz offset  
-149.5 dBC/Hz @ 10MHz offset | @ 3.5 GHz        | Phase noise data from LMX2594 preliminary datasheet (LMX2594_Datasheet_2017_2_23.pdf)       |
|                      | -108.8 dBC/Hz @ 10KHz offset  
-111.4 dBC/Hz @ 100KHz offset  
-123.1 dBC/Hz @ 1MHz offset  
-147.4 dBC/Hz @ 10MHz offset | @ 9 GHz          |                                                                                             |
|                      | -104.7 dBC/Hz @ 10KHz offset  
-107.5 dBC/Hz @ 100KHz offset  
-114.7 dBC/Hz @ 1MHz offset  
-141.7 dBC/Hz @ 10MHz offset | @ 15 GHz         |                                                                                             |
| **Channel-to-channel Time Skew** | < 50ps                                                                 | @ 357.77MHz ADC input signal  
@ 607.77MHz ADC input signal  
@ 982.77MHz ADC input signal  
@ 1857.77MHz ADC input signal  
@ 2482.77MHz ADC input signal | Value taken from TIDA-00432                                                                 |
| **SNR (dBFS) (DDC bypass mode)** | 55.0                                                                 | @ 357.77MHz ADC input signal  
@ 607.77MHz ADC input signal  
@ 982.77MHz ADC input signal  
@ 1857.77MHz ADC input signal  
@ 2482.77MHz ADC input signal | SNR values at -0.5dBFS input signal taken from ADC12DJ3200 preliminary datasheet (ADC12DJxx00_preliminarydatasheet_v1p17_13dec2016.pdf) |
## Measured Phase Noise Performance

<table>
<thead>
<tr>
<th>OUTPUT FREQUENCY (GHz)</th>
<th>CONDITION</th>
<th>EXPECTED PHASE NOISE (dBc/Hz)</th>
<th>MEASURED PHASE NOISE (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.5</td>
<td>10-kHz offset</td>
<td>-117.0</td>
<td>-116.0</td>
</tr>
<tr>
<td></td>
<td>100-kHz offset</td>
<td>-119.7</td>
<td>-118.3</td>
</tr>
<tr>
<td></td>
<td>1-MHz offset</td>
<td>-130.5</td>
<td>-128.7</td>
</tr>
<tr>
<td></td>
<td>10-MHz offset</td>
<td>-149.5</td>
<td>-151.5</td>
</tr>
<tr>
<td>9.0</td>
<td>10-kHz offset</td>
<td>-108.8</td>
<td>-108.1</td>
</tr>
<tr>
<td></td>
<td>100-kHz offset</td>
<td>-111.4</td>
<td>-110.1</td>
</tr>
<tr>
<td></td>
<td>1-MHz offset</td>
<td>-123.1</td>
<td>-122.9</td>
</tr>
<tr>
<td></td>
<td>10-MHz offset</td>
<td>-147.4</td>
<td>-147.5</td>
</tr>
<tr>
<td>15.0</td>
<td>10-kHz offset</td>
<td>-104.7</td>
<td>-103.8</td>
</tr>
<tr>
<td></td>
<td>100-kHz offset</td>
<td>-107.5</td>
<td>-105.9</td>
</tr>
<tr>
<td></td>
<td>1-MHz offset</td>
<td>-114.7</td>
<td>-115.1</td>
</tr>
<tr>
<td></td>
<td>10-MHz offset</td>
<td>-141.7</td>
<td>-140.8</td>
</tr>
</tbody>
</table>

Phase Noise at 3.5GHz  
Phase Noise at 9GHz  
Phase Noise at 15GHz
Measured Channel to Channel Clock Skew

<10ps skew measured between the two LMX2594 outputs!
# Measured Full Signal Chain Performance

## Table

<table>
<thead>
<tr>
<th>INPUT FREQ (MHz)</th>
<th>ADC DATASHEET SNR (dBFS)</th>
<th>MEASURED SNR ON ADC12DJ3200EVM WITH ONBOARD CLOCK (dBFS)</th>
<th>MEASURED SNR ON ADC12DJ3200EVM WITH TIDA-01021 CLOCKS (dBFS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>997</td>
<td>56.3</td>
<td>55.25</td>
<td>54.4</td>
</tr>
<tr>
<td>2483</td>
<td>55.2</td>
<td>52.71</td>
<td>51.9</td>
</tr>
<tr>
<td>5250</td>
<td>52.6</td>
<td>50.34</td>
<td>49.6</td>
</tr>
</tbody>
</table>

## Spectra

- **Spectrum at 997-MHz Input**
- **Spectrum at 2482-MHz Input**
- **Spectrum at 5250-MHz Input**
Future Investigations

TIDA-01021

- Multi-Channel JESD204B Clocking Solution (up to 15GHz)

TIDA-01021.1
- Multichannel solution with >3.2GHz external low noise DEVCLK clock
  - REFCLK generated from divider on DEVCLK

TIDA-01021.2
- Scalable multichannel clocking solution

TIDA-01021.3
- Multichannel clocking solutions for high speed RF ADC and DAC combo

TIDA-01021.4
- Synchronization of digital functions (ADC: NCO, DDC; DAC: NCO, DUC) in a multichannel clocking system

TIDA-01021.5
- Temp effects on deterministic latency, skew and SNR performance of multichannel clocking solution

TIDA-01021.6
- Multichannel solution with <3.2GHz external low noise DEVCLK clock
  - LMK04832 in distribution mode with DEVCLK as REFCLK

TIDA-01021.7
- Multichannel solution for >3.55GHz DEVCLK clock
Multiple Boards Synchronization

TIDA-01021

- Tree topology to connect multiple boards with master board for synchronization
- Maximum 7 boards can connect
- Single loop 0-delay operation with SYSREF re-clocking
- Master LMK will be in the distribution mode
- Master sends SYSREF pulses to each slave LMK04828 for sync the dividers
LMK0482x: JESD204B Compliant Clock Cleaner

**Features**

- Support Device clocks & SYSREF per JESD204B or larger conventional clocking systems!
- Dual Loop PLLatinum PLL Architecture
- 88 fs RMS jitter at 245.76 MHz, 10 kHz – 20 MHz
- 2 Integrated VCO to support 2 different freq
- Option of using external VCO for different apps
- Holdover mode when input clock is lost
- Digital Delay, Analog Delay and 0-delay mode
- Package 9mm x 9mm QFN-64

**Applications**

**Low Jitter Noise with JEDEC JESD204B**

- JESD204B and Traditional Clocking Systems
- Data Converter Clocking
- Wireless Infrastructure
- Networking, SONET/SDH, DSLAM,
- Medical, Video, Military, Aerospace
- Test and Measurement

**Benefits**

- **First Clocking/Timing solution** supports JESD204B standard
- **7 dB better than** AD9523 and PM7520 phase noise @ 368.64 MHz @ 800 kHz offset
- **5 dB lower than** AD9523 and PM7520 noise floor @ 368.64 MHz @ 800 kHz offset

**Part #** | **VCO0 Freq. (MHz)** | **VCO1 Freq. (MHz)**
--- | --- | ---
LMK04821 | 1930 – 2075 | 2920 – 3080
VCO1 Div = \(\div2\) to \(\div8\)
\(\div2 = 1460 – 1540\)

LMK04826 | 1840 – 1970 | 2440 – 2505

LMK04828 | 2370 – 2630 | 2920 – 3080

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TI Information – Selective Disclosure
LMX2594: 10MHz - 15GHz wideband PLL with integrated VCO
pin compatible with LMX2592 (no doubler)

Features

- Wideband PLL supporting output frequencies up to 15GHz with no doubler
- -110dBc/Hz Closed loop phase noise at 100KHz offset at 15GHz carrier frequency
- Best in class 1/f noise of -129 dBc/Hz
- Improved Noise FOM of -236 dBc/Hz
- 300 MHz PFD in fractional mode, 400MHz in Integer mode
- Technique to remove Integer Boundary Spurs
- Ability to synchronize output phase with OSCin
- Frequency Ramping feature
- Fast calibration time (< 25usec)
- SYSREF support
- Dual Differential outputs ; Single 3.3V supply

Benefits

- Improve channel density, save board space and complexity by replacing discrete components with LMX2594
- Remove need for external filters needed with solutions that have internal doubler
JESD204B SYSREF support

- RFoutB can be reconfigured as SYSREF
- Max output frequency 85MHz
- Fine delay adjustment available
  - Min resolution : ~9ps
  - Max delay : 2.5ns
ADC12DJ3200
12-Bit, Dual 3.2-GSPS or Single 6.4-Gsps ADC with JESD204B Interface

Features

- Configurations (SPI controlled):
  - Dual 12-bit 3.2 GSPS
  - Single 12-bit 6.4 GSPS
- Low Power:
  - 3.6 W total (1ch Mode, BG Cal)
- Buffered Inputs:
  - 8-GHz Input Bandwidth (-3 dB)
- Input Fullscale:
  - 0.8 Vpp (Adjustable, 0.5 Vpp to 0.95 Vpp)
- Noise Floor (3.2 Gsps):
  - -150 dBFS/Hz
- Noise Floor (6.4 Gsps):
  - -153 dBFS/Hz
- IMD3 at fin = 2.5GHz:
  - -73 dBc (@ -7 dBFS)
- Code Error Rate:
  - 10^-16
- Optional Decimation
  - 2x (real), 4/8/16x (complex)
- Digital Interface:
  - JESD204B
    - Subclass 1 support
    - 8 Lanes at 12.8 Gbps (max Fs)
    - 16 Lanes at 6.4 Gbps (max Fs)
- Power supplies:
  - 1.1V, 1.9V
- Package:
  - BGA (10x10mm, 0.8mm pitch)

1-ch Mode Performance (6.4 GSPS) | 1 GHz | 2.5 GHz
--- | --- | ---
SNR (dBFS, typ. int. spurs excluded, -1dBFS) | 56 | 55
NSD (dBFS/Hz, typ) | -153 | -152
HD2,3 (dBc, typ) | -68 | -68
Non HD2,3 (dBc, typ) | -73 | -72
Interleaving Spur (dBFS, typ) | -63 | -58
**TSW14J56**

**JESD204B Pattern Capture/Generation Tool**

### Specifications

- Works with all TI’s JESD204B data converters
- 8Gbit DDR3 memory (512Msamples 16 bits)
- Supports up to 10 lanes @ 10.3 GBits/ second
- Common HSDC Pro GUI software control
- Supports ADC, DAC, TXRX modes
- USB 2 interface
- Altera Arria V GZ FPGA
- Standard FMC port connectivity

### Benefits

- Single platform for evaluation and test of current and future TI JESD204B ADCs and DACs
- Generation or analysis of long time domain complex modulated signals
- Flexibility of system evaluation
- Easy to use software for signal analysis and generation
- USB 2.0 works with any PC

### Applications

- Pattern generation and capture of TI’s JESD204B data converters

### DAC Patterns (tx) and ADC Capture (rx)

- **TSW14J56**
- **204B DAC Data**
- **TSW14J56**
- **204B ADC Data**
Additional Resources

- Full reference design including the design guide, schematics, gerbers and BOM for the clocking and FPGA adapter boards – TIDA-01021
- **Hardware & Software** setup videos
- **LMK04828** Synthesizer & Jitter Cleaner
- **LMX2594** 15GHz RF Synthesizer
- **ADC12DJ3200** 12-Bit, Dual 3.2-GSPS/Single 6.4-GSPS ADC w/ JESD204B Interface
- **TSW14J56** JESD204B FPGA Capture Board
- **HSDC-PRO** Capture Software