

# Designing Ethernet Reference Clocks

TI Precision Labs – Ethernet

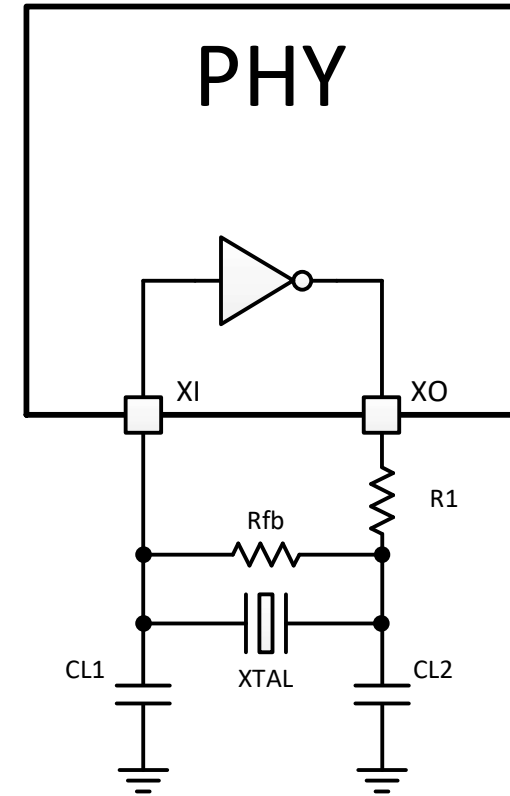
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# Crystal oscillator architecture for TI PHYs

Designator	Description
XTAL	AT cut, 25 MHz crystal
CL1, CL2	Load capacitors
R1	Current limiting resistor
Rfb	Feedback resistor



# Crystal selection

## Important crystal parameters to consider:

- Frequency tolerance
- Frequency stability
- Load capacitance
- ESR
- Drive level

## Example Crystal Specifications

Parameters	Min	Typ	Max	Units
Frequency Range	24.000 0		52.000 0	MHz
Operating Temperature Range	-40		+125	°C
Frequency Tolerance @ +25°C	-10		+10	ppm
Frequency Stability over Operating Temperature	-10		+10	ppm
Equivalent series resistance (ESR)		< 80	100	Ω
Load capacitance (CL)		4.0		pF
Drive Level (DL)		10	100	μW
Aging (1 year)	-2		+2	ppm

# Load capacitors selection

Ceq must be equal to load capacitance of XTAL (CL)

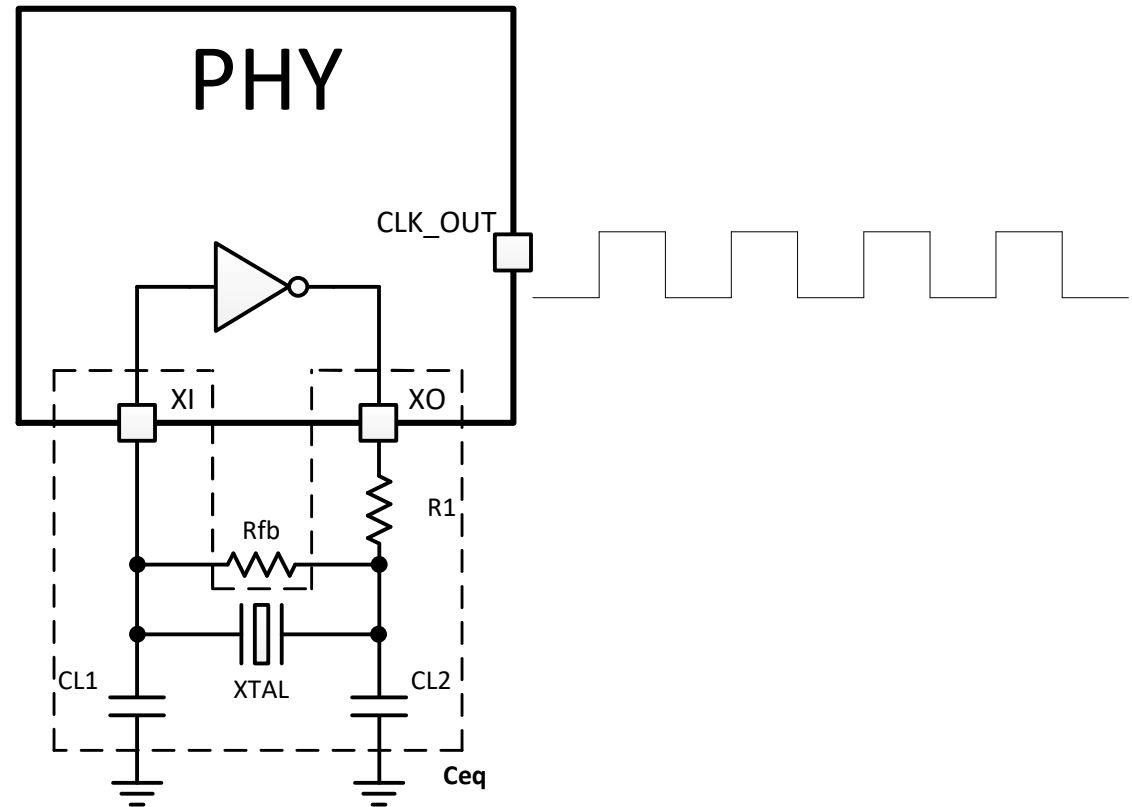
$$CL = Ceq$$

Ceq is estimated by

$$CL = Ceq = Cstray + \frac{CL1 \times CL2}{CL1 + CL2}$$

Cstray is the capacitance of traces and XI / XO pins

$$CL1 = CL2 = 2 \times (CL - Cstray)$$



**CL1 & CL2 ≠ load capacitance (CL) specified in XTAL datasheet**

# Current limiting resistor selection

1. Start with the first order approximation for R1:

$$R1 = \frac{1}{2\pi \times 25 \text{ MHz} \times CL2}$$

2. Measure  $I_{Y1,RMS}$  and determine if the crystal drive level meets the crystal specifications

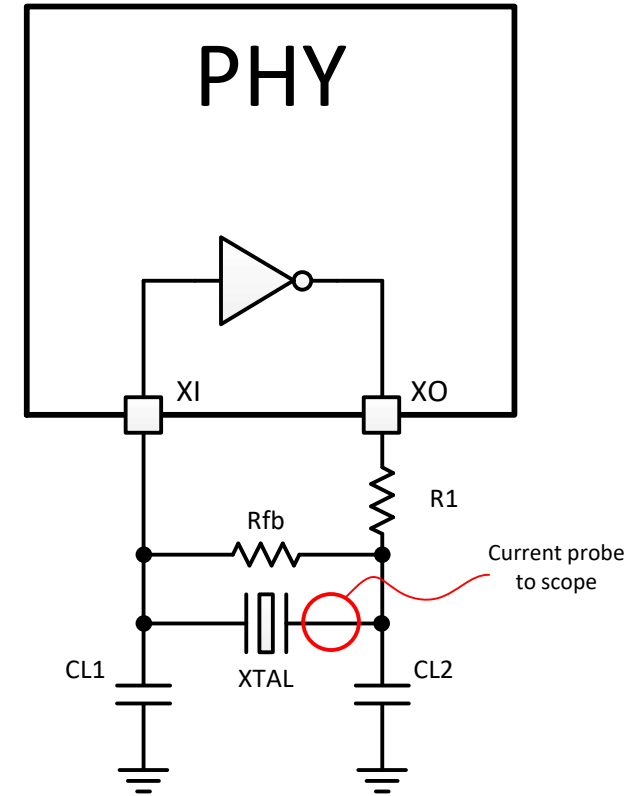
$$DL_{max} \geq I_{XTAL,RMS}^2 \times ESR$$

3. Increase value of R1 if calculated crystal drive level is not within crystal specifications

4. Calculate  $V_{CL1,pk-pk}$  and ensure it satisfies  $V_{ih}$  requirements of PHY's XI pin

$$V_{CL1,pk-pk} = I_{XTAL,RMS} \times \sqrt{2} \times |Z_{CL1}|$$

NOTE: 500  $\mu$ W or higher crystals may not require a current limiting resistor



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