Digitally Controlled High Efficiency and High Power Density PFC Circuits

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C2000 Digital Power System Solutions
Detailed Agenda

• PFC Stage, PF, THD, Modes of Operation, Evolution of PFC Circuits

• 3Ph Interleaved CCM Totem Pole PFC Ref Design (TIDM-1007)
  – Overview
  – Software Structure
  – Digital Control Design
  – Experimental waveforms and test data
  – Improvements in efficiency, Transient Response & Power Factor

• 2Ph Interleaved TRM Totem Pole PFC Ref Design (TIDA-0961)
  – Overview
  – Challenges and Solutions
  – Software Structure
  – Experimental waveforms and test data
• Power Factor is affected by Distortion factor ($K_d$) and Displacement factor ($K_\theta$)
  \[ PF = \frac{I_{rms,1}}{I_{rms}} \cos \theta = K_d K_\theta, \]
  where $\theta$ is the phase angle between fundamentals of $V_{in}$ and $i_{in}$

• THD is affected by Distortion factor
  \[ THD = \sqrt{\left(\frac{I_{rms}}{I_{1,rms}}\right)^2 - 1}. \]
  $I_{rms,1} = I_{rms}$ implies $K_d = 1$. Then $THD = 0$.

• PFC circuit is controlled to achieve $PF \approx 1$ and $THD \approx 0$ in AC to DC conversion
PFC Modes of Operation – CCM, DCM & TRM

**CCM Mode of operation**

- EPWM
- iL
- Vds

**DCM Mode of operation**

- EPWM
- iL
- Vds

**TRM/CRM/BCM Mode of operation**

- EPWM
- iL
- Vds

**CCM Mode** TIDM-1007
Fixed Frequency

**DCM Mode** TIDM-2PHILPFC
(under light load)
Fixed Frequency

**TRM/CRM/BCM Mode** CRM Mode TIDA-00961
Variable Frequency
Evolution of PFC Circuits

Interleaved Boost PFC  TIDM-2PHILPFC
Bridgeless PFC  BLPFCKIT
Traditional Totem Pole PFC

IL ZVS TP PFC with SiC
CCM Mode TIDA-01604

IL ZVS TP PFC with GaN
CCM Mode TIDM-1007
CRM Mode TIDA-00961

ZVS Totem Pole PFC

➤ Challenges in Totem Pole Bridgeless PFC
- Control Design: Voltage and Current Loops
- Zero crossing current spike/ distortion
- Meeting Spec : Power Factor, THD, Efficiency
TIDM-1007

Interleaved CCM Totem Pole PFC Reference Design

C2000 System Solutions: Digital Power
TIDM-1007 Interleaved CCM TP PFC

Features

- GaN based Totem Pole 1PH PFC with three interleaved phases using LMG3410 & controlled using C2000 MCU
- Power Spec
  - Input: 80-260 Vac, 50/60Hz
  - Output: 400V DC
  - Power: 3.3KW at 220Vrms & 1.6KW at 110Vrms
  - Efficiency: > 98.67% peak efficiency
- Low total harmonic distortion (THDi) < 2% (at low line)
- 100 kHz PWM switching
- Soft starting for totem pole bridge
- Phase shedding to enable higher efficiency
- Non Linear control loop to reduce voltage spikes

Benefits

- High power density design, with form factor matching OEM specifications
- TI-GaN with integrated gate drivers - greater integration.
- High performance C2000 controller enables superior and advanced control scheme to be implemented
- poweSUITE support enables easy adaptation of software

Applications

- On-board chargers for EV
- Telecom Rectifiers
- Other industrial applications

Tools & Resources

- Key TI Devices: TMS320F28075, LMG3410, UCC27714D, UCC28740, UCC24636
CCM TP PFC Operation

Positive Vin Line Cycle (50/60 Hz)

Negative Vin Line Cycle (50/60 Hz)

PWM Switching Cycle
CCS Software Structure
CCS Project Structure

Incremental Build Levels to Simplify the Design of the System

**INCR_BUILD 1** : Open Loop Check under DC input

**INCR_BUILD 2 - DC** : Closed Current Loop Check under DC input

**INCR_BUILD 2 - AC** : Closed Current Loop under AC input

**INCR_BUILD 3** : Closed Voltage and Current Loop under AC input
Setup device
Setup PWM
Setup ADC

Global Variables Initialization
Setup Board Protection

Setup Interrupts

Current Loop ISR (100Khz)

C – ISR
Save context & clear interrupt flags
Read ADC Result
Run Current Loop Compensator Gi
Run PWM Modulator
Run SPLL & calculate current reference
Run Adaptive Deadtime Calc.
Restore Context
Return

Save contexts and clear int flags
Enable Interrupt EINT
Run notch filter on measured bus voltage
Run Voltage Loop Compensator Gv
Run power measurement
Run Data Logger
Restore Context
Return

Main Loop

Cinit_0

Current Loop ISR

Voltage Loop plus Instrumentation Code (10Khz)

Setup Board Protection

Current Loop ISR

BackGround Loop
State Machine
SFRA Background Function

Voltage Loop plus Instrumentation ISR

Restore Context
Return
Build Level 1- DC: Open Loop Check

4th Order Notch Filter

Compute Average

100kHz, Voltage Loop & Instrumentation ISR

10kHz, Current Loop ISR

PWM
dutyPU_DC

DCL_DF22

DCL_DF22

vBus_sensedFilteredNotch2

Read ADC & Scale to PU

ac_vol_sensed
ac_cur_sensed
ac_N_sensed
ac_L_sensed
vBus_sensed
iL1/2/3_sensed

10kHz,
Voltage Loop
&
Instrumentation
ISR
Build Level 2 - DC: Closed Current Loop

DCL_DF22

4th Order Notch Filter

vBus_sensedFilteredNotch2

ac_cur_ref

PFC Current Controller Gi

DCL_PI

ac_cur_ref_inst

PWM

dutyPU

10Khz, Voltage Loop and Instrumentation ISR

Compute Average

Read ADC & Scale to PU

IL1/2/3_sensed
ac_cur_sensed
ac_vol_sensed
ac_N_sensed
ac_L_sensed

vBus_sensed

10Khz Current Loop ISR

100Khz, Voltage Loop and Instrumentation ISR

DLOG_4CH

input_ptr1
input_ptr2
input_ptr3
input_ptr4

output_ptr1
output_ptr2
output_ptr3
output_ptr4

100Khz, Current Loop ISR

Gi

AC Voltage Feedforward

Boost Voltage Drop Feedforward

Bus Voltage Feedforward

Input

DBUFF1
DBUFF2
DBUFF3
DBUFF4

Output

10Khz, Voltage Loop and Instrumentation ISR
Build Level 2 - AC: Closed Current Loop

**POWER MEAS SINE ANALYZER**
- Vin
- Vrms
- Irms
- SampleFreq
- Threshold
- Sigfreq
- Pwr

**DCL_DF22**
- vBus_sensedFilteredNotch2

**DLOG_4CH**
- DBUFF1
- DBUFF2
- DBUFF3
- DBUFF4

**DCL PI**
- Bus Voltage Feedforward
- AC Voltage Feedforward
- Boost Voltage Drop Feedforward
- Soft Start Around Zero Crossing
- PWM modulation change for AC half cycle

**PWM**
- DutyPU

**VBus_sensed**
- ac_vol_sensed
- ac_cur_sensed
- ac_N_sensed
- ac_L_sensed
- vBus_sensed

**SPLL 1ph SOGI**
- sin(θ)
- cos(θ)
- Vbus

**Compute Average**

**10Khz, Voltage Loop and Instrumentation ISR**
- ac_vol_ref

**4th Order Notch Filter**

**100Khz, Current Loop ISR**

**SampleFreq Threshold**

**Threshold**

**SampleFreq**

**Sigfreq**

**Pwr**

**Compute Notch**

**vBus_sensedFilteredNotch2**

**ac_cur_ref**

**ac_cur_ref_inst**

**PWM modulation change for AC half cycle**

**Soft Start Around Zero Crossing**
Build Level 3: Closed Voltage and Current Loop

- **PFC Voltage Controller Gv**
- **PFC Current Controller Gi**
CCM TP PFC Current Loop Model

Current Loop Model includes sync FET control and feedforward for
- Input AC voltage
- Output bus voltage
- Inductor Voltage drop
CCM TP PFC Voltage Loop Model

Small signal model of the DC Bus regulation loop is developed by linearizing the following power equation:

\[ i_{DC} V_{bus} = \eta V_{Nrms} i_{Nrms} \Rightarrow i_{DC} = \eta \frac{V_{Nrms}}{V_{bus}} i_{Li} \]

For resistive load the bus voltage and current are relating as:

\[ \hat{v}_{bus} = \frac{R_L}{1 + sR_L C_o} \hat{i}_{DC} \]

The plant model for the bus control can be written as below:

\[ H_p_{bus} = H_{load} \times \eta \times K_{i\_gain} \times K_{v\_gain} \times K_{v\_flt} \]
Current & Voltage Loop Verification Using SFRA

Gi OL Gain Model vs Measured with AC from direct Grid Input

- Model
- Measured with AC from direct Grid Input

BW: 6.47KHz 5.97KHz
GM: 7.17dB 6.62dB
PM: 49.8° 44°

Gv OL Gain Model vs Measured

BW: 6.15 Hz
GM: 38dB 31dB
PM: 73° 75°
CCM TP PFC Current & Voltage Loops SFRA Plots

TI Information – Selective Disclosure
Startup Waveforms

Low Line - 120Vrms, 60Hz

High Line - 230Vrms, 50Hz
Steady State Waveforms

120Vrms, 60Hz

- DC Bus Voltage: 120Vrms
- Current: 6.7% voltage ripple
- Steady State: 1628W
- iTHD: 1.75%
- Efficiency: 97.61%

230Vrms, 50Hz

- DC Bus Voltage: 230Vrms
- Current: 5.42% V Ripple
- Steady State: 1.1KW
- iTHD: 3.14%
- Efficiency: 98.42%
## PF, THD & Efficiency

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<tr>
<th>Vin</th>
<th>Vout</th>
<th>Pin</th>
<th>Iout</th>
<th>Pout</th>
<th>Efficiency %</th>
<th>iTHD%</th>
<th>PF</th>
<th>%Rated Load</th>
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### Low Line

### High Line

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<tr>
<th>Vin</th>
<th>Vout</th>
<th>Pin</th>
<th>Iout</th>
<th>Pout</th>
<th>Efficiency %</th>
<th>iTHD%</th>
<th>PF</th>
<th>%Rated Load</th>
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Improved Transient Response

- Non Linear Voltage Loop
Fast Transient Response - Non Linear Voltage Loop

- Use parallel form of DCL Controller, enables to prevent integral term causing issues when changing voltage loop gain

\[
\text{Abs Voltage Error} = \text{Abs} (V_{\text{ref}} - V_{\text{fdbk}})
\]

\[
K_1 \leq \text{Abs} (V_{\text{ref}} - V_{\text{fdbk}}) < K_2 \]

\[
\text{abs}(V_{\text{ref}} - V_{\text{fdbk}}) > E_1
\]

Note the value is slewed to the new \( K_p \) gain to avoid any sudden changes.

Voltage Transient Waveform: Linear Voltage Loop (Left), Non Linear Voltage Loop (Right)

Overshoot Reduced from 51.2V to 16.8V
Transient Response at 120/230Vrms

DC Bus Voltage Vac 120Vrms
Step Load Change 0% to 50%
Current 14.3V Under-shoot
Non Linear Voltage Loop

DC Bus Voltage Vac 230Vrms
Step Load Change 3.3KW to 1.1KW
Current 41.5V Overshoot

DC Bus Voltage Vac 120Vrms
Step Load Change 50% to 0%
Current 16.8V Overshoot

DC Bus Voltage Vac 120Vrms
Step Load Change 100% to 50%
Current 15.7V Overshoot
Non Linear Voltage Loop
Improved Efficiency

- Adaptive Deadtime
ZVS Operation - Adaptive Dead Time Control

- The optimal dead time calculation
  - Waveforms are provided in different $t_{d,\text{on}}$
  - The optimal dead time: $t_{d,\text{on}} = \frac{2C_{\text{oss}}V_{\text{out}}}{i_{L,\text{peak}}}$

Q4 turns OFF => DT $t_{d,\text{on}}$ => Q3 turns ON
Adaptive Dead Time Control Implementation

In PFC, the operating point changes in every line cycle (60 Hz or 50 Hz), the optimal $t_{d,on}$ should be calculated in real time with respect to $i_{L,peak}$

A.D.T from individual $i_{L,peak}$ and $i_{L,AVG}$ show almost same efficiency

$$A.D.T = \frac{2C_{oss}V_{out}}{|i_{L,AVG}|}$$

Current sensor (AVG)

Current sensors (Individual)

![Diagram of current sensor and limiter]

Senseing $i_{L,AVG}$ → Absolute value function $|i_{L,AVG}|$ → Limiter → A.D.T Calculation $A.D.T = \frac{2C_{oss}V_{out}}{|i_{L,AVG}|}$ → Limiter → Update ePWM DBRED

$DBRED = A.D.T$
Adaptive Dead time Power Savings

Power savings data for using Adaptive Dead Time (20ns-200ns).
Power savings compared to fixed Dead Time of 100ns.

Vin 230V, 50Hz,

TI Information – Selective Disclosure
Improved Light Load Efficiency

➤ Phase Shedding Control
Light Load Efficiency Improvement - Phase Shedding

• The concept of phase shedding
  – Phase shedding technique is control the # of operating phases
  – It improves the light load efficiency

• State-machine for phase shedding control
  – The # of operating phase is determined by state machine
  – $I_{in} < I_1$, 1-Ph has the highest efficiency
    $I_1 < I_{in} < I_2$, 2-Ph has the highest efficiency
    $I_{in} > I_2$, 3-Ph has the highest efficiency
  – Hysteresis Band is used for reliable transition
Phase Shedding Control Implementation

• MCU (F28004x) Implementation
  – The # of phases is determined by state-machine
  – In state transition, PWM settings are changed near zero crossing point (PWM on/off, Phase shift)

Why?
In zero-crossing points, current goes down to zero and do not introduce disturbance from PWM configuration
Phase Adding

DC Bus Voltage

150W, single phase

Vac 110Vrms

1350W, three phase
Phase Shedding

DC Bus Voltage

1350W, three phase

150W, single phase

Vac 110 Vrms

Iac
Phase shedding Test Result (120V, 60Hz)

**Efficiency**

- **η enhancement**
- 1 Ph
- 2 Ph
- 3 Ph

**THD**

- **THD degradation**

**η Difference**

**Power Factor**

- **Similar PF**
Phase shedding Test Result (230V, 50Hz)

**Efficiency**

- **η enhancement**
- 1 Ph
- 2 Ph
- 3 Ph

**THD**

- **THD degradation**

**η Difference**

**Power Factor**

- **Similar PF**

---

[Graphs and data provided in the image]
Improved Light Load Power Factor (PF)

- Input Cap Compensation
Light Load PF Improvement - Input Cap Compensation

- Input capacitor current draw causes significant PF loss at high line and light load
- Execution of SPLL enables Vector Cancellation based techniques to adjust the current reference to compensate for PF loss
- At 10% load the improvement is ~ 18% and at 2% load more than 40% improvement
Other Improvements
Cost sensitive PFC application uses resistor divider network to sense the AC input voltage.

Totem Pole PFC PWM driver requires accurate zero crossing detection. This can be specially challenging with the low cost voltage sensing method.

Phase Locked Loop (PLL) Based AC angle is used to accurately detect the grid angle and change modulation based on that.

TMU on C28x CPU reduces cycle counts to run the PLL algorithm and enables integration on the current loop which can run at 100-200KHz.

### Table: PLL Algorithm Performance

<table>
<thead>
<tr>
<th></th>
<th>C28x FPU</th>
<th>C28x FPU + TMU</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPLL_1PH_SOGI</td>
<td>175</td>
<td>115</td>
</tr>
</tbody>
</table>

35% Improvement

**TP PFC Accurate Zero Cross Detection - SPLL with TMU**
Accurate PWM Generation for IL TP PFC - Type 4 PWM

- Interleaved topologies require PWM updates to happen in a given interval of time, otherwise an in-accurate pulse can be applied to the power converter. The time interval reduced with number of phases.

- Totem Pole PFC Topology requires PWM to be started and stopped in a particular sequence to reduce zero current spike. In addition to this the active switch is swapped from positive half to negative half of the AC sine wave.

- Type 4 PWM features such as shadowed dead band and shadowed action qualifier enable accurate generation of PWM pulses in a straightforward manner.

TI Information – Selective Disclosure
TIDA-0961
Interleaved TRM/TCM/CRM/BCM Totem Pole PFC Reference Design

C2000 System Solutions: Digital Power
TIDA-0961 Interleaved TRM Totem Pole PFC

**Features**

- TMS320F280xx Controller based full digital control PFC
- Wide input voltage range: 85 – 265 VAC
- Output Power: 1.6 KW, 4.1A @ 390V
- Efficiency: 99%; Power Factor : >0.99
- 200 kHz ~1.2MHz PWM switching
- Compact Form Factor (65 x 30 x 40 mm)
- Power density about **80W/in³**

**Benefits**

- **Super High Efficiency** makes thermal design simpler
- **Extremely compact** solution with low component count
- Makes compliance with **80 Plus Titanium specs** easier
- Integrated GaN FET and driver eases layout constraints
- High PF > 0.99 and less than 5% THD for 20% to full load
- High performance C2000 controller enables superior control scheme and high PWM frequency operation
- poweSUITE support enables easy adaptation of software
GaN at High Frequency – Soft Switching vs Hard Switching

V_{in}=200V, V_o=400V, P_o=1.2kW, F_s=500kHz
Boost Converter

Loss Breakdown @ 1.2kW

CCM Hard SW

CRM Soft SW

Soft switching significantly benefits GaN

* Source: CPES, Virginia Tech
High Frequency TP PFC Challenges
#1 Achieving ZVS across line-load and over full AC cycle

![Diagram of Totem-pole PFC](image)

- \( V_{\text{IN,RMS}} = 230\,\text{V}, \, V_o = 400\,\text{V}, \text{Full Load}, \, F_s = 1-3\,\text{MHz} \)

- Line-cycle Averaged Non-ZVS
  - High non-ZVS loss
  - 1MHz
  - 100kHz

- Valley Switching
  - \( F_s = 1.31\,\text{MHz} \)
  - \( F_s = 2.19\,\text{MHz} \)
ZVS Extension

Conventional Solution
- Inductor current zero crossing sensing
- Low SNR
- Worse under high-line low-load

C2x Solution
- Sensing voltage across the inductor
- On-chip CMPSS and type-4 PWM features on C2000 are used to solve this

* Source: CPES, Virginia Tech


ZVS Detection
ZVS Detection

- 3 control loops (Voltage, Current and ZVS)
- Blanking may also be implemented as part of CMPSS (comparator).
ZVS with AC Input

Positive half-cycle

Q4 turns ON

Negative half-cycle

Q3 turns ON

Positive half-cycle

Q4 turns ON

ZVS lost

Approaching ZVS

Vsw

Q3 turns ON

Vsw

Q4 turns ON
#2 Cycle Intensive Calculations

- Calculating correct turn-on and turn-off durations at every switching/control instant

Solution

- C2000’s TMU helps reduce the MIPS requirements considerably
  
  Example: From possible > 10us calculation time to <0.5us calculation time

Ton Calculations

\[
f_1(T_{\text{on}}) = \frac{V_{\text{in}}V_o}{V_o - V_{\text{in}}}L \cdot \frac{T_{\text{on}}^2}{2I_{\text{ref}} \sqrt{2LC_{\text{oss}}}} - \frac{T_{\text{on}}}{\sqrt{2LC_{\text{oss}}}} - \frac{V_{\text{in}}^2}{(V_o - V_{\text{in}})^2} \left( 1 + \frac{T_{\text{on}}^2}{2LC_{\text{oss}}} \right) - 1
\]

\[
f_2(T_{\text{on}}) = \frac{(V_o - V_{\text{in}})T_{\text{on}} + \sqrt{V_{\text{in}}^2T_{\text{on}}^2 + 2LC_{\text{oss}}(2V_{\text{in}}V_o - V_o^2)}}{(V_o - V_{\text{in}})\sqrt{2LC_{\text{oss}} - (V_o - V_{\text{in}})T_{\text{on}} \sqrt{V_{\text{in}}^2T_{\text{on}}^2 + 2LC_{\text{oss}}(2V_{\text{in}}V_o - V_o^2)}}
\]

\[
C = \frac{V_{\text{in}}^2(2V_o - V_{\text{in}})}{V_o(V_o - V_{\text{in}})} \cdot \frac{1}{2I_{\text{ref}}} \sqrt{\frac{2C_{\text{oss}}}{L}} - 2\pi - \frac{\sqrt{V_o^2 - 2V_{\text{in}}V_o}}{V_{\text{in}}} + \tan^{-1}\left( \frac{\sqrt{V_o^2 - 2V_{\text{in}}V_o}}{V_{\text{in}}} \right)
\]

Dead-time Calculations

- Possibility of negative current/current spikes
- Body diode losses
#3 Clean cross-over transitions

- High Freq TRM PFC uses small boost inductor and therefore small voltage across the inductor can cause fast current rise time.

- During AC voltage transitions, the stored charge across the output capacitance of the Si FET (in off state) discharges at a very high rate as soon as the GaN active FET is turned ON causing current spikes at zero crossing point.
#3 Clean cross-over transitions - Solutions

- Soft-start for active FETs during zero voltage crossover providing a soft transition
- Proper sequence to turn-on silicon FET and the GaN sync FET must be followed
- These are implemented using a software state-machine
What is missing?

– A clean and easy way to update multiple registers in a PWM module
– A clean and easy way to update registers in multiple PWM modules
Solution: One Shot & Global Reload (Type-4 PWMs)

One shot reload usage

Initialization
– Enable global reload
– Link GLDCTL2 registers

Run Time
– Update all registers
– Write ‘1’ to GLDCTL2[OSHTLD]
– Write ‘1’ to GLDCTL2[GFRCLD], if desired

TRM PFC operating at high switching frequencies also requires **hi-res dead-band (HRDB)** between the turn-off of the active FET and the turn-on of the sync FET.
Software Flowchart

C Environment

System Level Management

- Main
  - Initialization
    - 28x Device level
    - Peripheral level
    - System level
    - SFRA Init
    - ISR, ADC
  - Background Loop

Tasks:
- Timer 0
  - Trip level adjust
  - Fault management
  - Startup
  - Shutdown

Tasks:
- Timer 1
  - Instrumentation
  - SFRA Background
  - In-rush relay control
  - Serial comms

Background Loop

- PWM ISR
  - 10 kHz
  - EXIT

- ADC_VBUS()

- SFRA_INJECT()

- Vloop

- SFRA_COLLECT()

- EMAVG()

- Datalog (optional)

- Instrumentation (RMS calculations)

- Phase Shedding

- OVP

Crossover state machine. SW PLL

- PWM register updates

- AC Cycle/Crossover

- PWM register updates

- Adjust Period (fsw)

- NO

- YES

- Duty preservation

- ZVS adjust req'd?

- PWM global update

- Adjust Period (fsw)

- Phase adjustment (if needed)
Input Voltage, Current and Output Ripple

- **High line, Pout = 600W**
- **Low line, Pout = 450W**
- **Low line, Pout = 1350W**
- **High line, Pout = 1500W**
ZVS Across AC Cycle

Low Line, Full Load, +ve Cycle

High Line, Full Load, +ve Cycle

Low Line, Full Load, -ve Cycle

High Line, Full Load, -ve Cycle
Phase Adding/Shedding
Phase Shedding – Low Line & High Line

Low line, $P_{out} = 1480W$

Low line, $P_{out} = 440W$

Low line, $P_{out} = 890W$

High line, $P_{out} = 1630W$

High line, $P_{out} = 440W$
Turn-on Characteristics

High Line Low Load (300W)

High Line Full Load (1800W)
Two Phase Interleaved PFC

P.F. Vs Pout

- Vin = 230V, 50Hz
- Vin = 120V, 60Hz

%THD Vs Pout

- Vin = 230V, 50Hz
- Vin = 120V, 60Hz

Texas Instruments
Two Phase Interleaved PFC

%Ƞ Vs Pout

Vin = 230V, 50Hz
Vin = 120V, 60Hz

%Ƞ
Pout (W)

2nd Phase ON
Phase Shedding
2nd Phase ON

Vin = 230V, 50Hz
Vin = 120V, 60Hz
Thank You