High-Speed Layout Guidelines for Reducing EMI for LVDS SerDes Designs

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Introduction

• LVDS SerDes helps to reduce radiated emissions, but does not completely eliminate them

• EMI prevention must be considered early in the design process
  – Ensure the PCB is compliant with PCB guidelines for high-speed signals
Initial considerations

- Create a diagram with the functional groups of the system
- Identify the sensitive signals (clock signals, impedance controlled signals, etc.)
- Clarify frequency requirements
- Clarify trace length and cable length requirements
PCB Stack-Up and Board Layout

• At minimum, select a PCB with at least four layers

• Use dedicated ground and power planes
  – Avoid cutting up the power and ground planes if possible
  – Keep the power and ground plane surface area equivalent in size and shape

• Keep traces as short as possible

• Keep single-ended signals away from differential traces (at least 2x the trace width)

• Place ESD susceptible circuitry at the center of the PCB
Serializer and deserializer location

- The serializer and deserializer should be located as close to the connector as possible
Device ground and power

• Use solid power and ground planes
  – Minimize current loops

• Do not route over plane-splits
  – Use 1μF or lower stitching capacitors across the split if routing is completely unavoidable
Device ground and power

• Separate digital and analog power supplies with filtering and bypassing

• Use multiple vias for both power and ground connections

• Use ferrite beads to decouple the IC power from the rest of the supply system
Device bypass

- To obtain supply noise 20 mVpp and lower, close bypassing is required
  - Put the largest value filter capacitors near power connectors and supply inputs

- Place high-quality X7R decoupling capacitors as close as possible to device pins
  - Use multiple capacitors (0.1uF, 0.01uF, 1uF) in parallel
  - Connect the pad of the capacitor directly to a via to the ground plane with 2 or 3 vias.
Device bypass

- Keep traces from decoupling caps to ground as short and wide as possible
- Ensure that decoupling capacitors are on the same layer as the device
- Do not place vias between decoupling capacitors and the IC
- Do not neglect PLL power-pin bypassing as it is the most critical of low noise operation
- 0805 or 1206 chip caps are recommended
LVDS traces

- Traces should be 100Ω (±5%) differential impedance of microstrip or differential stripline

- The spacing between LVDS signal pairs and other signals should be a minimum of 2x the width of the trace
  - 5x would be best

- The spacing between individual conductors of an LVDS pair should be less than 2x the width of the trace
LVDS traces

- Trace lengths should be matched (generally within 5mm of each other) to reduce inter-pair and intra-pair skew

- Route LVDS pairs symmetrically and parallel to each other
LVDS traces

• Avoid right-angle traces
  – 45° corners are acceptable, but rounded corners and best
LVDS traces

• A stub should be as short as possible and no longer than 2cm to 3cm

• Place termination resistors as close as possible (no more than ½ inch away) to the deserializer input pins

• Route traces with the most direct route and minimum trace length to the connector

• Ensure the termination resistor matches within 2% of the differential impedance of the media (typically 100Ω)
LVDS traces

• Do not route traces near or under
  – the edge of the PCB
  – Crystals
  – Oscillators
  – Clock signal generators
  – Switching power regulators
  – Mounting holes
  – Magnetic devices
  – ICs that use or duplicate clock signals

• Do not place probe or test points on any LVDS traces

• Any discontinuities that occur on one signal line of an LVDS pair should be mirrored on the other signal line
Connectors and cables

• Use shielded, high-speed connectors that have complete shielding around the connector interface

• Keep the impedance of the LVDS traces matched across transitions such as connectors

• When using a ribbon cable, place a ground line between each LVDS pair
Connectors and cables

• Twin-coax cables have the overall best performance
  – Low cable skew
  – Low EMI
  – Double shielding
  – Short and long applications

• Utilize a shield on each cable pair for twin-coax cables
  – Faster speeds
  – Longer distances
  – Reduced EMI
## Identifying EMI root cause

<table>
<thead>
<tr>
<th>Step</th>
<th>Source</th>
<th>Serializer</th>
<th>Deserializer</th>
<th>Other System Components</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>Captures ambient noise</td>
</tr>
<tr>
<td>2</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Serializer by itself</td>
</tr>
<tr>
<td>3</td>
<td>Off</td>
<td>Off</td>
<td>On</td>
<td>Off</td>
<td>Deserializer by itself</td>
</tr>
<tr>
<td>4</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>Serializer+deserializer+serializer source</td>
</tr>
<tr>
<td>5</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Slow down clock rise/fall times by putting capacitance at the clock pin</td>
</tr>
<tr>
<td>6</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Shield serializer board and connect the shield to a solid ground</td>
</tr>
<tr>
<td>7</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>On</td>
<td>Change to a better-shielded cable</td>
</tr>
</tbody>
</table>
Conclusion

• Follow the guidelines listed in this video to ensure LVDS SerDes designs are EMI compliant

• If issues are encountered, identify the root cause with the table in the previous slide

• Reference TI’s EVM schematic and layouts

Thanks for your time!