How to Design Multi-kW Converters for Electric Vehicles

Colin Gillmor: (HPC), email: colingillmor@ti.com

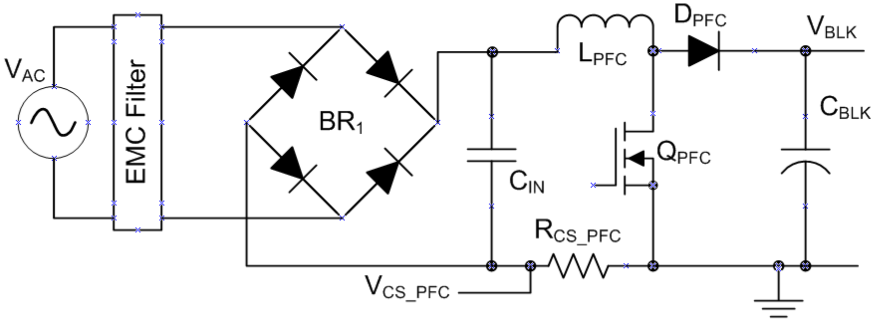
Boost PFC Topology

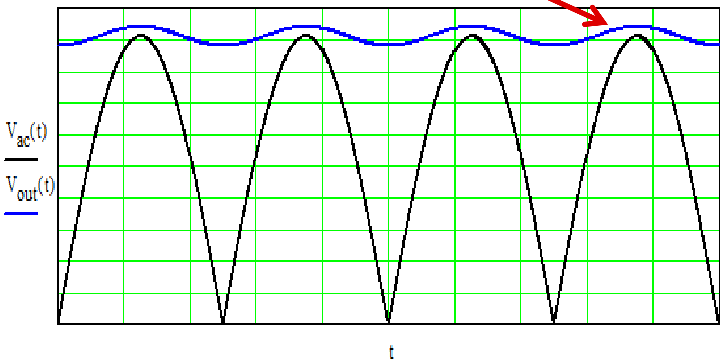
- Popular Because
  - Sinusoidal AC line current
  - Power Factor is high

DCM: Discontinuous Conduction Mode: 75W to 100W
TM: Transition Mode: 100W to 300W
CCM: Continuous Conduction Mode 150W to 1kW
Interleaved CCM > 1kW

- Output Voltage must be higher than input
  - Typically 400V

Inherent Ripple voltage on Vout at 2 x F_{line}



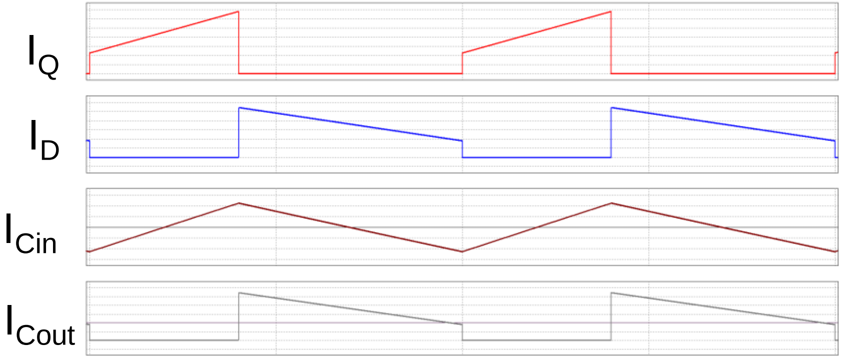


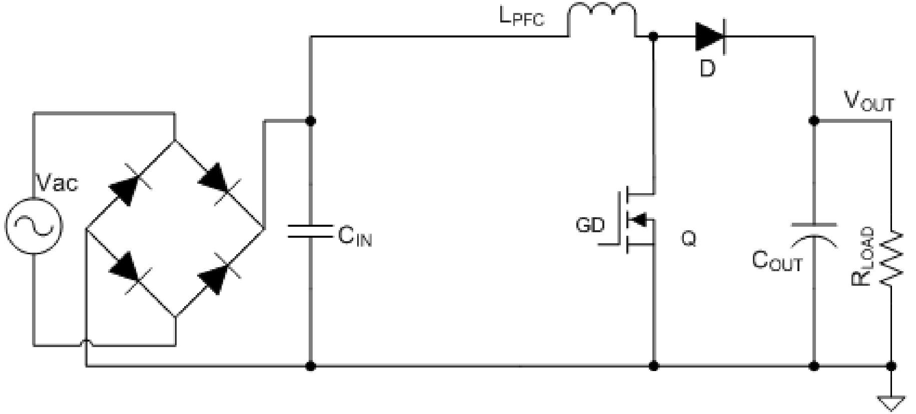
TM = Boundary Conduction Mode = Critical Conduction Mode

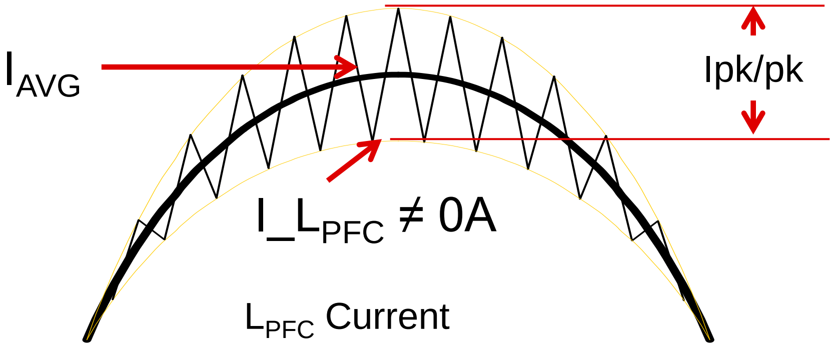
Boost PFC - CCM

- CCM   Continuous Conduction Mode
- Fixed Frequency
- Average or Peak Current mode control
- Ultra Fast rectifier Diode (eg SiC)
  - Inductor current not zero at turn-off
  - Qrr is significant
- Sinusoidal current in L_{PFC}

Typical currents over two switching cycles



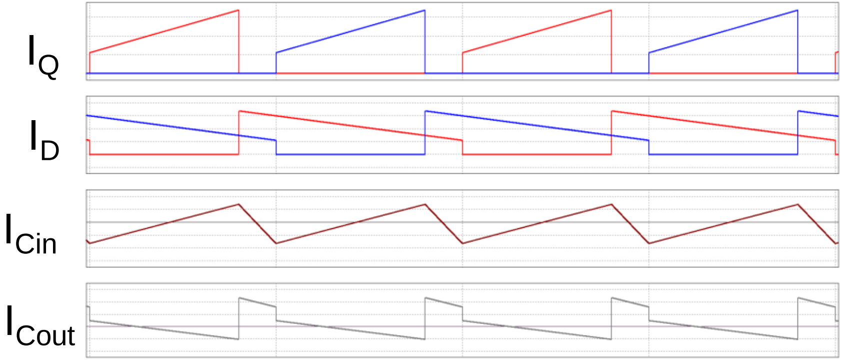


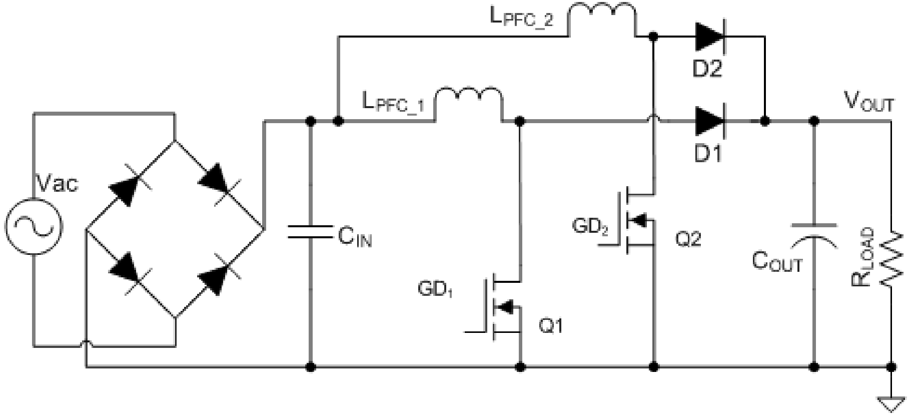


Boost PFC - Interleaving

- Two Boost stages with180° phase shift
- Reduces ripple current in Cin and Cout *
  - Smaller EMI filter
  - Smaller Cout
- Distributes power loss over more parts
- Extends operating power range
  - CCM: 4kW +
- Phase shedding.
  - Turn one phase off at light load
- Controller
  - UCC28070-Q1, Interleaved CCM

Typical currents over two switching cycles



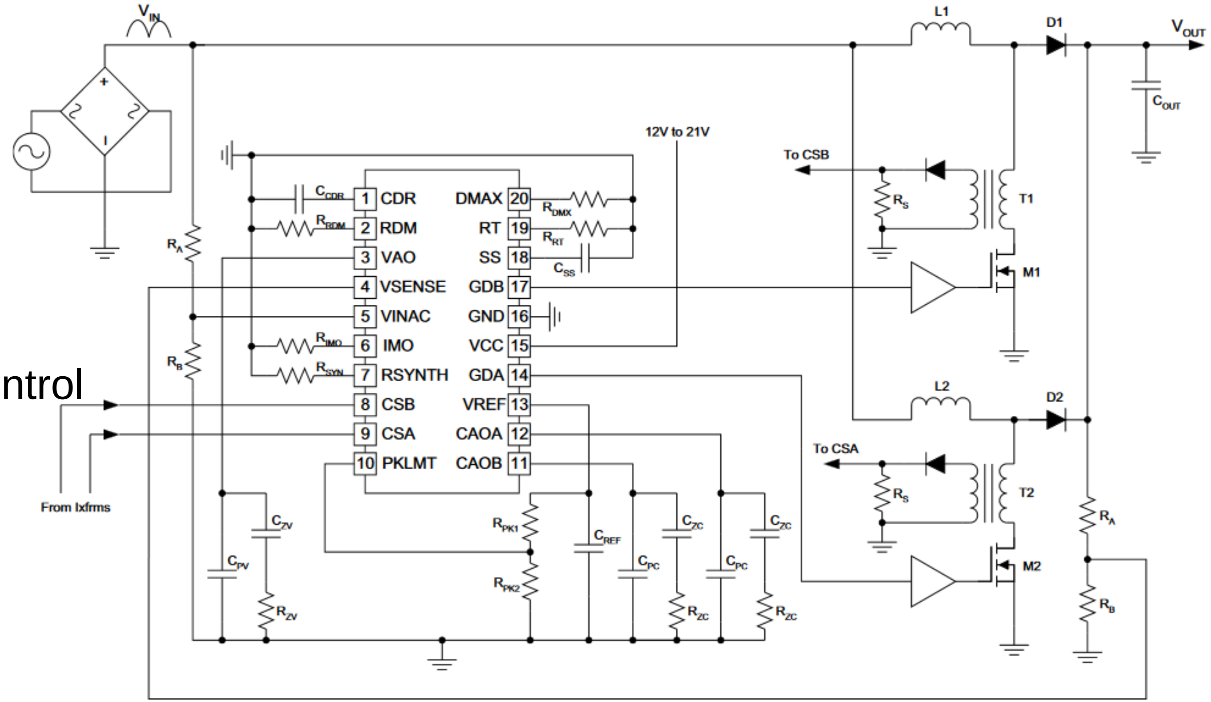


* See Ref 1, 2, 3, 4, 5 for more information

Boost PFC - Interleaving

- UCC28070-Q1 controller

Simplified Application Schematic



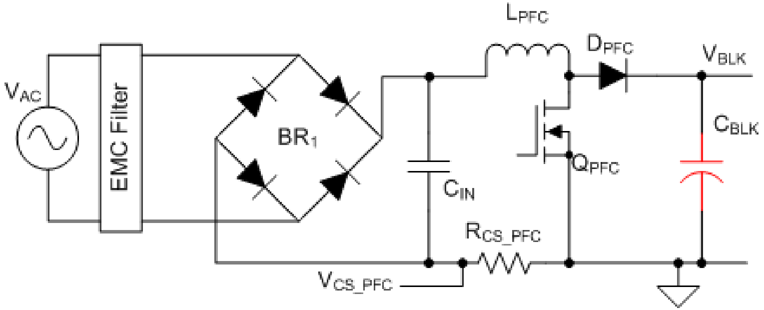
- Near Unity PF
- 2 Phase Interleaving
- Average Current Mode Control
- Current Sharing
- Enhanced Load and Line Transient Response

PFC Bulk Capacitor

- Bulk Caps store a lot of energy
  - Make sure you discharge them before handling
- Ripple current rating –
  - HF ripple at switching Frequency, Complex calculation
  - Interleaving gives typically 40% to 50% reduction over non-interleaved case
    - See Ref 1, 2, 3, 4, 5, 6
  - Low Freq at 2x Line frequency, not affected by interleaving. →

$$I_{Cout\_LF} = \frac{\eta P_{in}}{\sqrt{2}\, V_{OUT}}$$

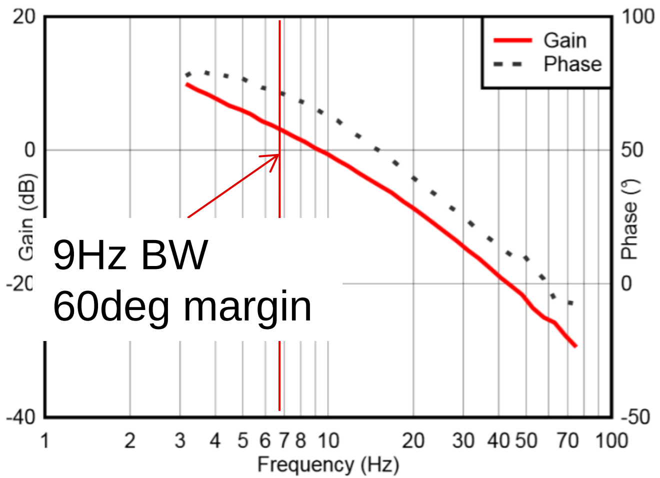
  - Increases as frequency increases.
  - Decreases as Temp increases
- ESR
  - Reduces as Freq increases
- Temperature and Lifetime rating considerations
  - Lower Temperature implies longer lifetime

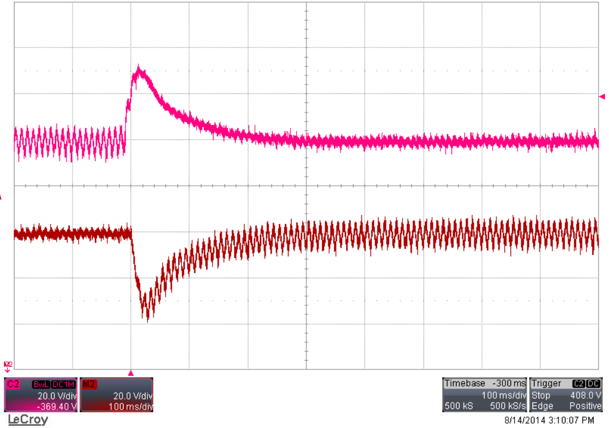


PFC Control – Compensation

- Loop stability tests ensure stable operation
  - Bode Plots, Small Signal
  - Look for gain and phase margin

  - Transient Tests, Large Signal
  - Look for acceptable voltage deviations and
  - Both types of test are necessary





- Overall Loop
  - Good PFC / low iTHD
  - Good output voltage regulation

- L_PFC value does not appear in loop transfer equations

How to Design Multi-kW Converters for Electric Vehicles

Thank You

Colin Gillmor: (HPC), email: colingillmor@ti.com