

How to Design Multi-kW Converters for Electric Vehicles

- Part 1: Electric Vehicle power systems
- Part 2: Introduction to Battery Charging
- Part 3: Power Factor and Harmonic Currents
- Part 4: Power Factor Correction
- Part 5: The Phase Shifted Full Bridge
- Part 6: How the PSFB works
- Part 7: A High Power On Board Charger Design
- Part 8: MOSFET gate driver considerations and References**

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Gate Driver Transformers

Advantages

- Primary/Secondary Isolation
- Simple (in theory)
- Zero Quiescent Current
- No start-up delay
- No bootstrap cap to charge
- Robust

Disadvantages

- High Component count
- Bulky in comparison to IC
- Need drivers to drive primary
- Need series Cap to prevent DC current
- Prone to saturation if not driven correctly

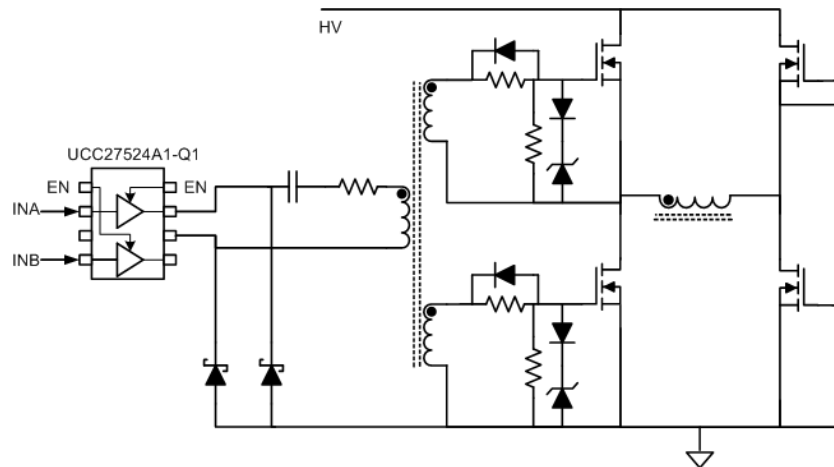
Tradeoff -

Good Pri/Sec coupling:

- Low leakage inductance, High pri/sec capacitance
- Large CM currents, can 'upset' driver

Poor Pri/Sec coupling:

- Large leakage inductance, low pri/sec capacitance
- Large spikes due to leakage – must be clamped



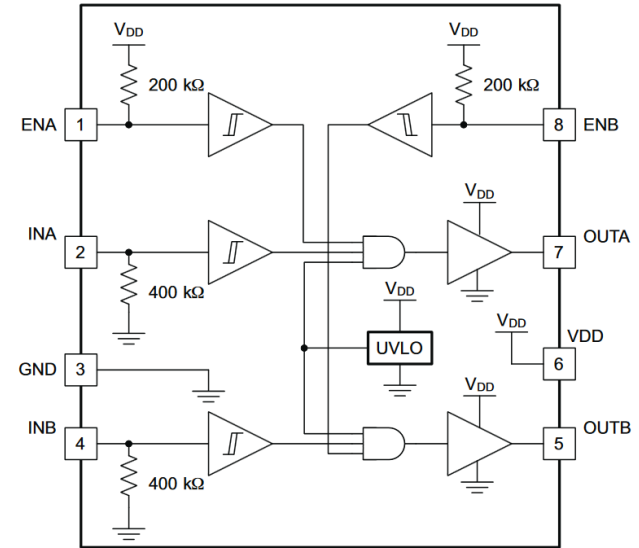
Gate Driver Considerations

- MOSFET gate appears as a capacitor (to a good first approximation)
- Aim is to reduce MOSFET switching losses
- Drive MOSFET gate correctly –
 - Keep MOSFET OFF when it is supposed to be OFF
 - Keep MOSFET ON when it is supposed to be ON
- MOSFET turn-on and turn-off times must be minimised
- Needs a low impedance source
- High peak currents (4A to 5A typ) but Low average currents

Driver may or may not have to cross an isolation barrier

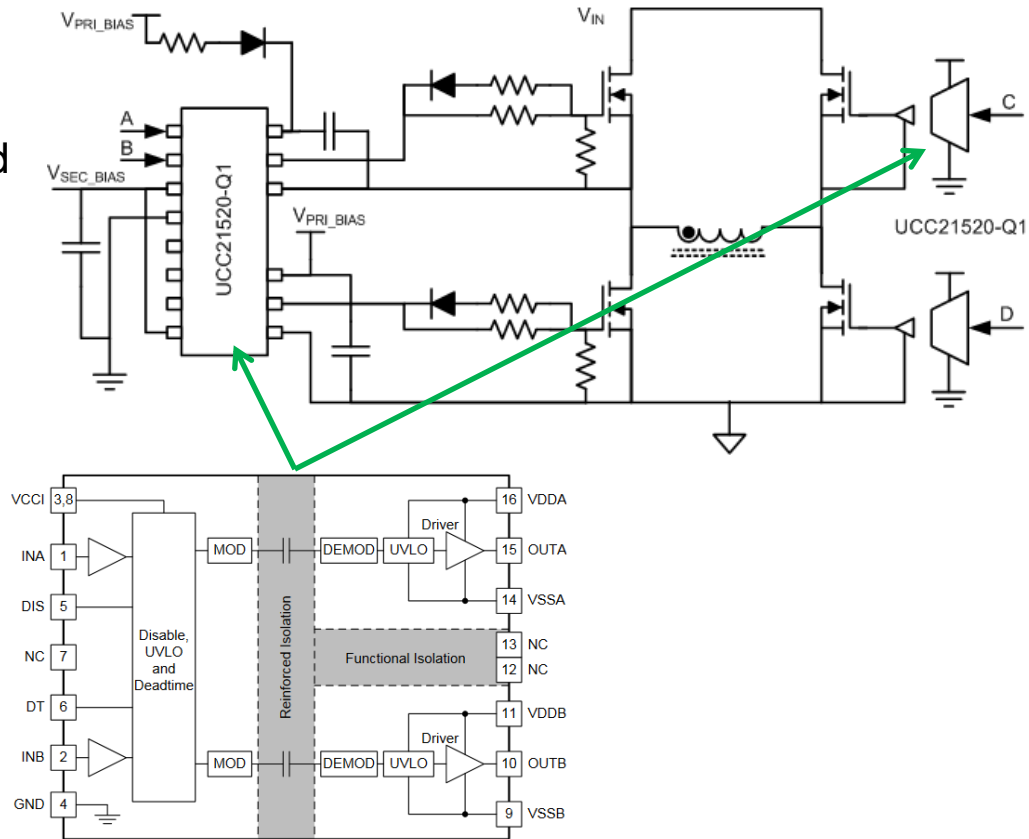
Low side Driver – MOSFET is Ground referenced

High side Driver – MOSFET is not Ground referenced



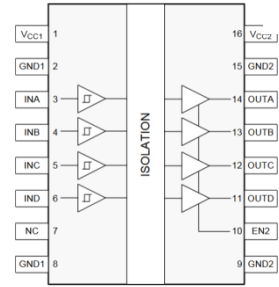
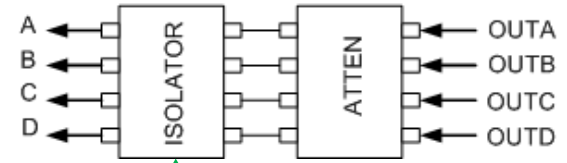
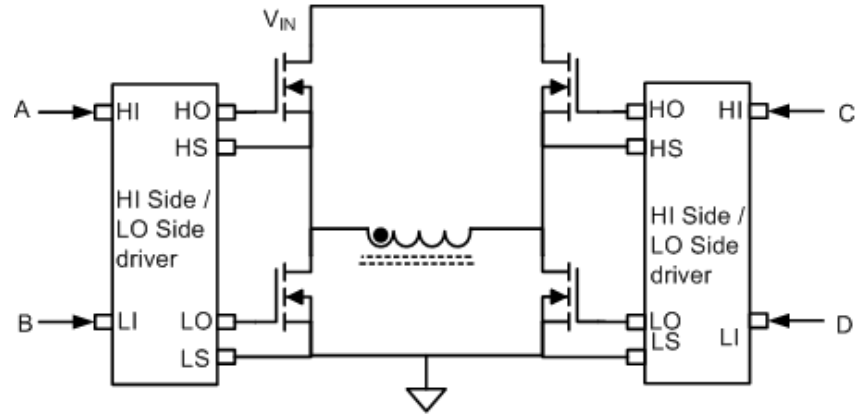
On Board Charger: Isolated Driver, Option 1

- Primary/Secondary Isolation
- Switching of Primary side MOSFETs
- High Side and Low Side outputs needed
- 4 isolated outputs in total
- 2 high side drives, 2 low side drives
- Isolation to $5.7\text{kV}_{\text{RMS}}$
- 2 x UCC21520-Q1, 4A, 6 A driver
- Low Propagation Delays
- Good Propagation Delay Matching
- Adjustable Dead Time
- Safety Features, UVLO etc.
- As with all drivers, PCB layout is critical



On Board Charger: Isolated Driver, Option 2

- Pri/Sec Isolation
- ISO7740-Q1 provides pri/sec isolation
 - 5kV RMS
- 0/10V signal from UCC28951-Q1 needs attenuation (2:1) to meet ISO7740-Q1 input level.
- Gate drivers drive the MOSFETs
- ISO7740FQDWQ

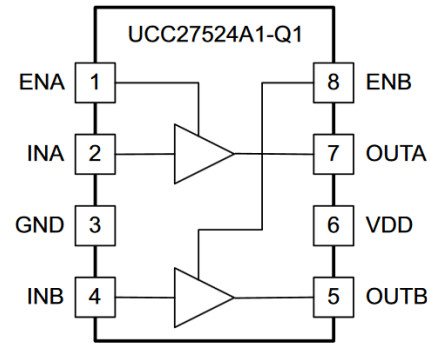
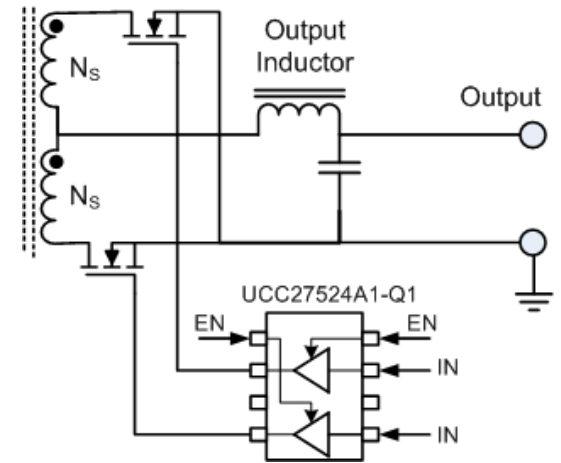


- F option – outputs default LOW !

ISO7740F-Q1

UCC27524A1-Q1 Gate Driver IC

- UCC27524A1-Q1 Dual 5-A High-Speed, Low-Side Gate Driver
 - Drive SRs
 - Drive Primary Side MOSFETs
- Two independent channels
- Independent enable on each channel
- Fast, matched rise and fall times
- Outputs LOW when inputs floating
- SRs are large rectifier MOSFETs.
 - Up to 5A peak for fast turn-on and turn-off



Design Resources

- Power factor correction (PFC) controller
 - <http://www.ti.com/lscs/ti/power-management/power-factor-correction-overview.page>
- Isolated DC/DC controller
 - <http://www.ti.com/lscs/ti/power-management/pwm-resonant-controller-overview.page>
- TI Reference designs
 - <http://www.ti.com/general/docs/refdesignsearchresults.tsp>
- Technical Support at TI E2E™ Community
 - <https://e2e.ti.com/>
- High Volt Interactive Training Series
 - <https://training.ti.com/high-voltage-training>
- Power Topologies Quick Reference Guide
 - <http://www.ti.com/lit/ug/slyu032/slyu032.pdf>
- Power Topologies Handbook
 - <https://www.ti.com/seclit/ug/slyu036/slyu036.pdf>
- Power Supply Design Seminars
 - <http://www.ti.com/ww/en/power-training/login.shtml?DCMP=pwr-psds-archive&HQS=pwr-psds-archive-psds>
- Power Stage Designer™
 - <http://www.ti.com/tool/powerstage-designer?DCMP=powerstagedesigner&HQS=powerstagedesigner>
- Introduction to Power Electronics
 - <https://training.ti.com/introduction-power-electronics?HQS=pwr-null-null-pentonever-asset-tr-null-ww>

References

Ref 1: Fundamentals of Power Electronics, Erickson and Maksimovic; Springer 2001, Table 18.3, summary of rectifier current stresses.

Ref 2: Analytic Expressions for currents in the CCM PFC stage, <http://www.ti.com/lit/ml/slyy131/slyy131.pdf> , Gillmor.

Ref 3: Predicting output-capacitor ripple in a CCM boost PFC circuit, https://e2e.ti.com/blogs_/b/powerhouse/archive/2016/06/14/predicting-output-capacitor-ripple-in-a-ccm-boost-pfc-circuit Gillmor

Ref 4: SLUP279 An Interleaving PFC Pre-Regulator for High-Power Converters. O'Loughlin

Ref 5: Capacitor Ripple current in an interleaved PFC converter, Pratt and Jinsong, IEEE transactions on Power Electronics, Vol 24, No 6 June 2009.

Ref 6: <http://www.ti.com/lit/an/slua479b/slua479b.pdf> Interleaved PFC design review. O'Loughlin

[Blog: Are-you-ready-for-totem-pole-pfc](#)

[GaN FET-Based CCM Totem Pole Bridgeless PFC](#)

[Magnetics Design Handbook, Dixon.](#)

[Understanding the basics of flyback converter design](#)

Synchronizing Three or More UCC28950 PSFB Controllers <http://www.ti.com/lit/an/slua609/slua609.pdf>

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Thank You

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