Introduction to Processor SDK Radar – Part 2
Agenda

• What is Processor SDK Radar?
  – Radar SDK Software Stack

• Processor SDK Radar Processing Chain
  – Algorithm Blocks (FFT, Peak Detection, Beam Forming)
  – Cascade Radar Data Processing Chain

• Getting Started with Processor SDK Radar
Radar Data Processing flow

1. RFFT
   - Range Complex Pts
2. DFFT
   - Doppler Complex Pts
3. Doppler Correction
   - Range x Doppler
   - Point to point multiply
4. Tx Decoding
   - Range x Doppler
   - Actual samples (or Detected objects)
5. Detection
   - Log Mag, SUM
   - For Detected objects (or actual samples)
6. Beam Forming
   - Range x Doppler
   - For Detected objects
7. CLUSTERING and POST PROCESSING
   - N_ANT
   - For Detected objects
Single Chip AWR1243 based Object Detection using Processor SDK – Radar on TDA3xx

- This usecase demonstrates the EVE object detection computation.
- The data flow shows a radar data capture for a configuration of 128 samples per chirp and 128 chirps per frame @ 15 FPS for 4 Rx Antenna and 2 Tx Antenna.
A single radar algorithm link exposes the FFT, Peak Detection and Beam forming algorithm modules.

This is achieved by the concept of “Algorithm Function”.

The Algorithm link takes care of buffer management for single input and single output queue.

Processor SDK Radar Users can develop their own Radar Processing algorithms and use the algorithm plugin and algorithm function infrastructure to create their own Radar processing.

```bash
PROCESSOR_SDK_RADAR_xx_xx_xx_xx\vision_sdk\apps\src\rtos\radar\src\alg_plugins
```
Algorithm Modules (FFT)

- **Kernels**
  - **FFT**: 64, 128, 256, 512, 1024 point FFT kernels (16-bit fixed point with shift control at each stage, overflow detection)
  - Interference zero out
  - DC offset
  - Windowing
  - Doppler correction

- **Applet**
  - XDAIS based interface
  - Control to enable/disable interference zero out, DC offset, windowing and Doppler correction
  - DMA based data flow using internal memories for data processing
Algorithm Modules (Peak Detector)

Peak Detector

- Tx decoding
- Log magnitude & SUM
- CFAR-CA detection

• Kernels
  - Tx decoding
  - Log magnitude, sum
  - CFAR-CA detection

• Applet
  - XDAIS based interface
  - Control to enable/disable Tx decoding
  - Control for energy computation for detection to be sum of log magnitude vs direct energy sum
  - Control for cell sum direction (range vs doppler)
  - DMA based data flow using internal memories for data processing
Algorithm Modules (Beam forming)

Beam forming

- **Matrix multiply**
- **Energy computation**
- **Peak localization**

**Kernels**
- Matrix multiply
- Energy computation
- Peak Localization

**Applet**
- XDAIS based interface
- DMA based data flow using internal memories for data processing

PROCESSOR_SDK_RADAR_xx_xx_xx_x	i_components\algorithms\eve_sw_xx_xx_xx_xx\apps\beam_forming
System architecture: Cascade FMCW radars

MIMO cascade with synchronous radars

2 PCB system, Up-to 192 radar virtual array combinations
Radar front-end few inches from processors

Highly configurable frequency modulated continuous wave radio frequency transceivers with 76-81 GHz band which support up to 3 transmit (Tx) and 4 receive (Rx) chains

Highly optimized and scalable family of TI ADAS devices. Mix of TI’s fixed and floating-point TMS320C66x digital signal processor (DSP), Vision/Vector AccelerationPac (EVE), ARM Cortex-A15 MPCore™ and dual-Cortex-M4 processors.
4-Chip Cascade Radar Data Flow

![Diagram of 4-Chip Cascade Radar Data Flow](image-url)
Radar System Planner

- Excel Based Utility to analyze the Radar processing requirements on TDA devices.

<table>
<thead>
<tr>
<th>Configurations</th>
<th>Range Dimension</th>
<th>Doppler Dimension (per Tx)</th>
<th>Rx</th>
<th>Ts</th>
<th>Frames/sec</th>
<th>Multiplexing across Ts</th>
<th>Detection Method</th>
<th>Detection/dwells</th>
<th>Number of Angles (Angle resolution)</th>
<th>System Overhead</th>
<th>Virtual Antennas</th>
<th>Rx samples/dwell (cube size)</th>
<th>Plane size (range * doppler)</th>
<th>#Raw samples/dwell</th>
<th>Plane size (range * doppler)</th>
<th>BeamForming Matrix Columns</th>
<th>Sample size (in bytes)</th>
<th>Sample size (in bytes)</th>
<th>Processing/Memory subsystem</th>
<th>Cores</th>
<th>%Loading</th>
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SOC Utilization Summary

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SOC Utilization Summary

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Drawing for SOC Utilization Summary

Texas Instruments
Looking for Support?

• Use TI E2E forum to get additional support
• Kindly post queries/feedback on below forum
  – https://e2e.ti.com/support/arm/automotive_processors
Thank you