Jacinto™ 7 processors: application-specific hardware accelerators
Application-specific hardware accelerators

- Key features and benefits
- Heterogeneous processing cores
- **Application-specific hardware accelerators**
- Device management architecture
- Memory architecture and data movement
- Safety and isolation features
- Virtualization features
- Security features
- Power management features
- Network connectivity
- Flash and storage
- Serial connectivity

DRA829V/TDA4VM superset device representation
Capture, vision and imaging HWAs

Capture, vision and imaging:
- 2x CSI2 4-lane camera interface (+ 1x transmit)
- Vision Pre-Processing Accelerator (VPAC)
- Depth and Motion Perception Accelerator (DMPAC)

- >10 years of learning in ADAS systems
- 7th generation image processor
- Pixel-processing HWAs improve effective CNN-based deep learning performance
Capture, vision and imaging:

- 2x CSI2 4-lane camera interface (+ 1x transmit)
- Vision Pre-Processing Accelerator (VPAC)
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Features:

- Flex CFA
- Pyramid
- WDR+
- Designed for multi-modal sensor fusion systems
- Camera
- LIDAR
- Radar
- Ultrasound

VPAC

- Vision processing
- ISP
- Noise
- Scalar
- Re-map

DMPAC

- Depth and motion
- Stereo Depth Engine (SDE)
- Dense Optical Flow (DOF)

UNIQUE SOLUTIONS

- >10 years of learning in ADAS systems
- 7th generation image processor
- Pixel-processing HWAs improve effective CNN-based deep learning performance

Enables lower system cost:

- ISP Chip
  - Stereo disparity processing
  - Dense optical flow
  - Radar processing

Augments CNN/DL performance:

- Dense optical flow (vs. sparse)
- High-resolution stereo (vs low resolution)
- Algorithmic functional safety
Deep learning algorithm HWAs

Jacinto 7 optimizes data flow for deep learning:
- Improves performance utilization of the processor
- Minimizes off-chip accesses to reduce system BOM/power

Streaming Engine (SE) enables streaming-based, in-line, 6-dimensional, high-bandwidth data movement.

Multi-Core Shared Memory Controller (MSMC) enables slice-based approach to minimize external SDRAM memory accesses.

High performance (fps/TOP), latency, and memory usage

TI Deep Learning (TIDL) software framework realizes optimal data flow and facilitates ease-of-use.

Device | Network | FPS | DL TOPS | Latency | Memory
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Jacinto 7 | InceptionNetv1 | 1000 | 8 | 1 frame | 32b LPDDR4
Competition | InceptionNetv1 | 700 | 20 | 4 frames | 256b LPDDR4
TI deep learning (TIDL) CNN solution

Optimized for real-world performance

Optimized for higher resolution (0.5-4 MP) and lower latency (Batch size = 1) (It is not just TOPS rating)

Optimized solution for modern networks MobileNet, ResNet, ShuffleNet, etc.

Highly optimized for Automotive Market

DDR speed & interface optimized

Lowest number of DDR interfaces & speed using TI proprietary technology

ISO 26262

Designed for lower power
Enables fan-less design

Designed for functional safety

Flexible for multiple applications

Object detection
Semantic segmentation
Motion segmentation
Parking spot detection
Display processing HWAs

Display processing subsystem:

- High-performance, flexible display controller with pixel processing
- Flexible output protocol options:
  - Display serial interface (v1.3)
  - Embedded display port (v1.4)
  - Display parallel interface
- 4 video pipes + writeback
  - Multi-format with scaling
- 4 overlay managers
- Up to 8k pixel output
  - Flexible frame size
- Frame-buffer decompression
- Multi-port load balancing
- Rich safety and isolation features:
  - Pipe isolation and control
  - Freeze frame detection
- Page address translation support for real-time de-fragmentation
Video processing HWAs

**Video decode:**
- PowerVR D5520MP2 video processing unit from Imagination Technologies
- Dual-core multi-standard video decoder
- Decode up to 1x 4k60 / 2x 4k30 / 4x 1080p60 / 8x 1080p30 streams
- Formats H.265, H.264, WMV-9, VC1, MPEG2 and others
- Hardware scaling and rotation
- Secure playback support

**Video encode:**
- PowerVR VXE384MP2 video processing unit from Imagination Technologies
- Dual-core multi-standard video encoder
- Encode up to 1x 1080p60 / 2x 1080p30 streams
- Formats H.264 MVC/HP/MP/BP, MPEG-4 SP, H.263BP and others
- Hardware scaling, motion estimation and other accelerations
For more information

• For more training on Jacinto 7 processors: http://training.ti.com/jacinto7
• Order TDA4VM Jacinto Automotive processors for ADAS & autonomous vehicles: http://www.ti.com/product/TDA4VM
• Order the TDA4VMx evaluation module: http://www.ti.com/tool/TDA4VMXEVEM
• Order DRA829V Jacinto Automotive processors for gateway & vehicle compute: http://www.ti.com/product/DRA829V
• Order the DRA829Vx evaluation module: http://www.ti.com/tool/DRA829VXEVM
• For questions regarding topics covered in this training, visit the processors support forum at the TI E2E Community website: https://e2e.ti.com