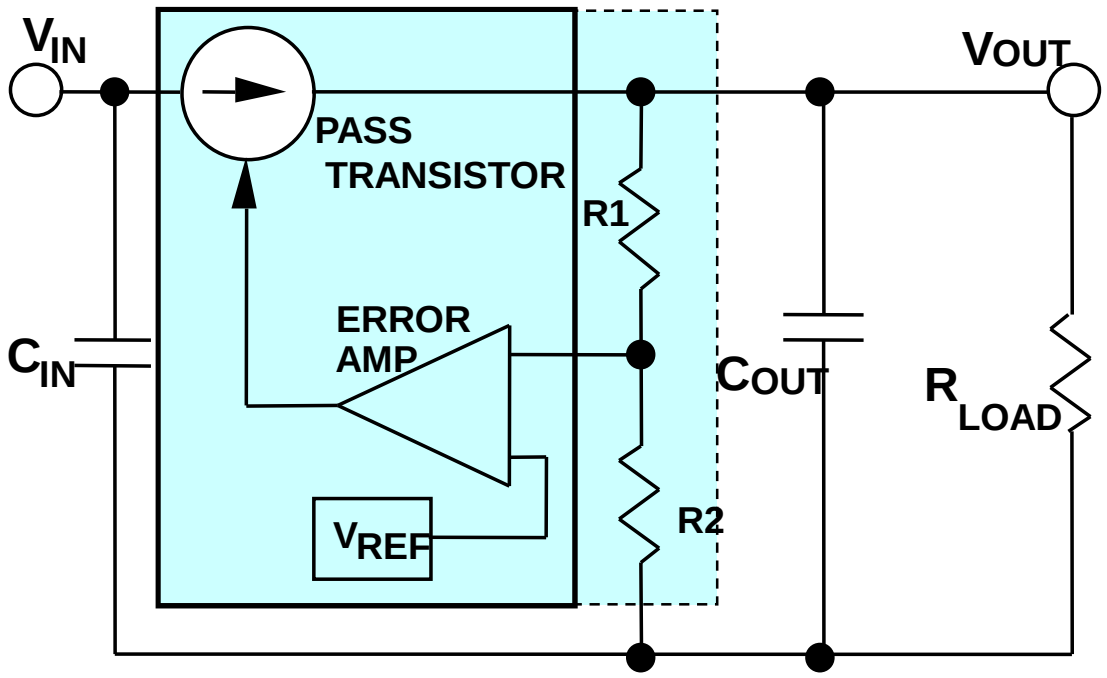
Linear Regulator Fundamentals

2.5 PMOS

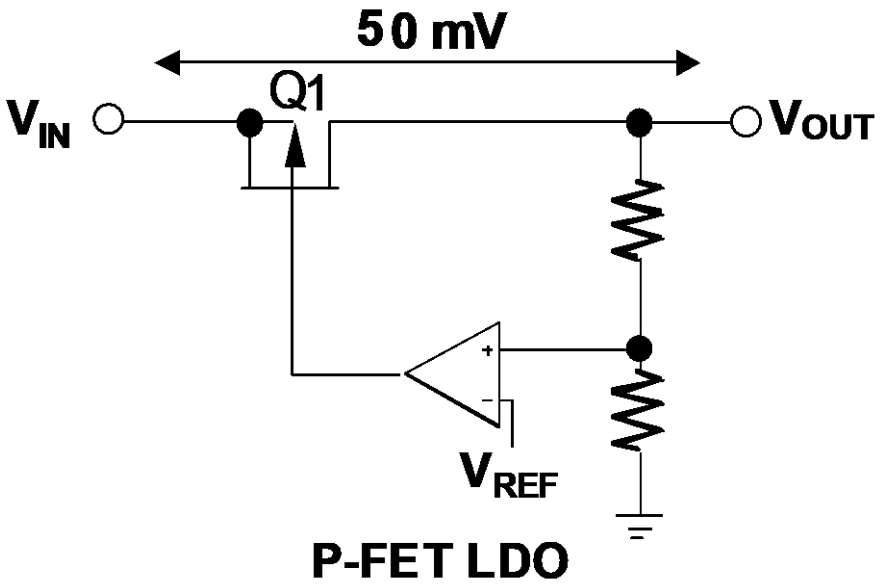
Linear-Regulator Operation

- Voltage feedback samples the output R1 and R2 may be internal or external
- Feedback controls pass transistor's current to the load

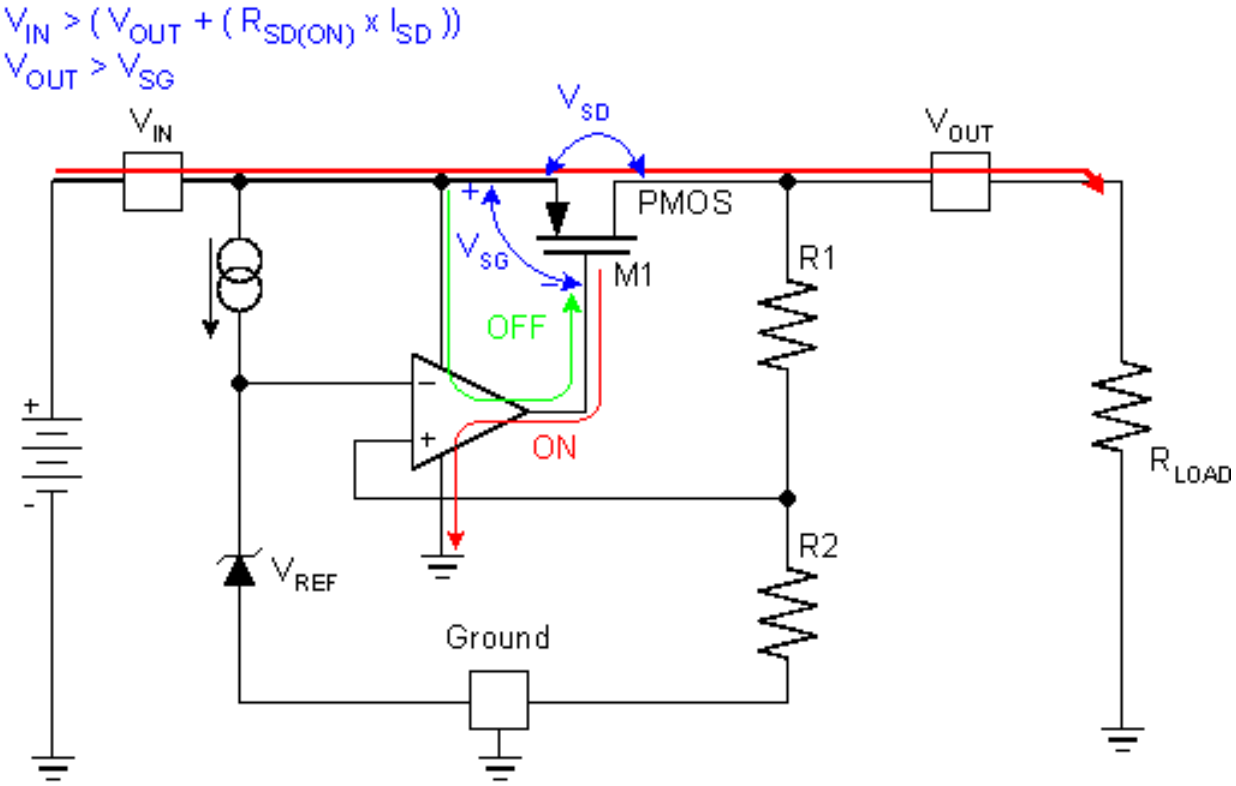


P-FET-LDO Linear Regulators

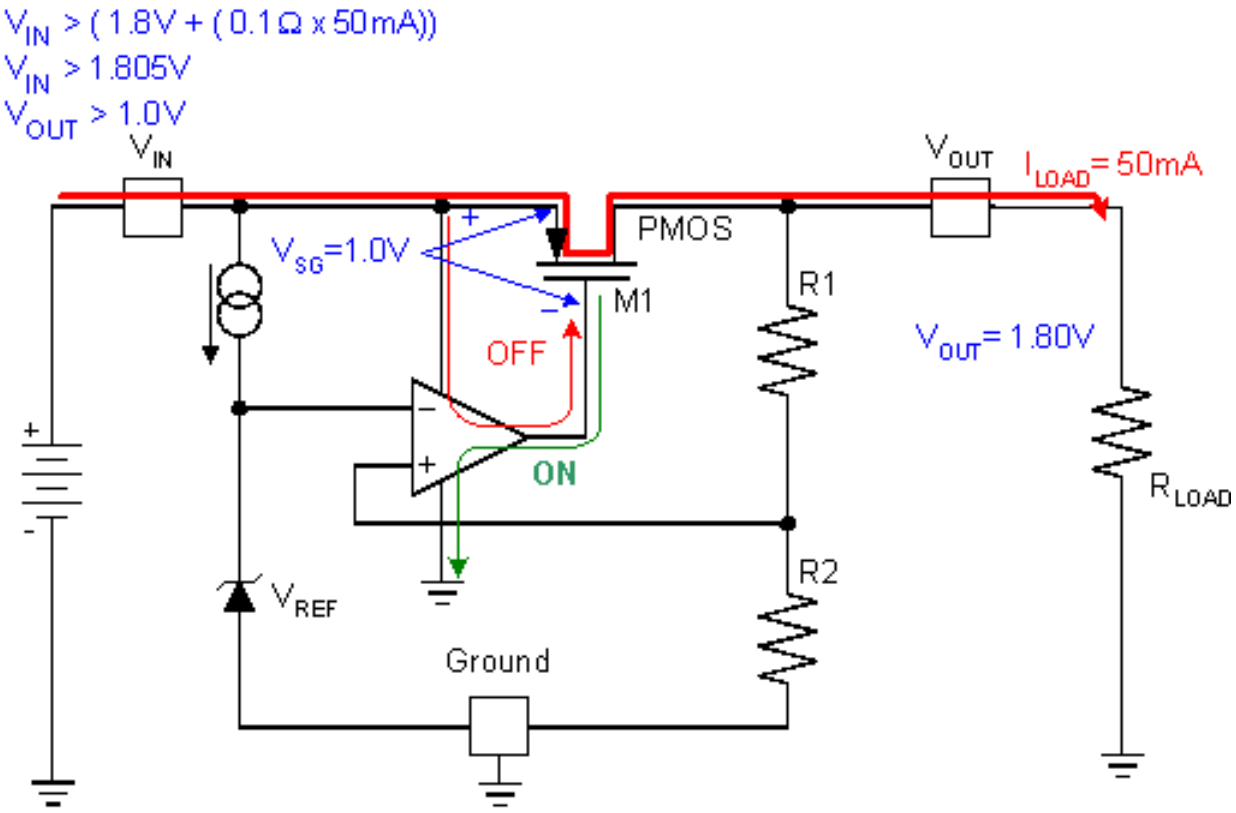
- Drop-out voltage set by by FET R_{DS-ON}
- Very low quiescent (ground pin) current
- Ground-pin current independent of load



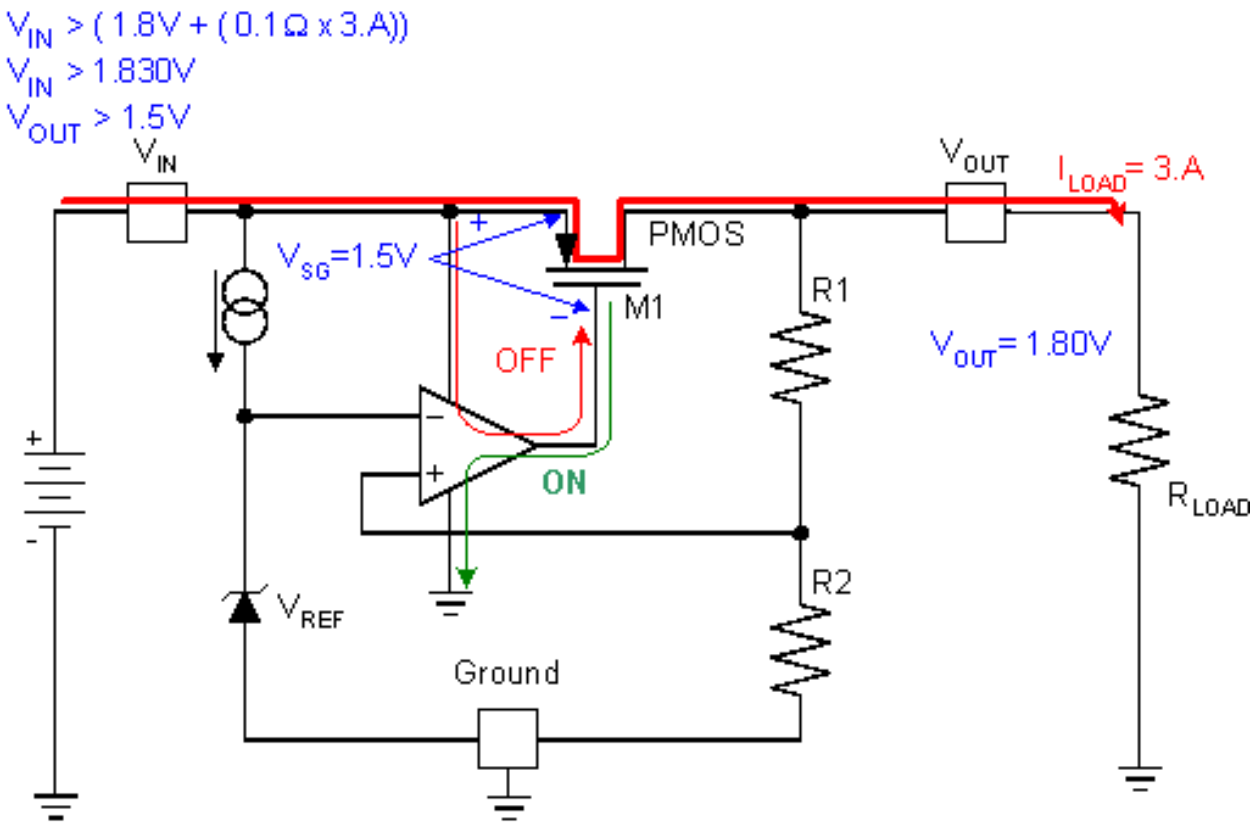
Driving PMOS LDO Pass Element



Gate Drive vs. Low Load Current



Gate Drive vs. High Load Current



Summary

- The PMOS LDO has the following Characteristics:
  - Requires that the input voltage be higher than the output voltage based on the load current and the On Resistance of the pass element:
    - $V_{IN} > R_{DS(on)} \times I_{OUT}$
  - Requires that the output voltage be higher than the V_{GS} requirement of the pass element
  - Requires careful selection of the output capacitor value and ESR ratings
  - To achieve similar $R_{DS(on)}$ performance a PMOS transistor will require a larger die area than NMOS transistors
  - The larger die area will affect pricing, and might affect performance

Thank you!