Low-Cost PCB Design

PCB design parameters

- Defining PCB design parameters begins with understanding:
  - End product features, uses, environment, and lifetime goals
  - PCB performance, manufacturing, and yield concerns
  - IPC-2221 “Generic Standard on Printed Board Design” which defines how to “establish design principles and recommendations” for producing PCB designs across three (3) end product classifications and three (3) levels of PCB produce-ability.
- Customers must select final PCB design parameters that meet:
  - End product form, fit, and functional needs while meeting reliability targets
  - PCB routing requirements and fabrication costs: Layer count, via type and size, trace width and space, number of interface signals, controlled impedance stack-up and routing, signal and power integrity
- Key PCB parameters to define for each PCB design:
  - PCB stack-up and routing plan
  - Controlled impedance plan
  - SoC breakout scheme
  - Cost target

PCB design parameters

- Recommendations for TI "New Fine-Pitch" (nFBGA) packages documented: Application Report "nFBGA Packaging" (SPRAA99B-March2008-Revised November 2015)
- Key SoC breakout scheme item:
  - BGA's Package Ball Via [a.k.a., Solder Mask Opening (SMO)] diameter vs PCB land diameter
  - Pkg SMO to PCB Land Dia Aspect Ratio (AR) recommendation = 1:1
    - Optimal solder joint reliability over thermal cycling
    - Best robustness under mechanical stresses

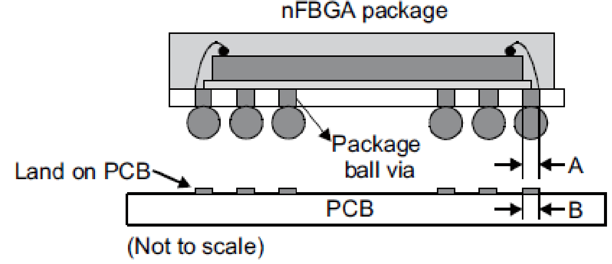


Figure 4. Package Via to Board Land Area Configuration

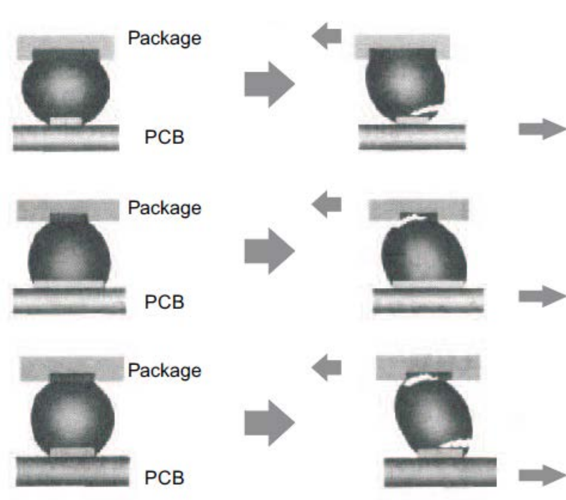
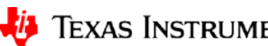


Figure 5. Effects of Via-to-Land Ratios



BGA vs VCA package types

- Package design seeks to maximize balls for supported features while minimizing total cost of an electronic system (die, package, PCB, and components).
- Removing balls from a full Ball Grid Array (BGA) pattern creates a Via Channel Array (VCA).
- VCA packages and footprints:
  - Enable routing channels to escape innermost BGA positions.
  - Reduce number of routing layers for 100% signal breakout.
  - Minimize package outline dimensions by using smaller ball pitch.
  - Allow larger breakout via land and drill diameters:
    - Lowers PCB manufacturing costs
    - Improves PCB reliability performance
  - Improve power integrity of power and ground plane layers:
    - Lower impedance vs frequency response that minimizes transient switching noise
    - Maintain current density/carrying capacity to innermost BGA positions

J6Entry Info PCB design

- PCB design breakout scheme:
  - Pkg SMO to PCB Land diameters, aspect ratio = 0.350 / 0.300, 1:0.86
    Same BLR performance as AR = 1:1 after 1600 temp cycles
  - IPC "Class 2"
    - 16/8 Breakout Via
      - Via Pad/Land diameter = 0.457mm / 16mil
      - Via Drill diameter = 0.203mm / 8mil
    - Allows "90° Partial Via Breakout"
      - Via drill edge can extend beyond via land edge by ~1.2mil
      - Only a few drill holes affected by max PCB manufacturing tolerance build-up
  - Center Location
    - Optimally places 16mil via land within SoC footprint
    - Improves PCB power and ground routing, which improves power integrity Z vs F performance by 15 - 20% @ 20MHz
    - Removes Via fill process step, which reduces PCB costs by 9-18%

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“16/8 Center Via Placement” breakout scheme

Advantages:

1) Reduces PCB cost 9-18% by center locating breakout via while meeting clearance rules to eliminate “Non-Conductive Via Fill” step.

2) Enables “Class2” PCBs with 90° partial via breakout.

Disadvantage:

1) A few automotive customers may not prefer 90° partial breakout.

0.65mm Pitch, 0.300mm Ball Pad, 16/8 Center Via Placement, 4mil Enlarged Solder Mask Ball Opening

650 um (25.6 mils)

919 um (36.19 mils)

106.5 um (4.19 mils)

406 um (16 mils)

29.7 um (1.17 mils)

26 um (1.02 mils)

203 um (8 mils)

Class2 PCBs allow 90° breakout

55.7 um (2.19 mils)

102 um (4 mils)

55.62 um (2.19 mils)

50.8 um (2 mils)

402 um (15.8 mils)

300 um (11.8 mils)

919 – 300 = 619
619 – 406 = 213
213 / 2 = 106.5 (4.19mil)
106.5 – 50.8 = 55.7 (2.19mil)
(4.19 – 2 ~ 2.19mil)

Solder Mask

Via Land/Ring

Via Drill/Hole

Line/Trace

Non-Solder Mask Defined (NSMD)

BGA Ball Land

Solder Mask Ball Opening Diameter

Recmd Solder Mask Diameter = Ball Pad Diameter + 0.1um (4mil)

J6Entry Info: PCB design rules, IPC Class 2

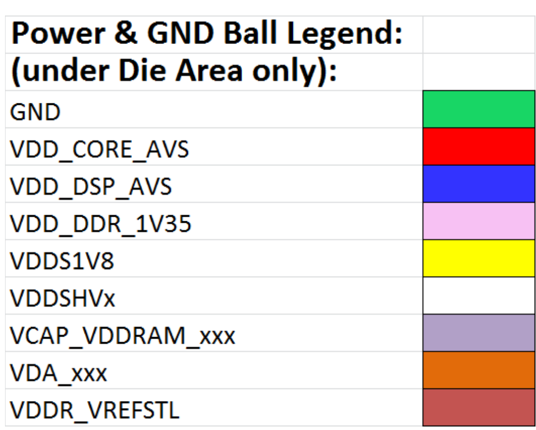
Items	Values [mm] (mil = 1/1000inch)
BGA Ball Pitch	0.650 (25.6)
BGA SMO to PCB Land Dia, Aspect Ratio	0.350/0.300 (11.8), 1:0.86
BGA Pad to Solder Mask Clearance, min	0.0508 (2.0)
Trace/Line Width, min	0.102 (4.0)
Space, Conductor to Conductor (different net),min (Conductor = any Cu surface, i.e. Trace, Pad, Via, Plane…)	0.102 (4.0)
Space, Conductor to Via Drill Edge, min	0.229 (9.0)
Via, Plated Through-Hole (PTH) Drill dia, min	0.203 (8.0)
Via, PTH Land dia, min	0.406 (16.0)
Via, PTH Anti-Pad (Plane Clearance) dia, min	0.965 (38.0)
Via, PTH Annular Ring Width, typ	0.102 (4.0)
Via, PTH Hole – Hole Pitch, min	0.559 (22.0)
PCB Thickness, Aspect Ratio = Thickness/Via dia (Volume PCB production desires max AR = 8:1)	1.58 (62.0), 7.75

J6Entry VCA Pattern (17x17, 0.65mm, 538 Ball, VCA)

Bottom-View

Ball Map Summary

Pkg Outline = 17x17mm
BGA Pitch = 0.65mm
BGA Grid (25x25) = 625
Ball Voids for VCA = 87
Total Balls = 538



Power & GND Ball Legend: (under Die Area only):	
GND	
VDD_CORE_AVS	
VDD_DSP_AVS	
VDD_DDR_1V35	
VDDS1V8	
VDDSHVx	
VCAP_VDDRAM_xxx	
VDA_xxx	
VDDR_VREFSTL	

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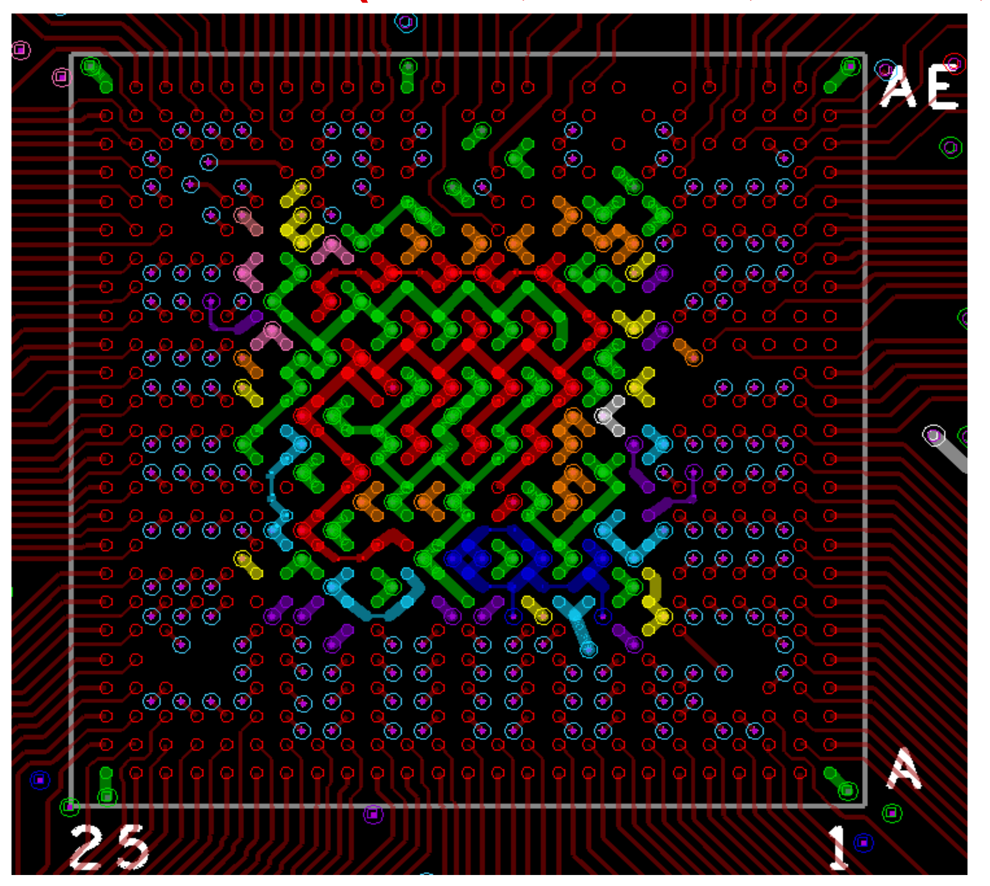
J6Entry Info RevB: Breakout (17x17, 0.65mm, 538 Ball, VCA)

PCB Layer = Top

BGA Ball Summary

Signal Balls = 325
Power Balls = 122
Gnd Balls = 88
No Connects = 3
Total Balls 538

Power & GND Ball/Net Legend:	
GND	
VDD_CORE_AVS	
VDD_DSP_AVS	
VDD_DDR_1V35	
VDDR_VREFSTL	
VDDS_1V8	
VIO_3V3	
VDA_xxx	
VDA_SDIO_DV	
VCAP_VDDRAM_xxx	
Signal Breakout Vias - 16/8 (Land/Drill dias [mil])	
BGA Land Pad	



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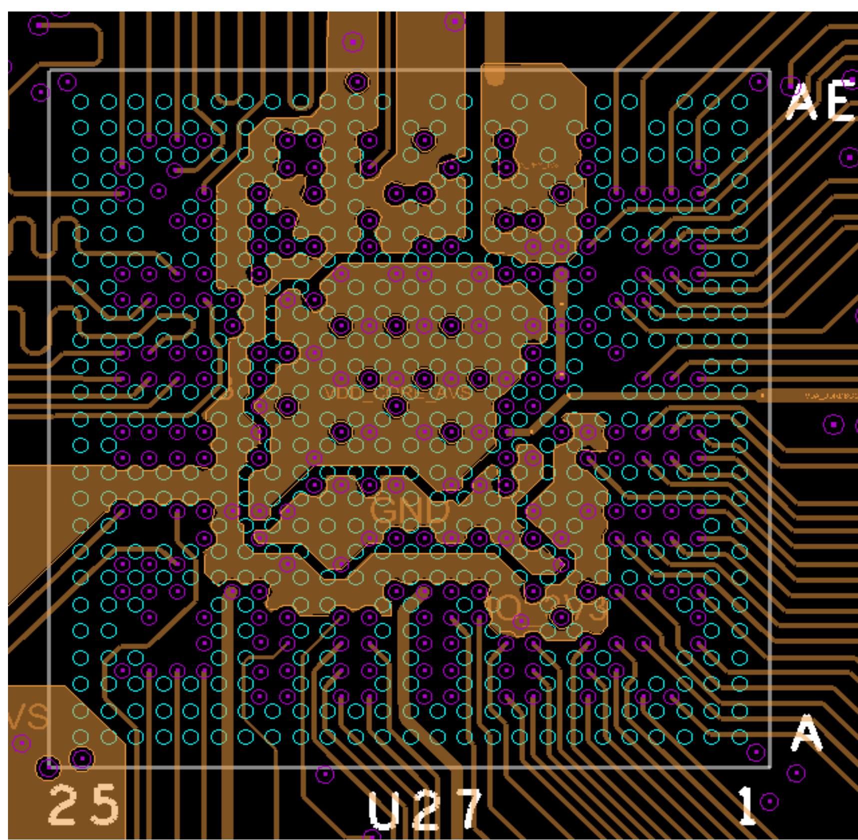
J6Entry VCA: Deeper breakout in less layers

PCB Layer 3
Signal #2



- VCA concentrates breakout vias to be into specific areas allowing “routing channels”.
- Routing channels provide easy access to signal balls located in deeper into the SoC footprint.
- End result is less PCB signal layers needed to breakout all signal balls vs a full BGA footprint.

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“Min Via Land Size” Visual Models

Annular Ring Requirements For IPC-6012 Class 2 & 3

IPC 6012B Class II

IPC 6012B Class III

Minimum annular Ring 1.969 mil

Larger pad than Class II to allow For registration

90 degree Breakout

Minimum annular Ring 0.984 mil

Worst case registration allowed by IPC Class II

Worst case registration allowed by IPC Class III

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TTM Technologies

PCB technology vs cost impacts

Key Items	Standard PCB Tech [mm] (mil)	Advanced PCB Tech [mm] (mil)	Approximate Cost Increase #
Min Trace Width & Conductor Space (Cu weight dependent)	0.102 (4.0)	0.0762 (3.0) < 3mil	1.2x 1.5x
Max Aspect Ratio (PCB thickness / Drill dia) dependent upon Drill size, for 8mil	8:1	> 8:1	1.2x
Min Via, Mechanical/Through-Hole Drill Dia	0.203 (8.0) for AR 8:1	0.150 (6.0) plus AR 10:1	1.2x (drill cost) 1.2x (AR cost)
Min, Blind Via Mechanical (may add Lam Cycle) Min, Blind Via Laser Drilled μ-Vias	NA (5mil offset, single Lam Cycle)	0.150 (6.0) 0.102 (4.0), Cu filled μvia	1.5x (per Lam Cycle) 1.0 – 1.4x*
Sequential Lamination	NA	Additional Lamination Cycles	1.5x (per Lam Cycle)
Via Fill, Non-Conductive (could be used with Via-In-Pad)	NA	10mil (preferred min drill)	1.2 – 1.4x*
Via Fill, Conductive	NA	Not Recommended	
Embedded Capacitance	2mil core	BC2000 ™, HK-04, FaradFlex ™	1.3 – 1.4x*
Embedded Resistance	NA	Ohmega ply, Ticer	2 – 3x*

NOTE: * Dependent upon PCB size, layer count & count per panel

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