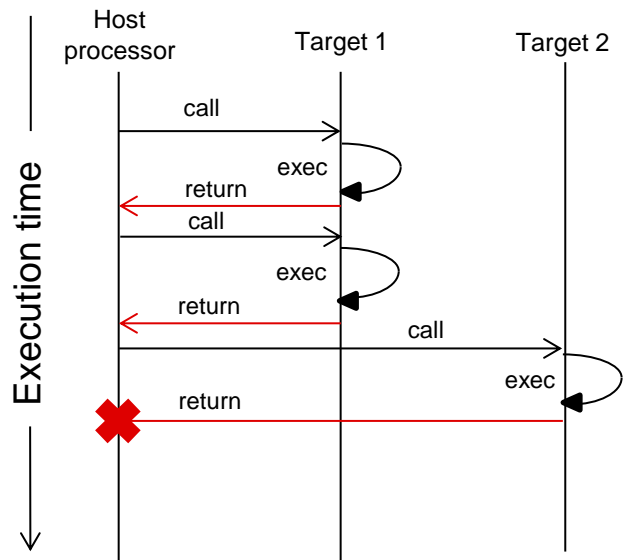


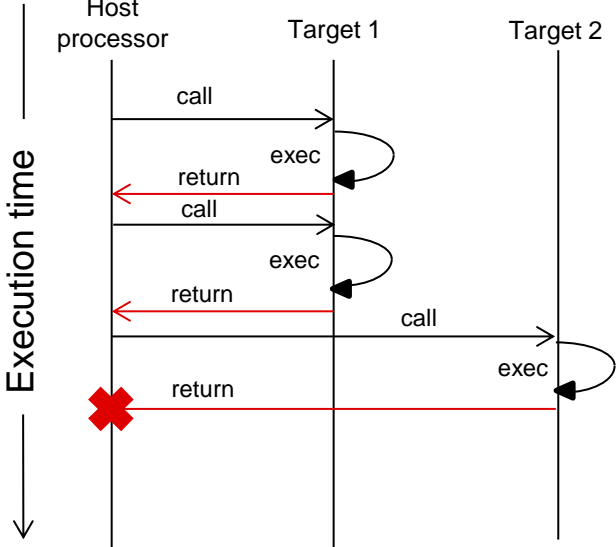
TI OpenVX™ (TIOVX): Framework optimizations

IPC aggregation

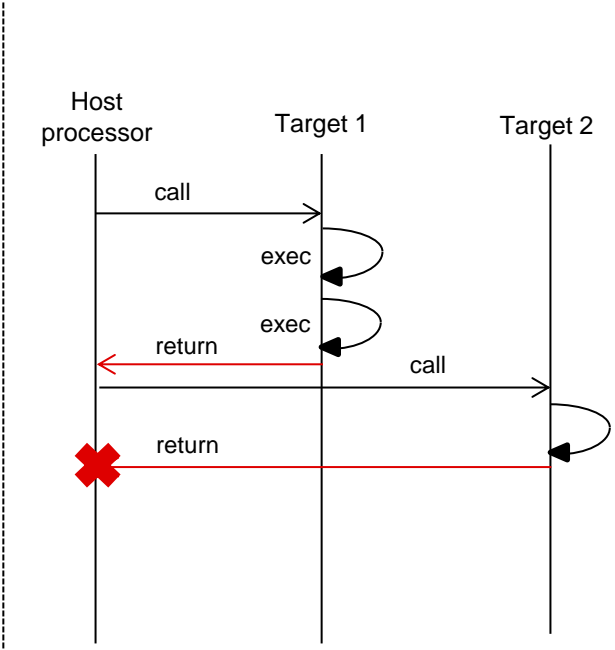


No aggregation
Highest overhead

IPC aggregation

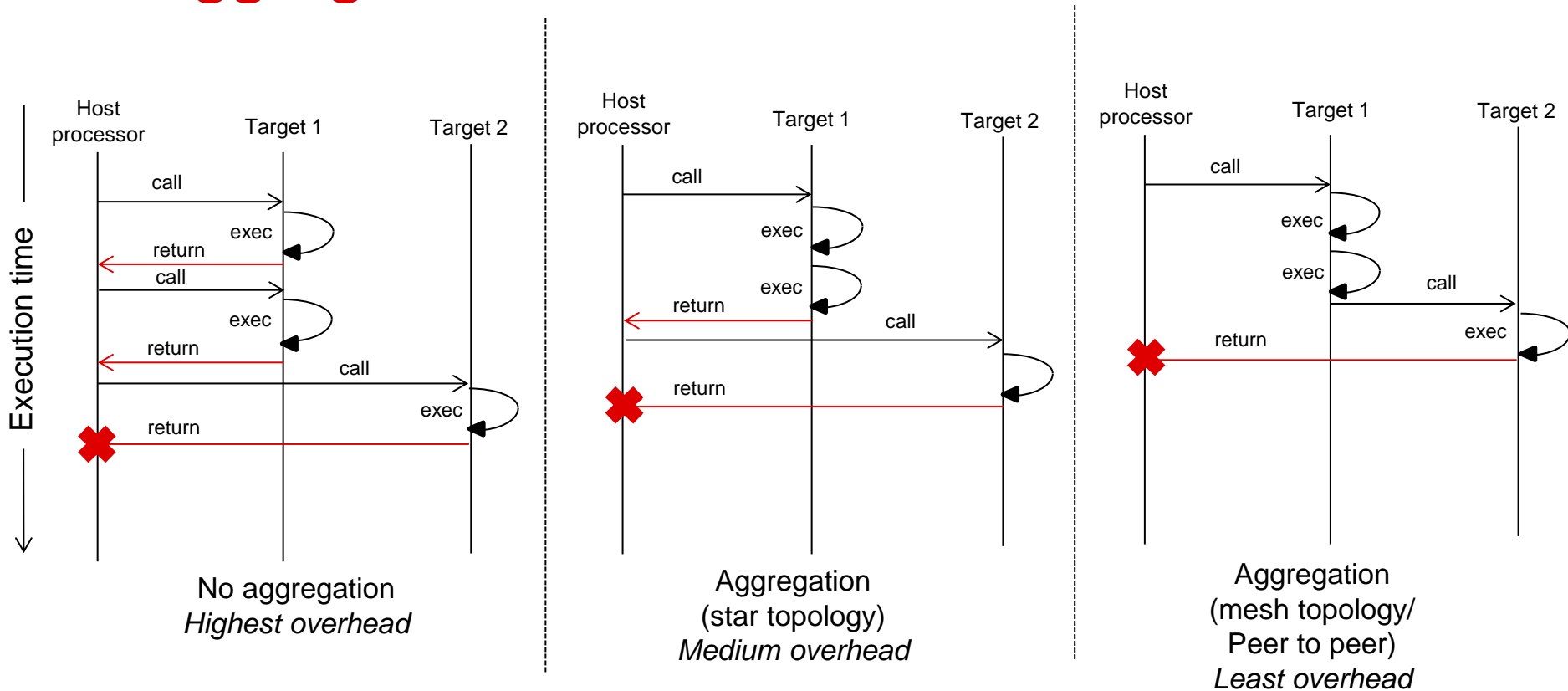


No aggregation
Highest overhead

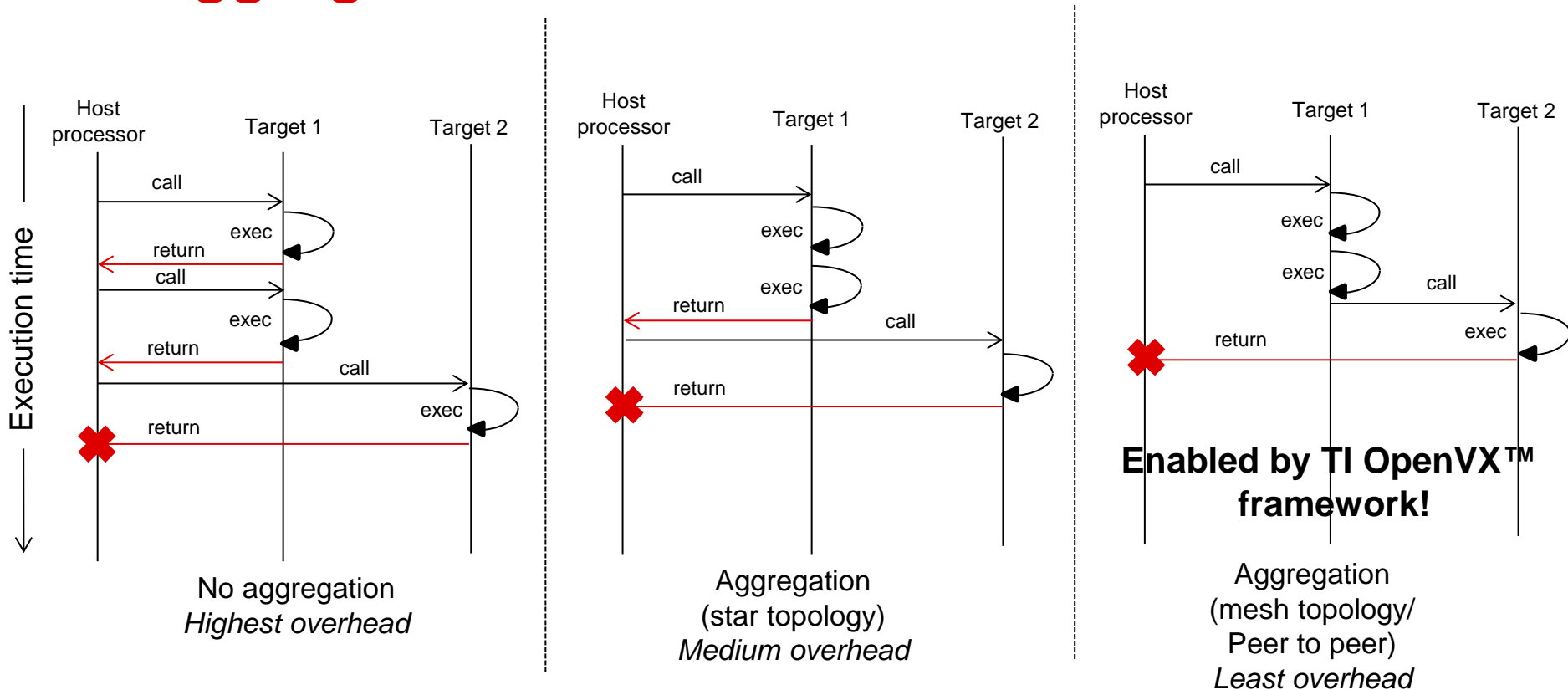


Aggregation
(star topology)
Medium overhead

IPC aggregation

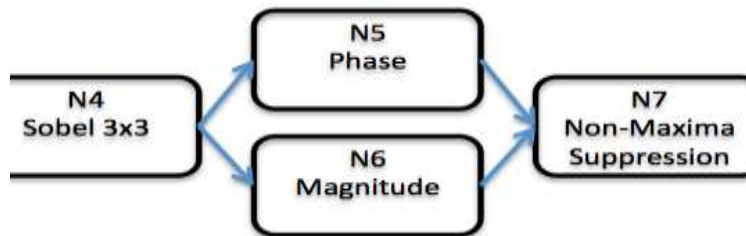


IPC aggregation



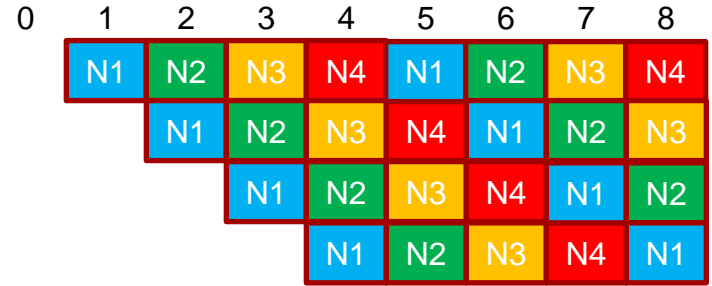
Parallelism

- Enabled by graph model
- Independent nodes can potentially be executed in parallel (using different execution units/cores)



Graph Pipelining

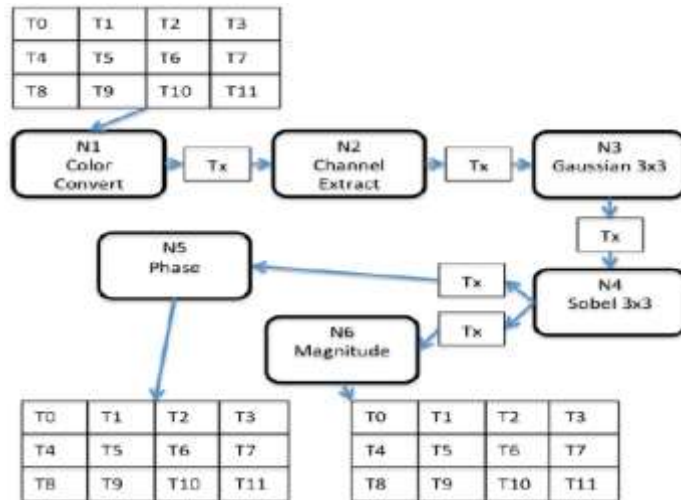
- Pipelining multiple invocations of a graph across targets:
 - As images are fed to the system, the graph execution of these input images can be staged across targets in a pipeline fashion.
 - Enables full performance entitlement on SoC's with multiple cores



Example of 4 nodes pipelined across 4 target cores

Additional optimizations

- Block/tile processing
 - When output depends only on subset of input (not entire input), the data to be processed can be broken into tiles, and fed into the graph.
 - Each node processes 1 tile of data at a time and the graph executes N times for 1 image (N is number of tiles in the image)
 - Removes intermediate round-trips to memory
 - Requires a custom DMA framework to be implemented
- Abstraction of cache operations/address translation
 - TI provides internal memory API's for optimized cache maintenance and address translation



For more information

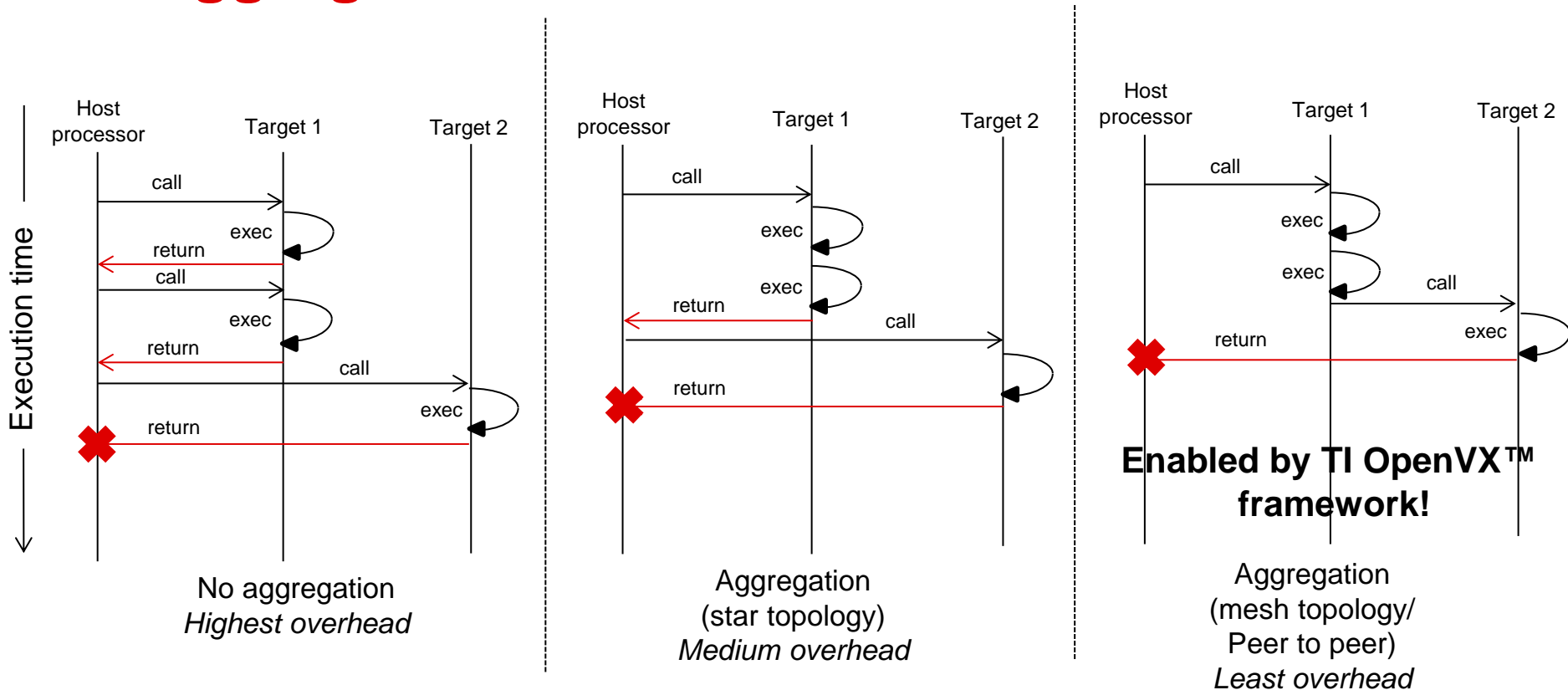
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<http://www.ti.com/tool/PROCESSOR-SDK-JACINTO-DRA8X-TDA4X>
- Processor SDK Linux Automotive (PSDKLA) user guide:
[#{PSDKLA_INSTALL_PATH}/docs/linux/index.html](http://www.ti.com/tool/PROCESSOR-SDK-LINUX-AUTOMOTIVE-PSDKLA-USER-GUIDE)
- Processor SDK RTOS Automotive (PSDKRA) user guide:
[#{PSDKRA_INSTALL_PATH}/index.html](http://www.ti.com/tool/PROCESSOR-SDK-RTOS-AUTOMOTIVE-PSDKRA-USER-GUIDE)
- For additional questions, refer to the E2E community forums:
<https://e2e.ti.com/support/processors/f/791>
- “Addressing System-Level Optimization with OpenVX Graphs”
<https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6910050>



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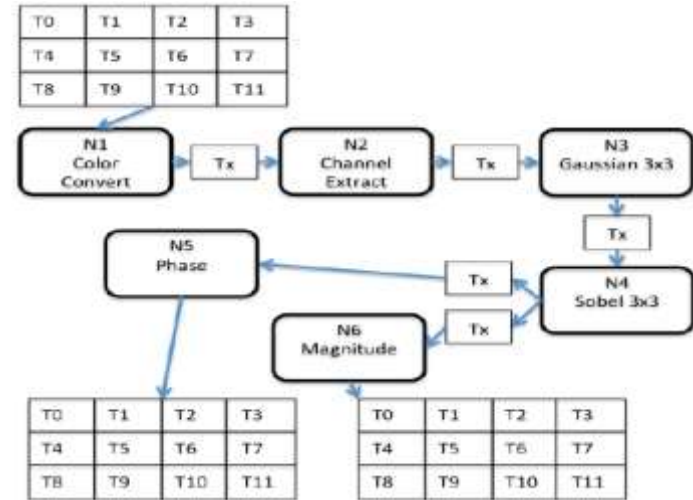
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IPC aggregation



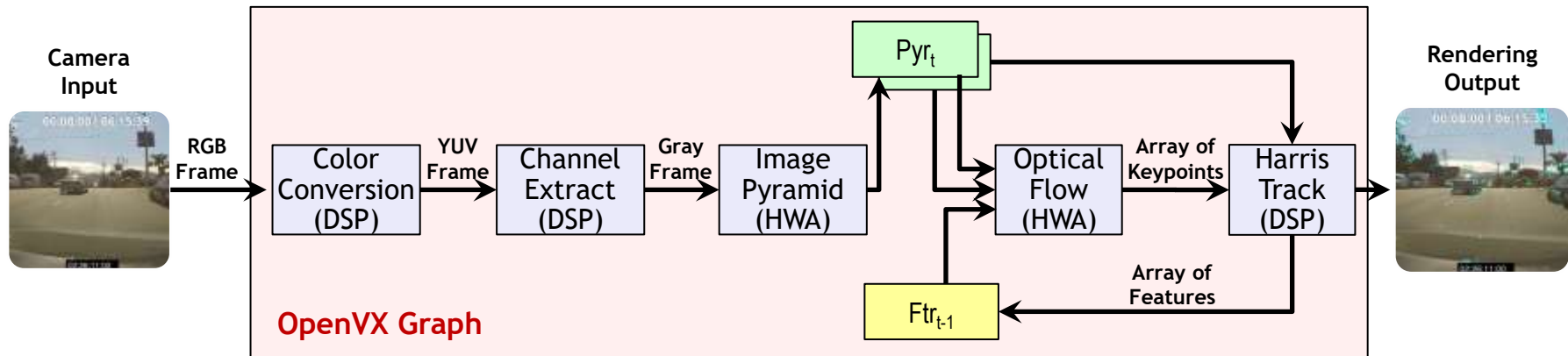
Block/tile processing

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Abstraction of cache operations/address translation

- TI provides internal memory API's for optimized cache maintenance and address translation



Graph model enables ... kernel fusion

- Aggregate function replacement :
 - Identifying a sub-set of nodes which can be replaced by a single equivalent node:

