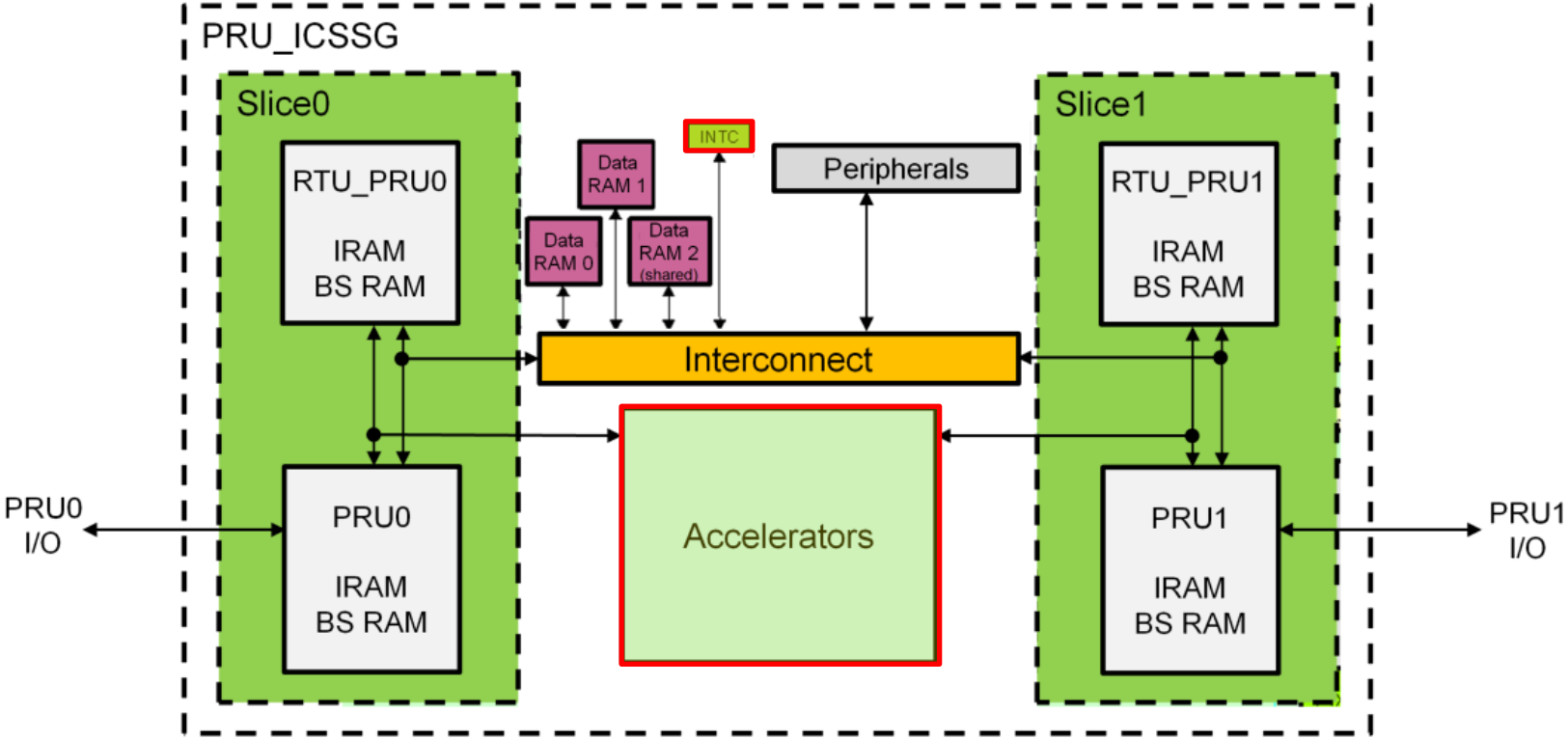
PRU_ICSSG

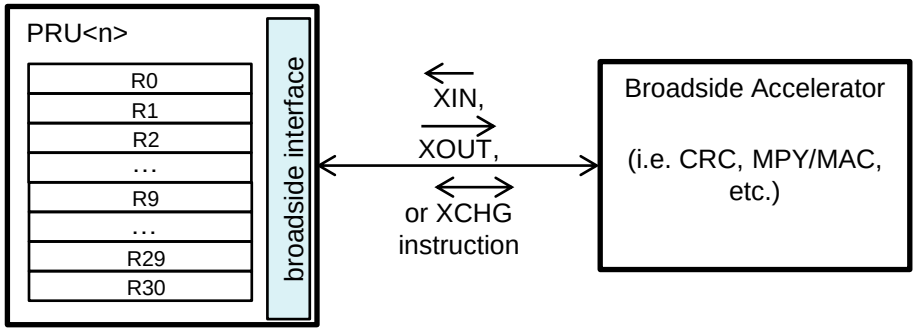
Accelerators

PRU_ICSSG Hardware Overview



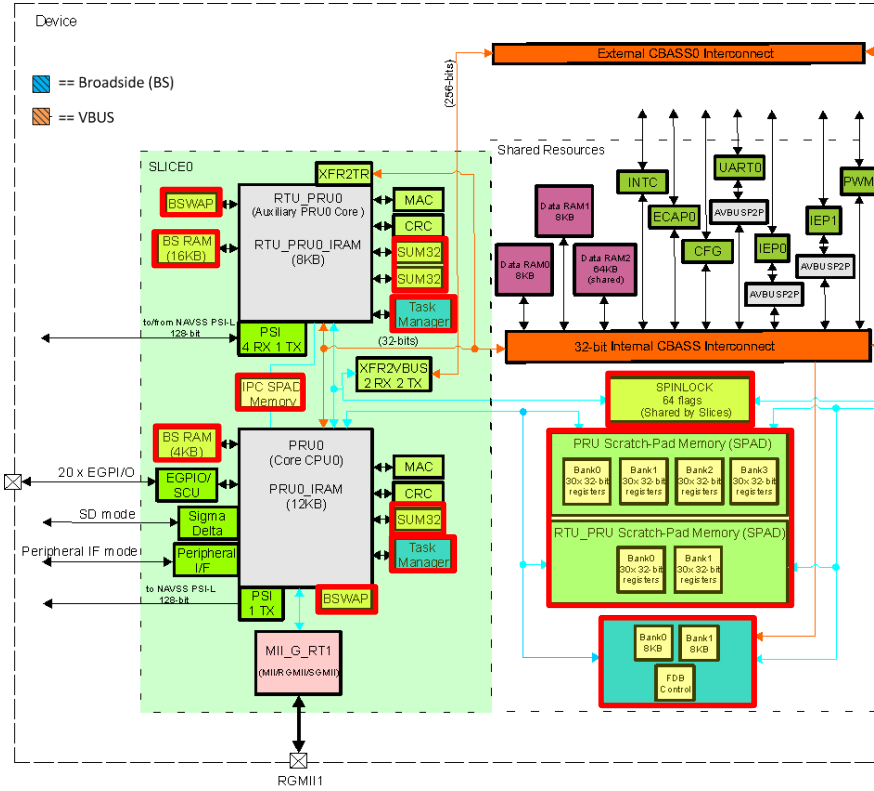
Broadside Interface

- Each PRU/RTU_PRU has a wide register load/store/exchange interface (referred to as broadside) that allows one cycle access to accelerators
- A special set of instructions (XIN/XOUT/XCHG) are used for broadside communication
  - XCHG is new to PRU_ICSSG
  - All accelerators attached to broadside interface have a “Broadside ID”
- Up to 31 registers (R0-R30, or 124 bytes) can be transferred in a single instruction



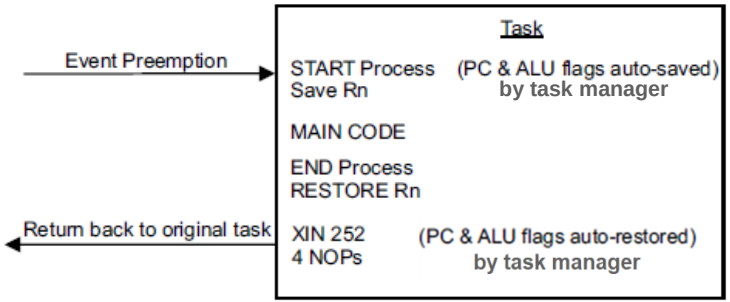
Data Processing Accelerators

Accelerators	PRU_ICSSG	Original Purpose
Task Manager	New	
Scratch Pad Memory	Same	
IPC Scratch Pad Memory	New	
Filter Data Base (FDB)	New	Ethernet
Broadside (BS) RAM	New	
SUM32	New	Ethernet
Byte Swap (BSWAP)	New	Ethernet
Spinlock	New	
CRC16/32	Upgraded	
MPY/MAC	Upgraded	



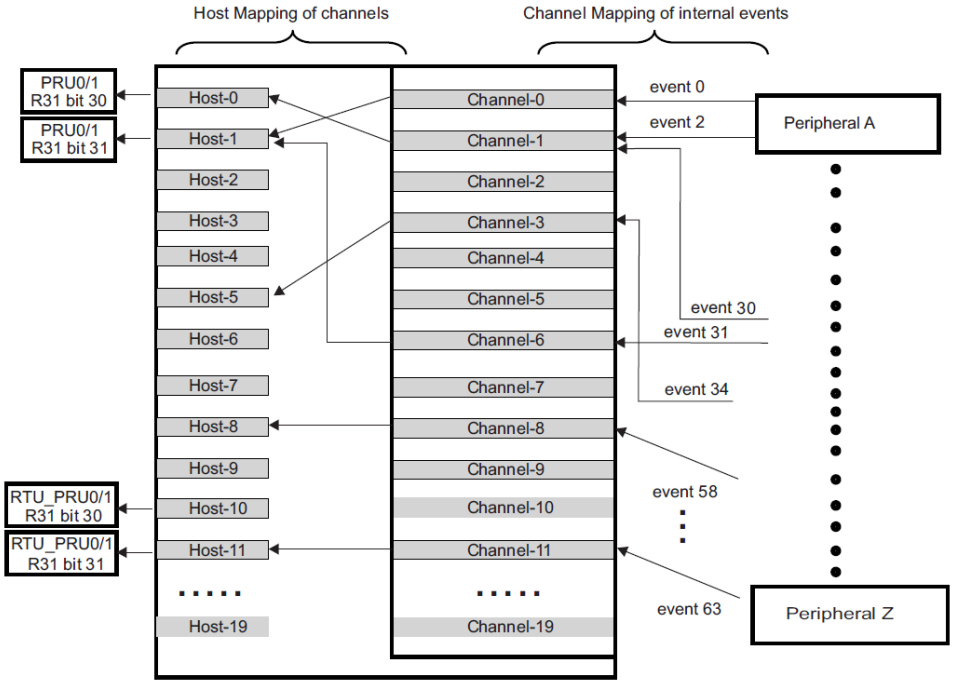
Task Manager

- Each PRU_ICSSG core has its own task manager block
- The task manager can be used as a preemptive, event-based context switcher
- There are 3 priorities (low / background, mid, high) and 5 subroutines within the mid and high priorities
- A list of events is provided that can be mapped to any subroutine in any priority
  - Once the event occurs (if it is the highest priority), then the Program Counter (PC) of the respective core will be jumped to the code for that subroutine



INTC Upgrades

Feature	PRU_ICSSG	PRU-ICSS
System events	**160 (total)** - 96 external events - 64 internal events	**64 (total)** - 32 external events - 32 internal events
Channels	**20 (total)**	**10 (total)**
Host Interrupts	**20 (total)** - 2 for PRUs - 2 for RTU_PRUs - 8 for device level interrupt controller - 8 for task manager	**10 (total)** - 2 for PRUs - 8 for device level interrupt controller



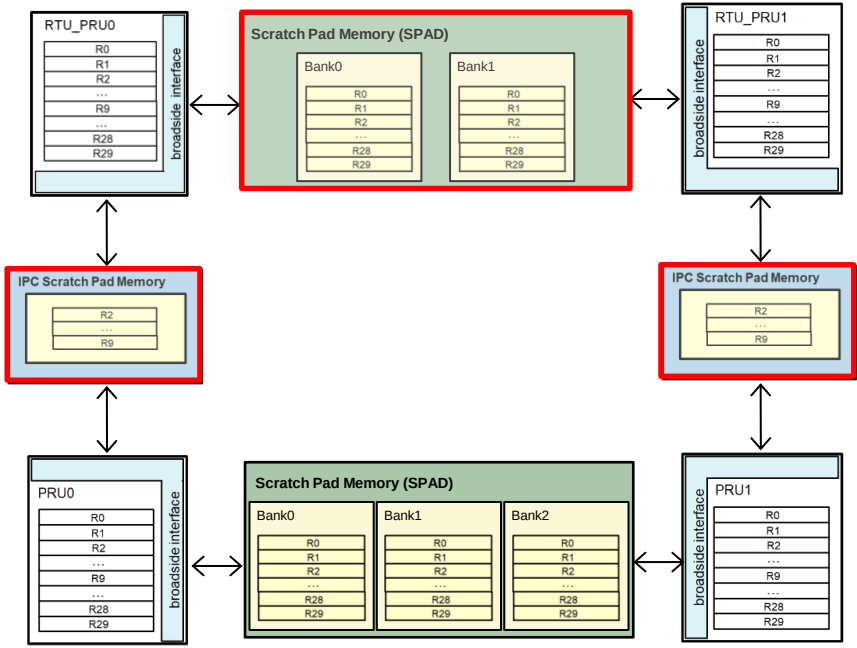
Note: The INTC is <u>not</u> connected to the broadside interface.

Scratch Pad Memory (SPAD)

New to PRU_ICSSG

- Scratch Pad Memories (SPAD)
  - Used to move data extremely quickly between similar cores (i.e. RTU0<->RTU1, PRU0 <->PRU1, TX_PRU0<->TX_PRU1)
  - Each bank is 30 x32bit registers
    - Cores can transfer its full internal register set into a scratchpad bank in a single cycle
  - Number of banks varies between devices

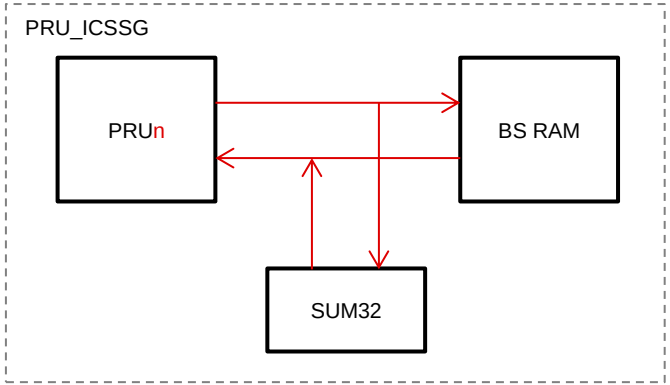
- IPC Scratchpad
  - Allows up to 32 bytes to be transferred between a PRU and an RTU very quickly
  - Takes a single cycle for a PRU/RTU to transfer up to 32 bytes into or out of the IPC scratchpad



Broadside RAM & SUM32

Broadside RAM (BS RAM)

- Fast access to memory
- Each type of PRU core has a dedicated BS RAM
- Supports 32Byte writes

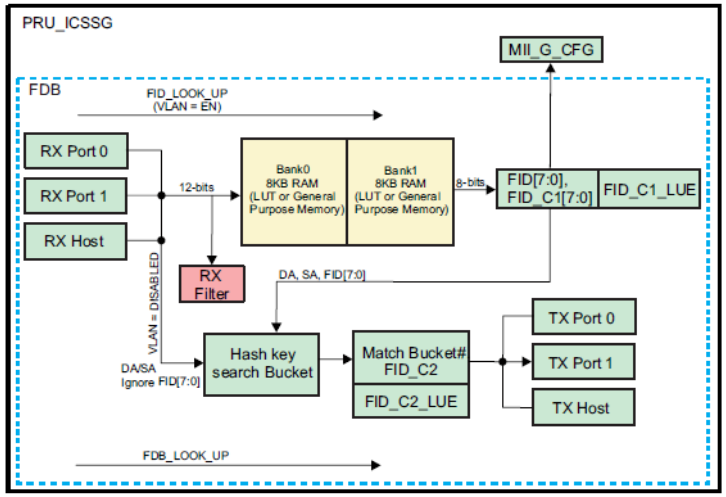


SUM32

- 32 bit sum accelerator for UDP checksum
- Snoops data writes to BS RAM

Filter Data Base (FDB)

- Accelerates switch function learning, primarily for Ethernet
  - Performs hardware lookup of VLAN_ID / HSR and provides port mapping
- Shared resource in PRU_ICSSG
  - Only PRU cores can access the FDB RAMs, spinlock required as only one core can own
  - RTU_PRU cores can only get the result of FDB lookup via its broadside access
- Supported modes:
  1. FDB Lookup Table (LUT)
  2. General Purpose, 16Byte compare
  3. Generic Broadside RAM (8KB/16KB)

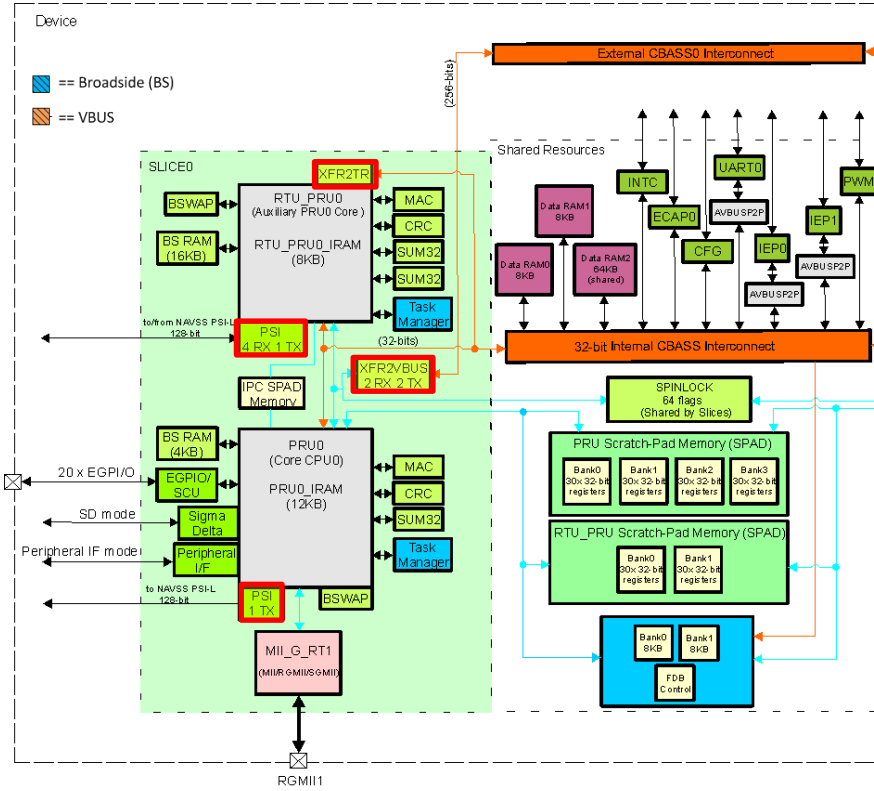


Other Data Processing Accelerators

- Byte Swap
  - Allows fast data reorder (Little/Big Endian conversion)
  - Developed to help accelerate Ethernet operations
- Spinlock
  - Spinlock to lock resources for lower latency in ICSSG using broadside connection
  - 64 ownership flags (shared by SLICE0 and SLICE1 within PRU_ICSSG)
- Multiplier with Accumulation (MPY/MAC)
  - Fixed carry flag limitation. Otherwise, same as previous PRU-ICSS devices.
- CRC16/32
  - Added new polynomial, CRC16 – CCITT ($x^{16}+x^{12}+x^5+1$)
  - Added FIFO in front to allow 32-byte pushes

Data Movement Accelerators

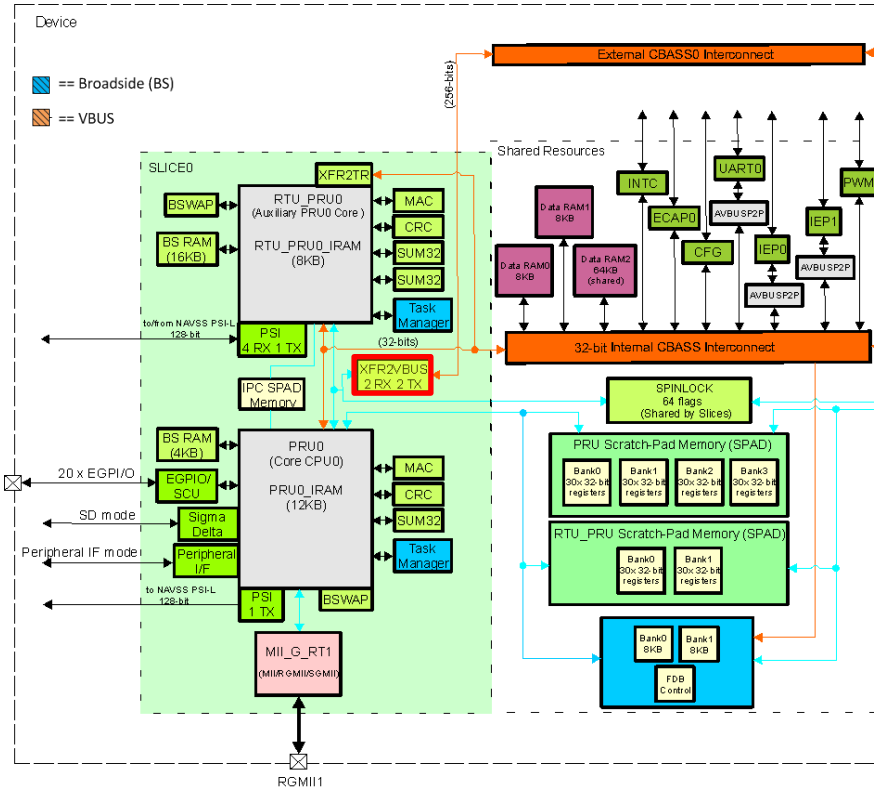
Accelerators	PRU_ICSSG
XFR2VBUS	New
PSI TX & RX	New
XFR2TR	New



XFR2VBUS Channels

Real-Time DMA

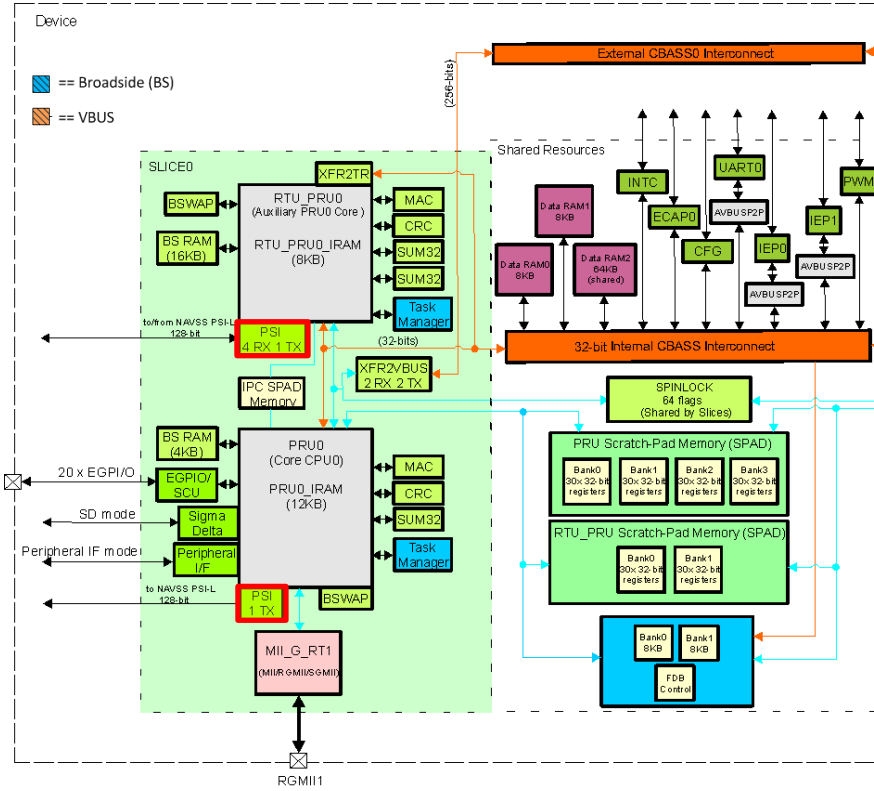
- Each slice has XFR2VBUS block with TX and RX paths
- Uses broadside interfaces to transfer data to/from device level MMRs
  - Up to 64 bytes of data transferred to PRU/RTU core registers in a single cycle
  - Low latency CBASS path to MSMC SRAM (32-byte bus)
- Reads are non-blocking
  - PRU/RTU can continue to process other data until new data has arrived at the XFR2VBUS block



PSI (Packet Streaming Interface) TX & RX

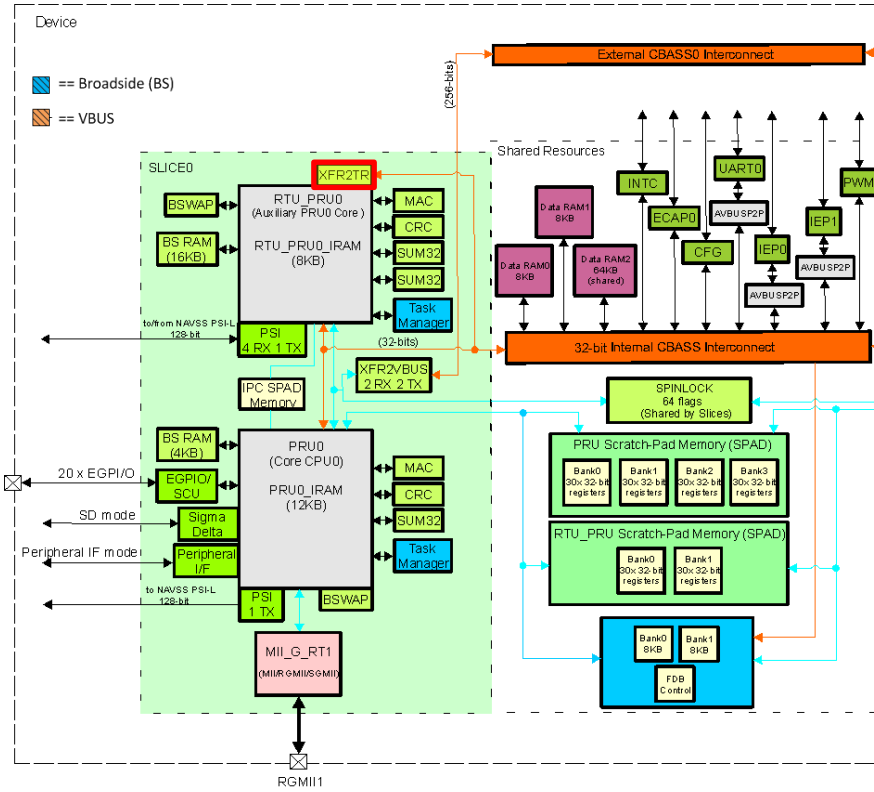
Non Real-Time DMA

- Each PRU/RTU_PRU core has paths to the packet streaming interface
  - The number of TX & RX paths varies between devices
- PSI is a packet based transport system to offload the data movement process to/from SoC peripherals
- The data path is configured once and then can be used repeatedly with no further overhead



XFR2TR Ring Accelerator

- Only available on RTU_PRU cores
- Accelerates internal memory copy of worklist from Transfer Requests (TR)
- Stored in Shared RAM



For more information

- PRU Training Series: https://training.ti.com/pru-training-series
- PRU-ICSS Feature Comparison: http://www.ti.com/lit/sprac90
- PRU_ICSSG Getting Starting Guide on Linux: http://www.ti.com/lit/sprace9
- PRU Read Latencies: http://www.ti.com/lit/sprace8
- PRU-ICSS / PRU_ICSSG Migration Guide http://www.ti.com/lit/spracj
- For questions about this training, refer to the E2E Community Forums at http://e2e.ti.com