

PCIe board layout recommendations

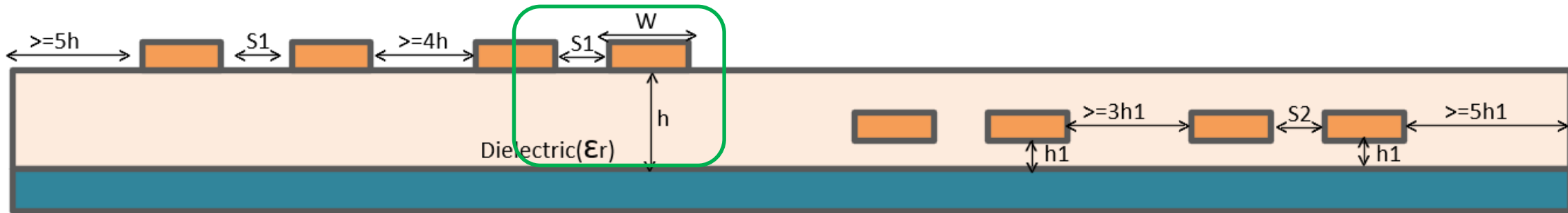
TI Precision Labs – PCIe

Prepared by Nasser Mohammadi

Presented by Nicholas Malone

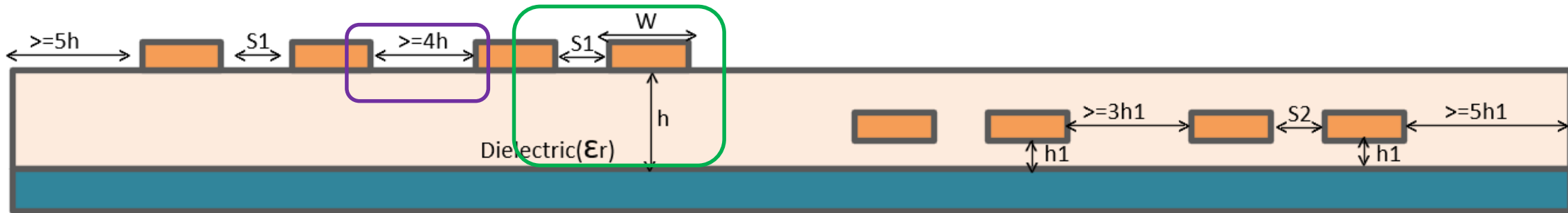
Differential board trace width and spacing

- Design trace width, height, and spacing to meet $85 \pm 20\%$ Ohm for PCIe connector
 - $100 \pm 20\%$ Ohm for chip to chip



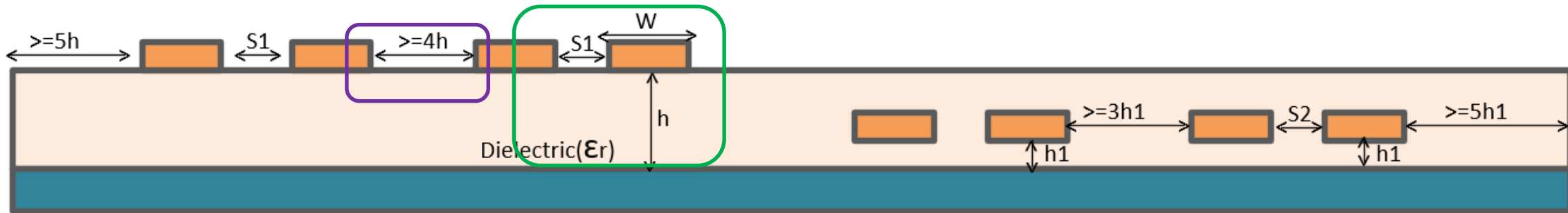
Differential board trace width and spacing

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- Distance between adjacent traces should be at least 4 times dielectric height(h)
 - Stripline traces should be 3 times



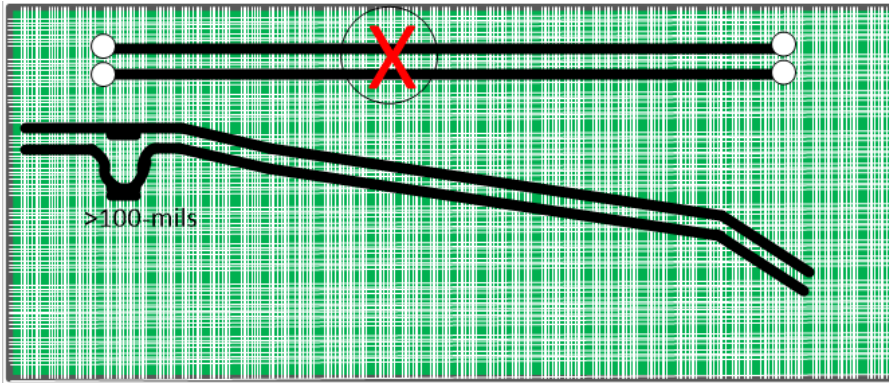
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 - $100 \pm 20\%$ Ohm for chip to chip
- Distance between adjacent traces should be at least 4 times dielectric height(h)
 - Stripline traces should be 3 times
- Distance between PCIe pair and non-PCle signals should be at least 4 times height
 - If non-PCle signal has higher slew rate or level, then this distance should be 6 times height



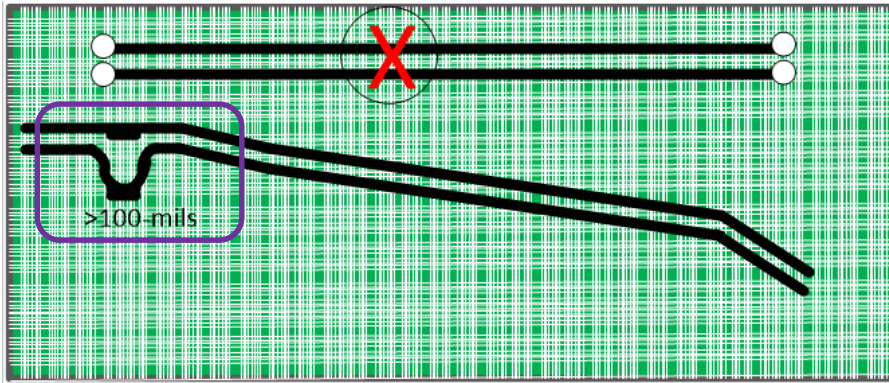
Trace length matching and trace length

- Avoid running long traces in parallel with grain of the fiber.



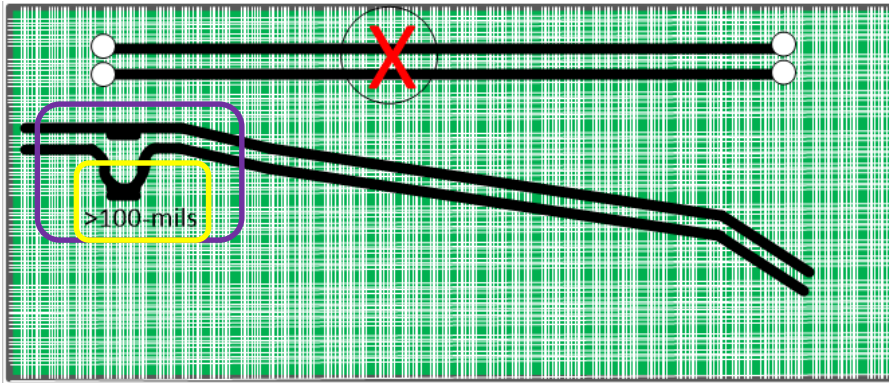
Trace length matching and trace length

- Avoid running long traces in parallel with grain of the fiber.
- Intra-pair trace should be matched to within 5-mils.
 - Trace mis-match compensation should be done at the point of mis-match.



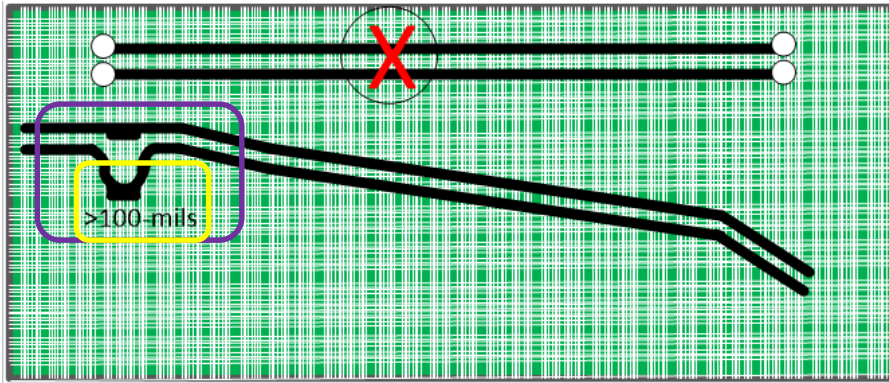
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- Trace width of any un-coupled section of a differential trace greater than 100-mils, should be increased to maintain target impedance



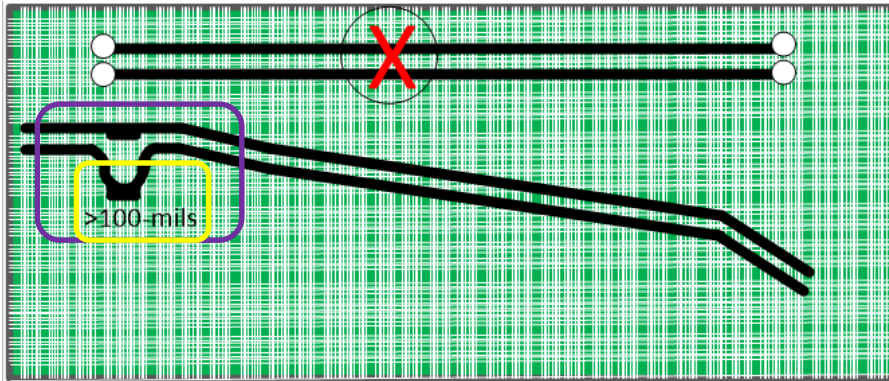
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- Trace length to a connector is limited to 12 inches – this includes breakout area
 - Trace length from the edge-finger to add-in card chip set is limited to 4 inches
 - Board stack up and material can impact this length



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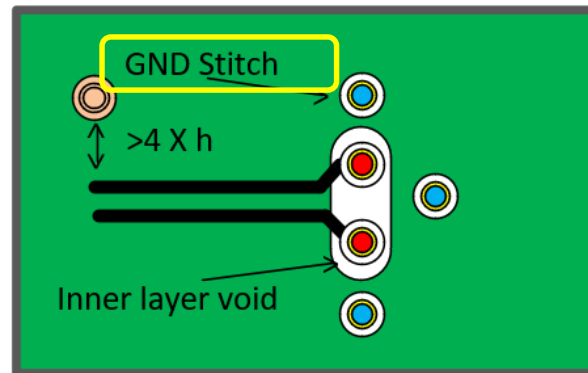


Via placement and guidelines

- Avoid vias as much as possible
 - Maximum of 6 via pairs are allowed on entire transmission line
 - In terms of loss, each via pair contributes to the loss budget per data rate 1dB at Gen4 and 0.5dB at Gen3
 - Via pad size should be 25 mils or less and a finished hole size of 14 mils or less

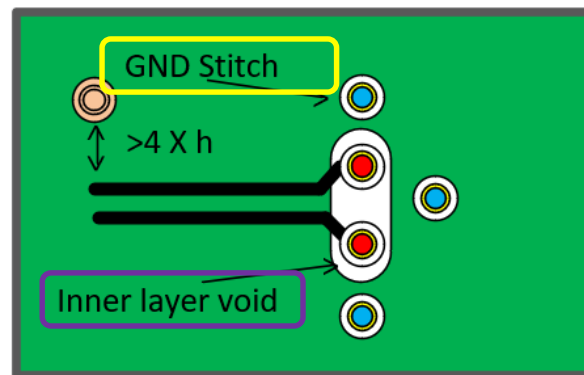
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 - Via pad size should be 25 mils or less and a finished hole size of 14 mils or less
- Provide GND stitch to improve signal impedance transition
 - Location of via should be simulated. Else via should be placed at $>$ via center to center spacing and $<$ 100mils away from the via
 - Signal vias should have pads removed on unused internal layer
 - GND Stitch should be between the signal two reference planes



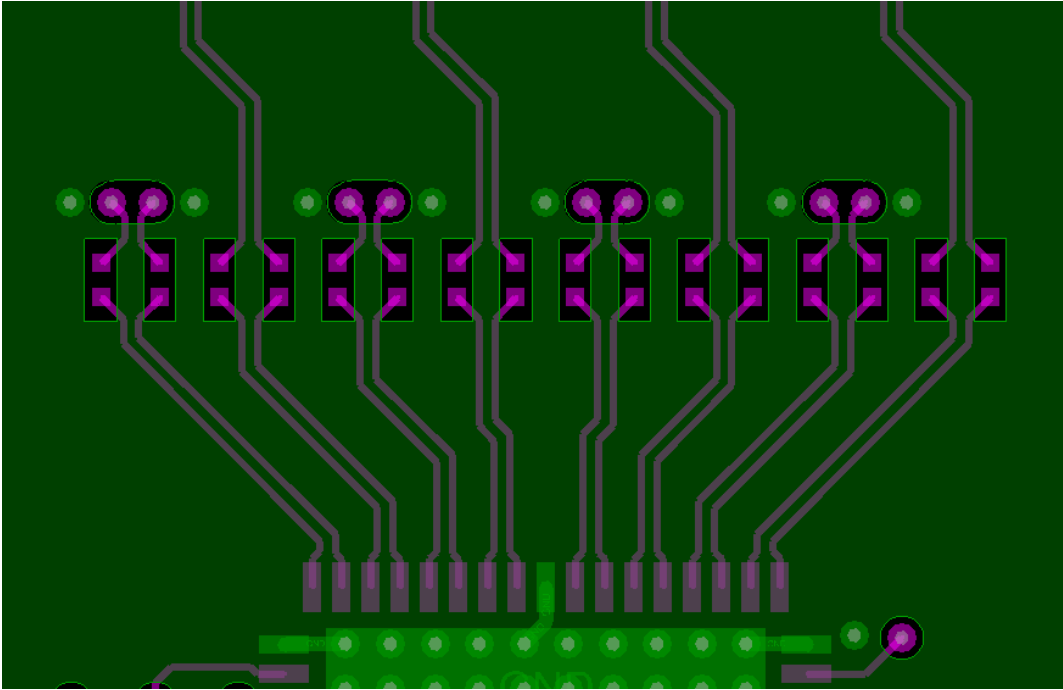
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- Provide inner layer void – no GND or VCC – to reduce parasitic



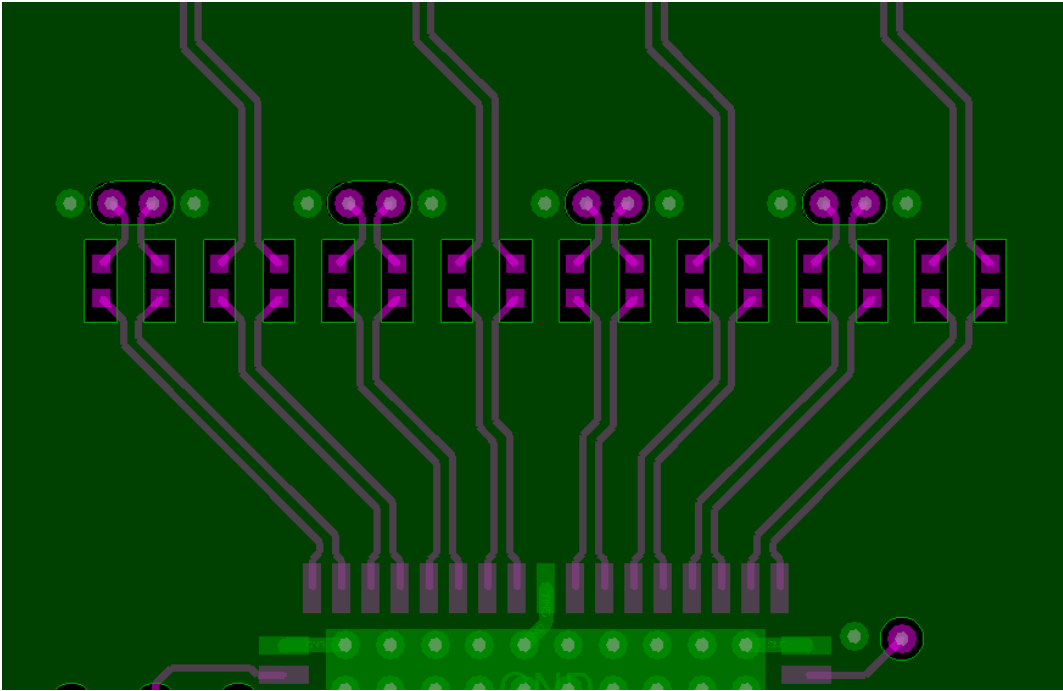
AC Coupling Cap void

- Void under AC coupling Caps pad:
 - Through as many layers as possible



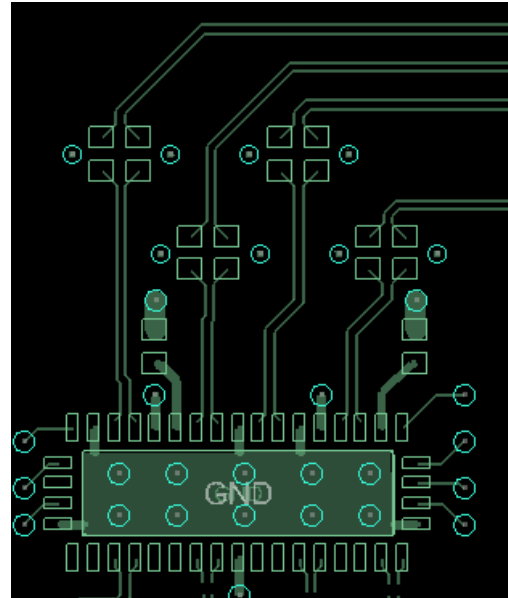
AC Coupling Cap void

- Void under AC coupling Caps pad:
 - Through as many layers as possible
- Via to differential trace should have at least 3 times differential trace spacing



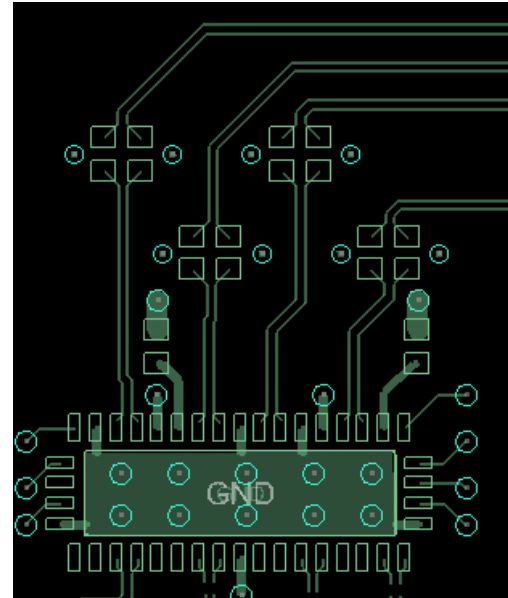
AC coupling capacitors placement

- Add-In Cards: Within 400mils of the CEM connectors



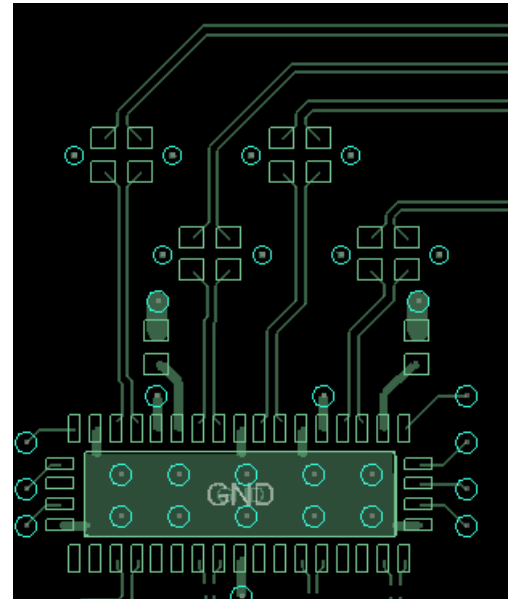
AC coupling capacitors placement

- Add-In Cards: Within 400mils of the CEM connectors
- Add-In Cards: Within 250mils of the finger edge



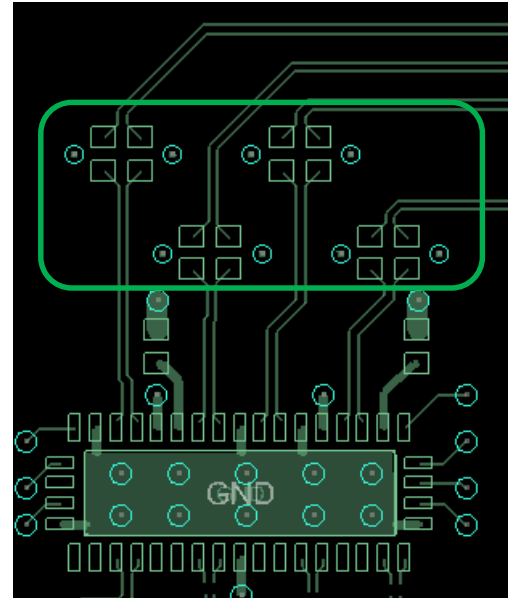
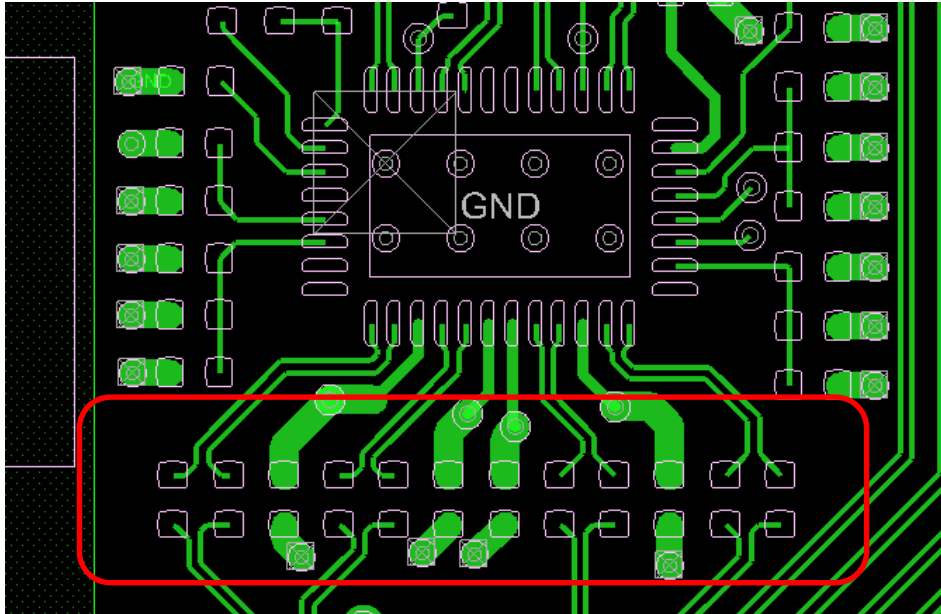
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- Add-In Cards: Within 400mils of the CEM connectors
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- Chip to chip connections, should be placed on the receiver side



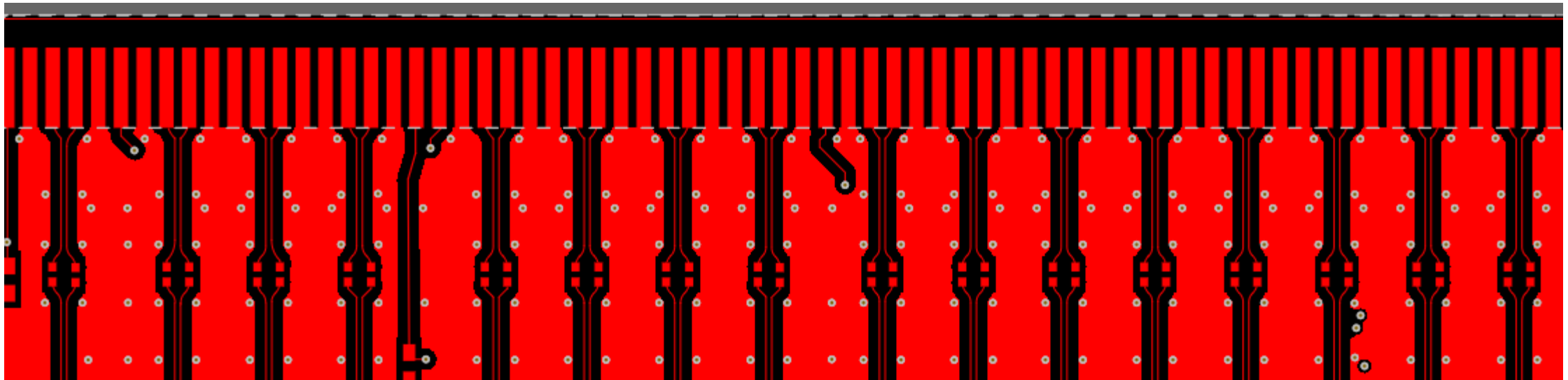
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- Chip to chip connections, should be placed on the receiver side
- Should be staggered to reduce plane disruption as much as possible
 - Improves high speed signal isolation as well



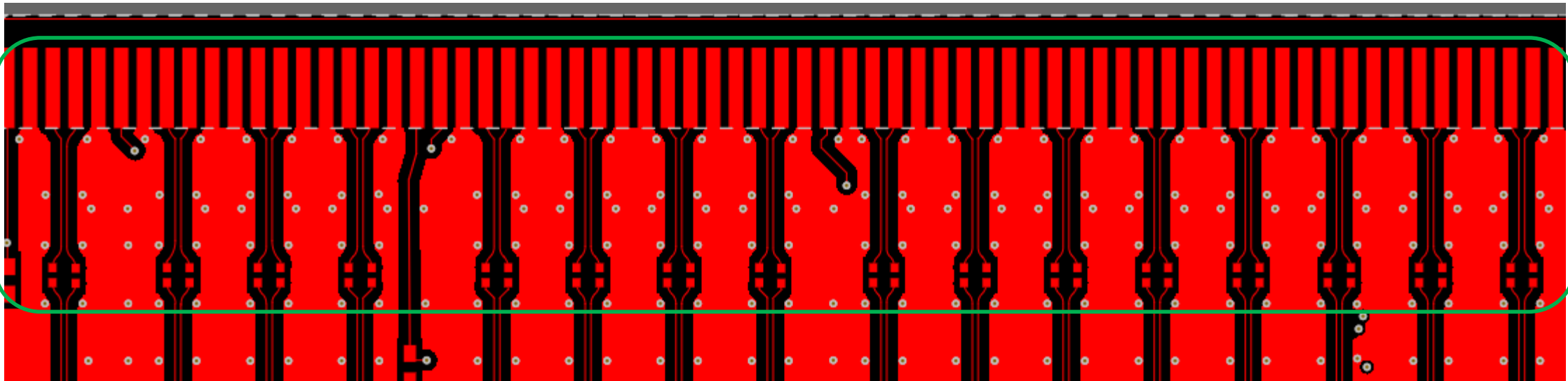
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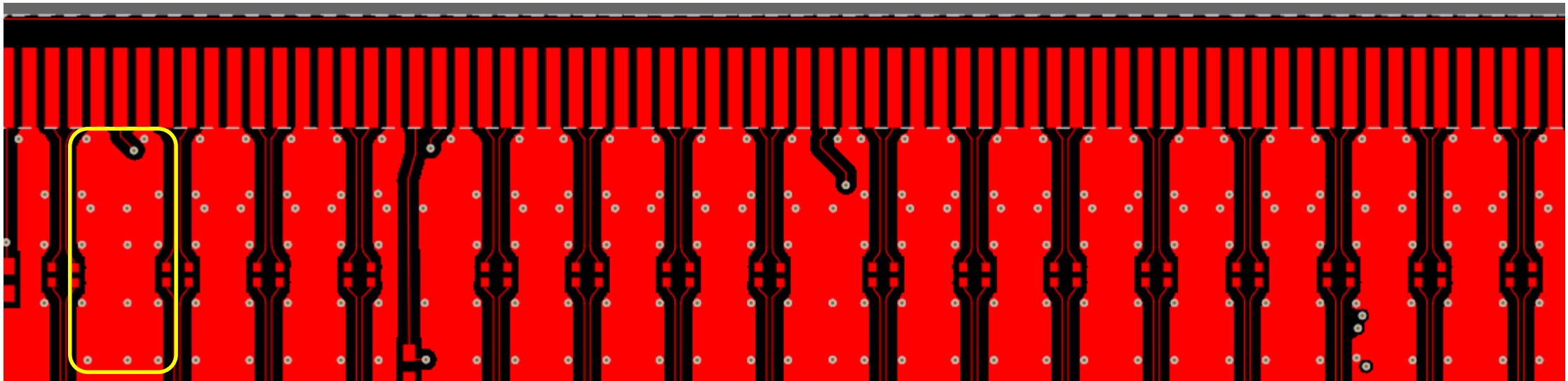
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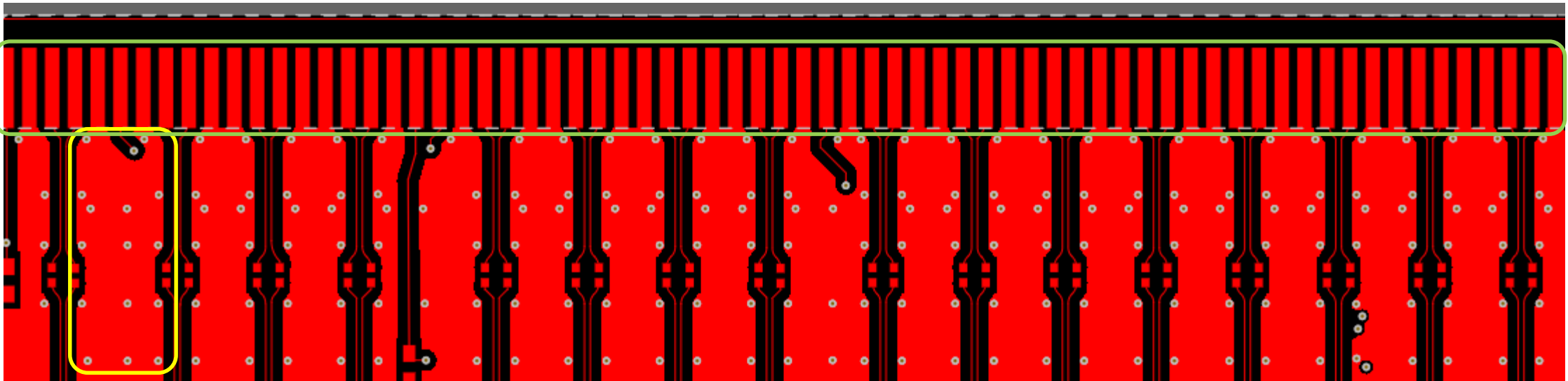
Cross talk mitigation

- GND Stitches along GND fill and vias



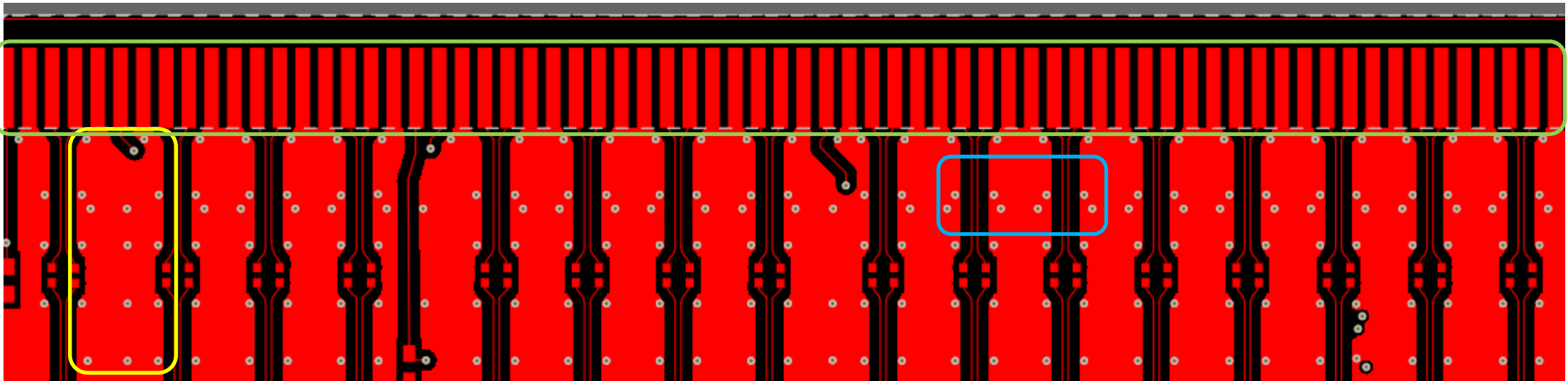
Cross talk mitigation

- GND Stitches along GND fill and vias
- Void under high speed pads – fingers and device



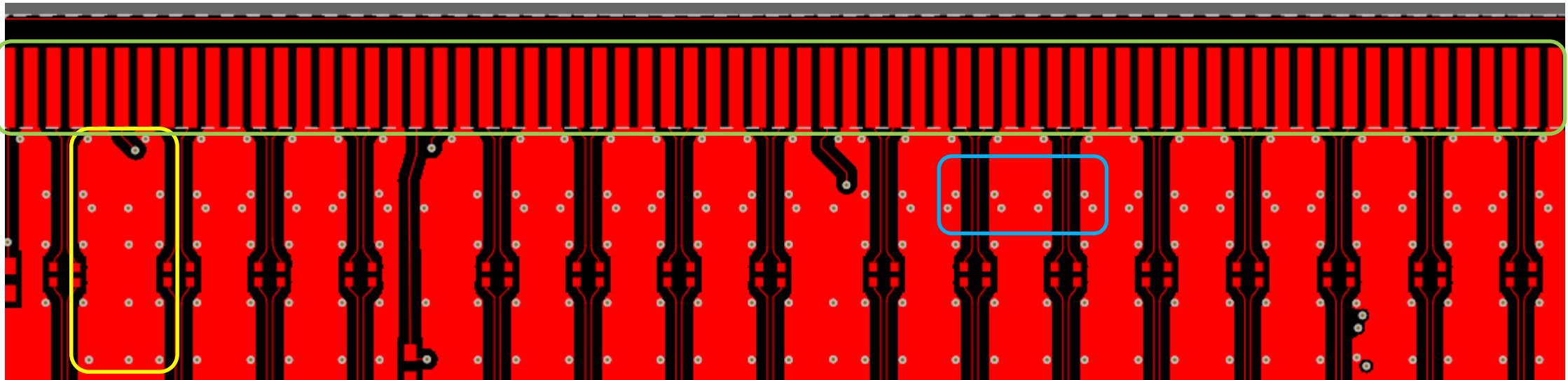
Cross talk mitigation

- GND Stitches along GND fill and vias
- Void under high speed pads – fingers and device
- Maintain differential trace impedance and distance from one another



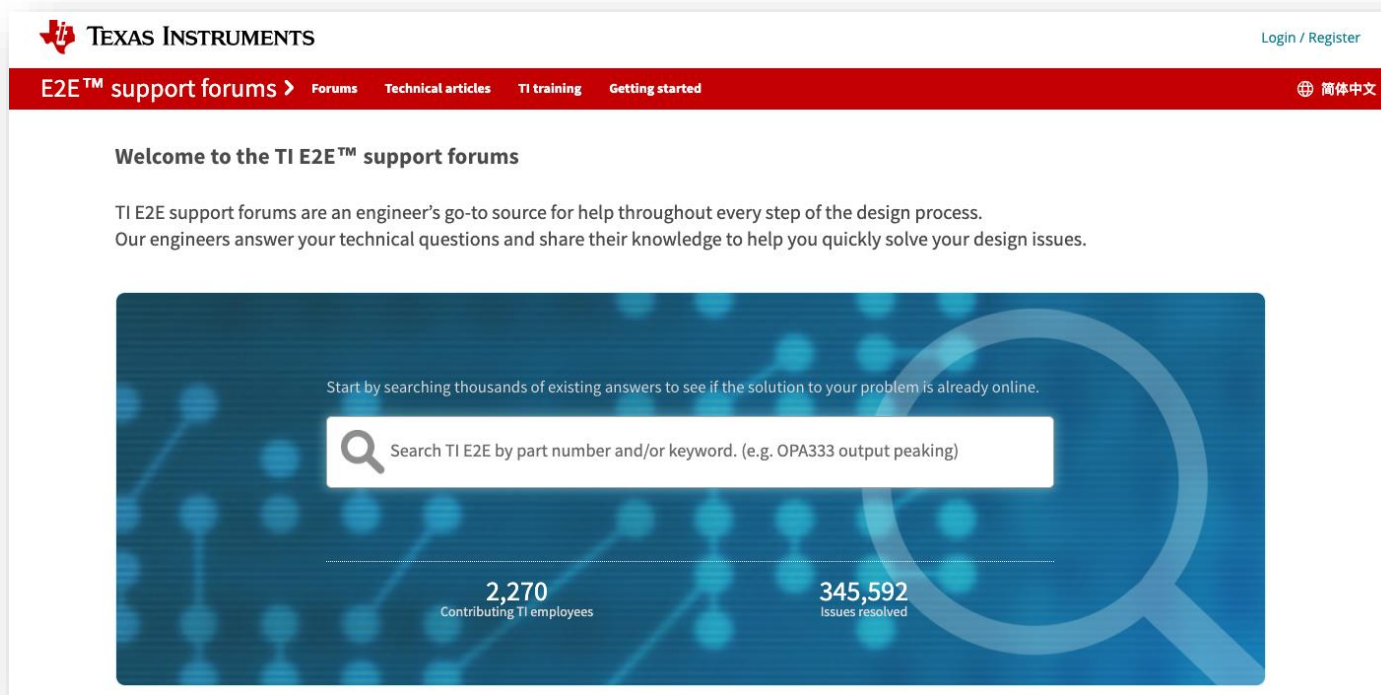
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Thank you

- TI Precision Labs – PCIe Solving Signal Integrity Challenges



The screenshot shows the homepage of the Texas Instruments E2E support forums. At the top left is the TI logo and "TEXAS INSTRUMENTS". At the top right are "Login / Register" and a language selector for "简体中文". A red navigation bar contains "E2E™ support forums > Forums Technical articles TI training Getting started". The main content area has a heading "Welcome to the TI E2E™ support forums" and a paragraph: "TI E2E support forums are an engineer's go-to source for help throughout every step of the design process. Our engineers answer your technical questions and share their knowledge to help you quickly solve your design issues." Below this is a search bar with the text "Start by searching thousands of existing answers to see if the solution to your problem is already online." and "Search TI E2E by part number and/or keyword. (e.g. OPA333 output peaking)". At the bottom of the search area, two statistics are displayed: "2,270 Contributing TI employees" and "345,592 Issues resolved".



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