PCle Signal Integrity Challenges and Remedies
TI Precision Labs – PCle

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### Five generations of PCI Express

<table>
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<tr>
<th>PCIe</th>
<th>Bandwidth</th>
<th>Line rate</th>
<th>Coding</th>
<th>UI</th>
<th>Media</th>
<th>Stressed eye</th>
<th>Eye pattern</th>
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</thead>
<tbody>
<tr>
<td>Gen 1.0 (2003)</td>
<td>250 MB/s</td>
<td><strong>2.5 Gbps</strong></td>
<td>8b/10b</td>
<td>400 ps</td>
<td>FR-4</td>
<td>Open – N/A</td>
<td><img src="image" alt="Eye Pattern" /></td>
</tr>
<tr>
<td>Gen 2.0 (2005)</td>
<td>500 MB/s</td>
<td><strong>5 Gbps</strong></td>
<td>8b/10b</td>
<td>200 ps</td>
<td>FR-4</td>
<td>Open – N/A</td>
<td><img src="image" alt="Eye Pattern" /></td>
</tr>
</tbody>
</table>
| Gen 3.0 (2010) | 1 GB/s    | **8 Gbps**   | 128b/130b | 125 ps  | FR-4             | HEO: ≤ 0.30 UI  
VEO: ≤ 25 mV | ![Eye Pattern](image) |
| Gen 4.0 (2017) | 2 GB/s    | **16 Gbps**  | 128b/130b | 62.5 ps | Low-loss PCB    | HEO: ≤ 0.30 UI  
VEO: ≤ 15 mV | ![Eye Pattern](image) |
| Gen 5.0 (2019) | 4 GB/s    | **32 Gbps**  | 128b/130b | 31.25 ps | Ultra-low-loss PCB | HEO: ≤ 0.30 UI  
VEO: ≤ 15 mV | ![Eye Pattern](image) |
Many channels can be serviced by a simple linear equalizer.

PCIe Gen3/4 insertion loss landscape model

Meet standard
Gen 4: ≤ 28dB
Gen 3: ≤ 22dB

Marginally over
Gen 4: < 40 dB
Gen 3: < 32 dB

Well beyond
Gen 4: > 40 dB
Gen 3: > 32 dB

Signal conditioning required

PCIe link channel loss (dB)*

* Gen3: [dB] @ 4 GHz
* Gen4: [dB] @ 8 GHz

Many channels can be serviced by a simple linear equalizer.
Signal conditioners to remedy impairments

Root complex

Linear driver(s)

Switch /endpoint

CTLE (Continuous time linear equalization)

Downstream EQ training

Upstream EQ training

Downstream EQ training

Upstream EQ training

Downstream 1 EQ training

Upstream 1 EQ training

Downstream 2 EQ training

Upstream 2 EQ training

TX
RX

TX
RX

TX
RX

TX
RX

TX
RX

TX
RX

TX
RX
PCle Gen4 without in-channel linear equalization

At signal source (< 1-dB loss)

After -24-dB channel
PCle Gen4 with in-channel linear equalization

The redriver restores horizontal and vertical eye opening

After -240-dB channel with no redriver CTLE

After -24-dB channel + redriver CTLE
PCle Gen4 with in channel linear equalization

Longer channel with redriver looks exactly like shorter channel without redriver

After -10 dB channel with no redriver

After -24 dB channel + redriver CTLE
PCIe Gen4 linear equalization – jitter comparison

After -10 dB channel with no redriver

Rj: + 100fs  Dj: + 2ps  Tj: + 3.4ps

After -24 dB channel + redriver CTLE
Short quiz

1. Check all correct statements:
   A. PCI Express is a serial bus protocol
   B. PCI Express uses a 100 MHz clock to provide robust setup and hold time on the PCI data
   C. PCI Express currently operates up to 16 Gbps
   D. PCI Express never uses any signal conditioning components

2. Check all correct statements:
   A. PCI Express is a widely used standard in computers
   B. Not all PCI Express channels will need signal conditioning
   C. Linear equalization can be very effective extending the reach of a PCIe link
   D. Protocol Aware Retimer operation is defined by the PCIe 4.0 standard.

3. PCI Express repeaters using Linear equalization have extremely low latency.
   A. True
   B. False
   C. Unknown