Inverter/PFC Converter Topology - Overview

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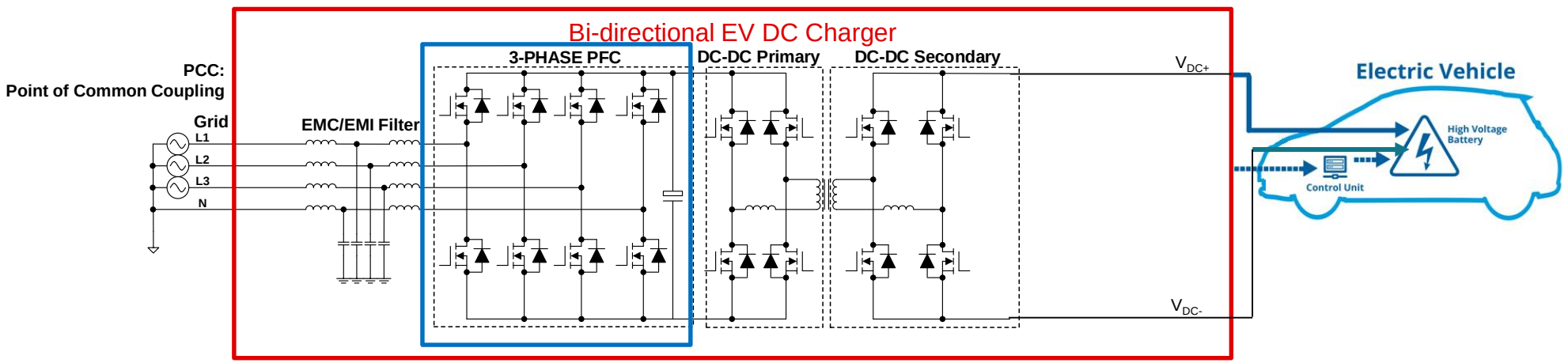
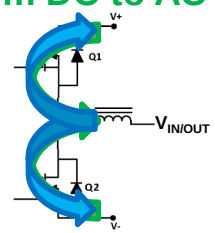
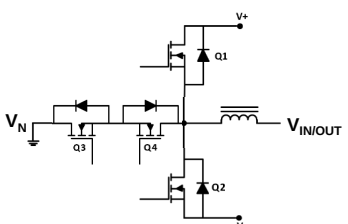
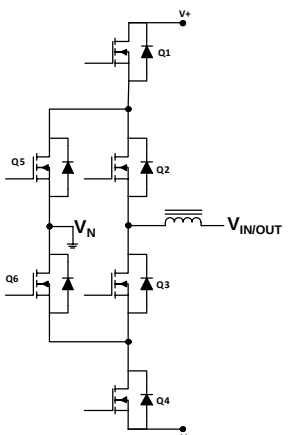
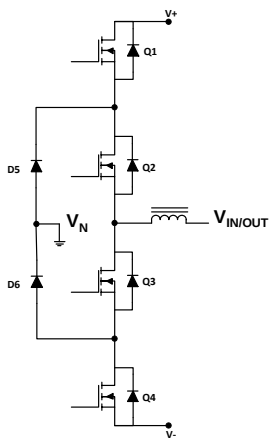
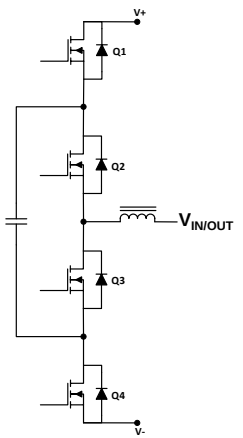
Power Conversion Building Blocks of a DC-Charger

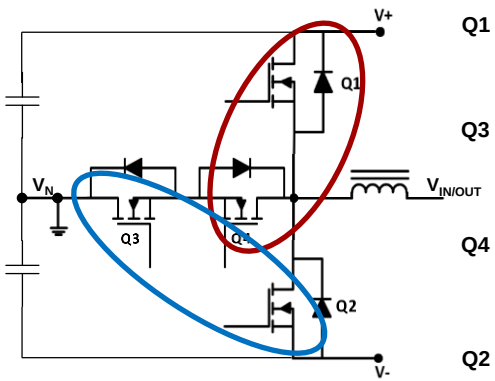


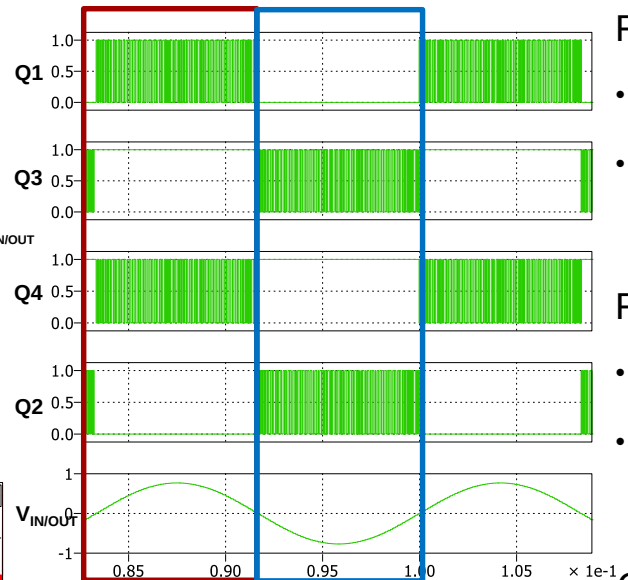
Inverter/PFC will be covered in this video

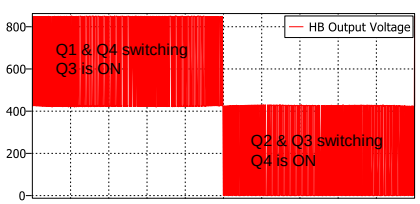
Topologies Overview on Inverter/PFC Power Stage

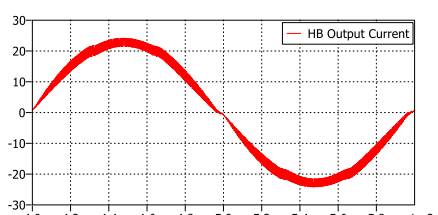
Topology	2L two level converter	T-Type 3L three level T-Type	ANPC 3L active neutral point converter	NPC 3L neutral point converter	FC3L Flying Capacitor 3L
Inverter Operation from DC to AC PFC Operation from AC to DC					

T-Type 3L – basic operation principle









For positive Sine-wave ($V_N \leq V_{IN/OUT} \leq V_+$) :

- Q1 and Q4 in red circle are switching f_{PWM}. Q3 is permanently in ON-state
- Dead time between Q1 and Q4 needs to be accounted for

For negative Sine-wave ($V_- \leq V_{IN/OUT} \leq V_N$) :

- Q2 and Q3 in blue circle are switching f_{PWM}. Q4 is permanently in ON-state
- Dead time between Q2 and Q3 needs to be accounted for

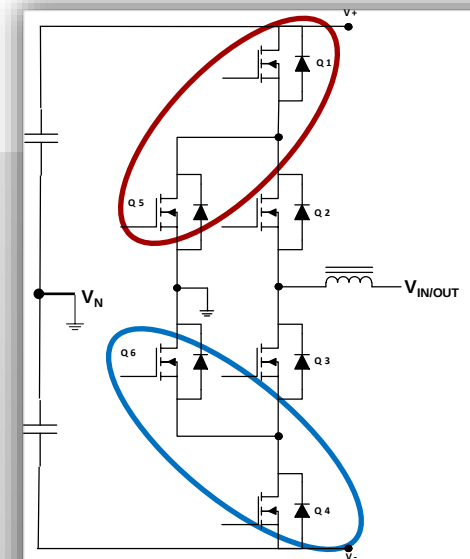
Output Ripple frequency f_{RIPPLE} equal to f_{PWM}

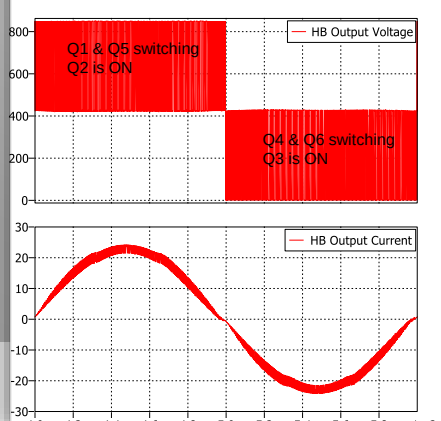
- f_{RIPPLE} defines size of filter components (magnetics and capacitors) for a given frequency

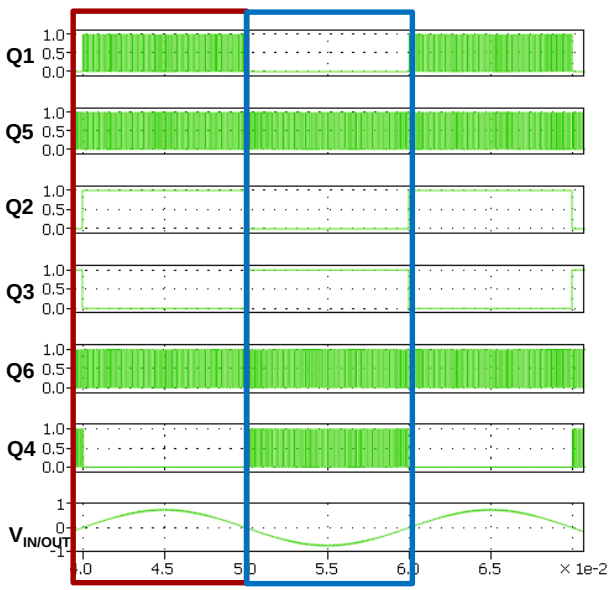
Q1 & Q2 need be V_{DC} – rated (i.e. for VDC 800V – 1200V rated)

Q3 & Q4 can be ½ V_{DC} – rated (i.e. for VDC 800V – 600V rated)

ANPC 3L – basic operation principle







For positive Sine-wave ($V_N \leq V_{IN/OUT} \leq V_+$) :

- Q1 and Q5 in red circle are switching f_{PWM}. Q2 is permanently in ON-state
- Additionally Q6 is switching with Q1 to keep ½ V_{DC} across Q3 / Q4

For negative Sine-wave ($V_- \leq V_{IN/OUT} \leq V_N$) :

- Q4 and Q6 in blue circle are switching f_{PWM}. Q3 is permanently in ON-state
- Additionally Q5 is switching with Q4 to keep ½ V_{DC} across Q1 / Q2

Output Ripple frequency f_{RIPPLE} equal to f_{PWM}

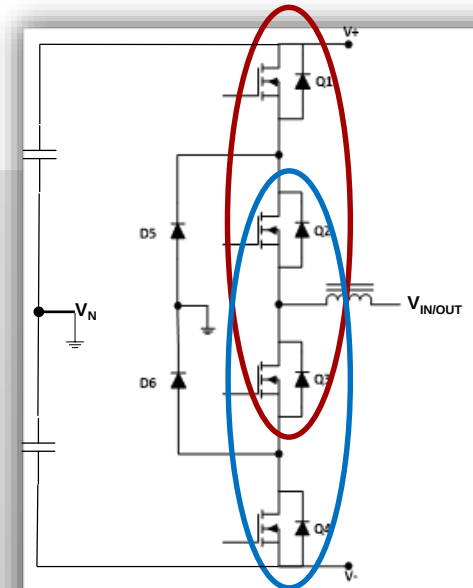
- Again f_{RIPPLE} defines size of filter components (magnetics and capacitors)

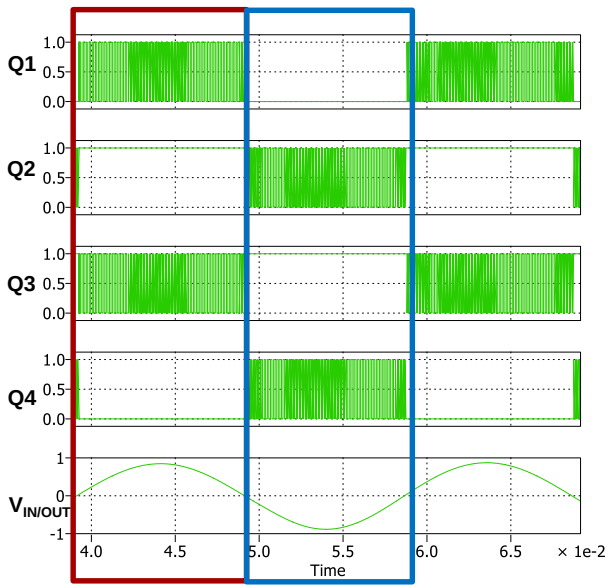
All switches can be ½ V_{DC} – rated (i.e. for VDC 800V – 600V rated)

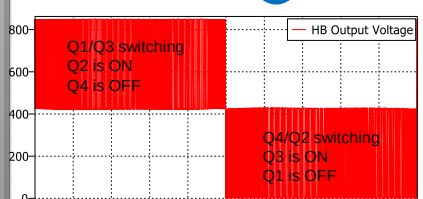
Q2 & Q3 are switching at f_{AC} (i.e. 50/60Hz)

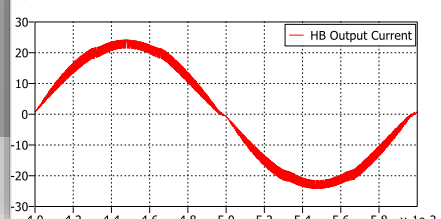
Critical shutdown sequencing – balancing of voltages to ½ V_{DC}

NPC 3L – basic operation principle









For positive Sine-wave ($V_N \leq V_{IN/OUT} \leq V_+$) :

- Q1 in red circle switching f_{PWL}. Q2 is permanently in ON-state
- Q3 is switching complementary with Q1 to keep ½ V_{DC} across Q3 / Q4

For negative Sine-wave ($V_- \leq V_{IN/OUT} \leq V_N$) :

- Q4 in blue circle switching f_{PWL}. Q3 is permanently in ON-state
- Q2 is switching complementary with Q4 to keep ½ V_{DC} across Q1 / Q2

Output Ripple frequency f_{RIPPLE} equal to f_{PWM}

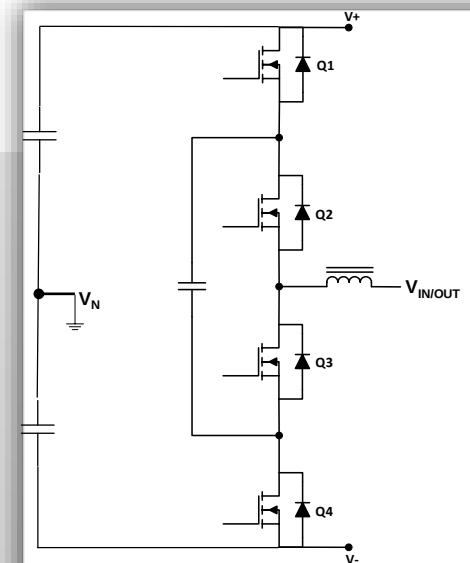
All switches can be ½ V_{DC} – rated (i.e. for VDC 800V – 600V rated)

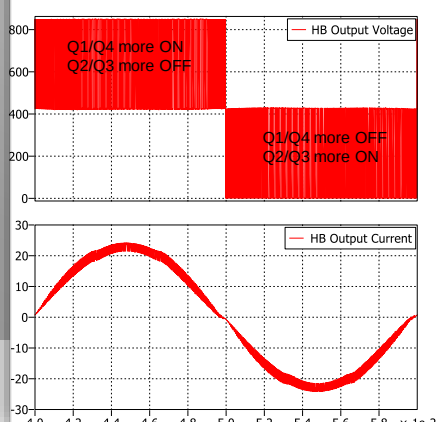
Q2 & Q3 are switching at f_{AC} (i.e. 50/60Hz)

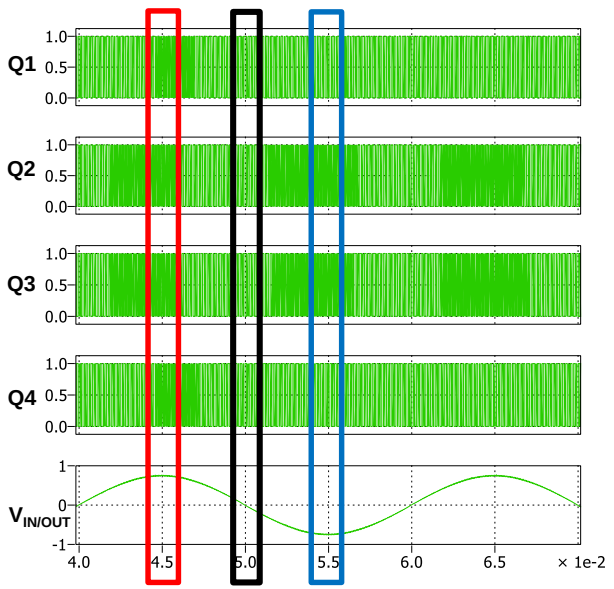
Efficiency is lower than ANPC

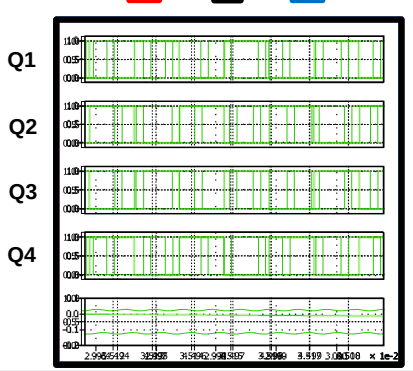
Critical shutdown sequencing – balancing of voltages to ½ V_{DC}

FC3L – basic operation principle









All FETs are switching f_{PWL}.

Pairs Q1/Q4 and Q2/Q3 are complementary to each other

For positive Sine-wave ($V_N \leq V_{IN/OUT} \leq V_+$) :

- At the +peak Q1/Q4 and Q2/Q3 are 180º phase-shifted to each other and Q1/Q2 are more in ON-state than Q3/Q4

For negative Sine-wave ($V_- \leq V_{IN/OUT} \leq V_N$) :

- At the -peak Q1/Q4 and Q2/Q3 are 180º phase-shifted to each other and Q1/Q2 are more in OFF-state than Q3/Q4

At zero Crossing:

- Duty cycle of Q1/Q4 and Q2/Q3 is each 50%

Output Ripple frequency f_{RIPPLE} equal to 2 x f_{PWM}

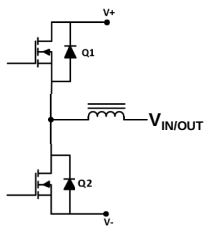
- This defines smaller size of filter components (magnetics and capacitors)

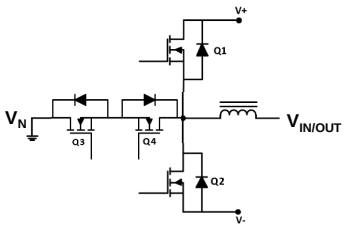
All switches can be ½ V_{DC} – rated (i.e. for VDC 800V – 600V rated)

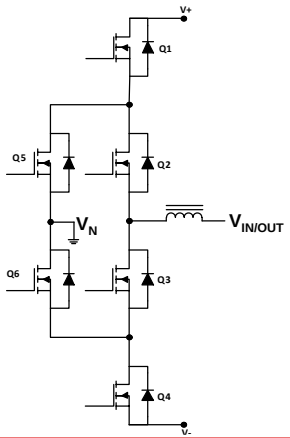
Initial Charging of Flying Cap to ½ V_{DC} is critical

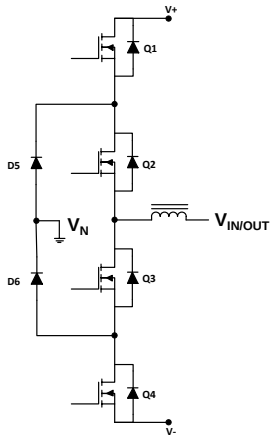
Critical shutdown sequencing – balancing of voltages to ½ V_{DC}

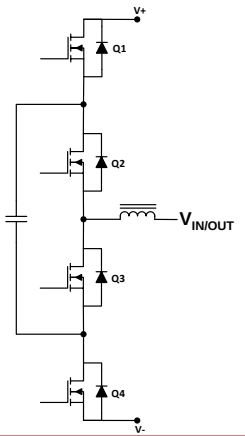
Multilevel Topologies Summary on Inverter/PFC Power Stage











	2L TIDA-01606 in 2L	T-Type 3L TIDA-01606	ANPC TIDA-010210	NPC 3L derived from ANPC	FC3L Flying Capacitor 3L
Benefits	• Simple control scheme • 2 switches only • 2 PWM	• Easy control scheme • Q3/Q4 see ½ V_{DC} • Better EMI than 2L • $f_{RIPPLE} = f_{PWM}$	• Good efficiency • All switches see ½ V_{DC} • Better EMI than 2L • $f_{RIPPLE} = f_{PWM}$	• Lower cost than ANPC • All switches see ½ V_{DC} • Better EMI than 2L • $f_{RIPPLE} = f_{PWM}$ • 4 PWM	• Highest efficiency • Only 4 HF FETs (& 1Cap) • $f_{RIPPLE} = 2 \times f_{PWM}$ • Smallest magnetics • Lowest EMI
Challenges	• Q1/Q2 see full V_{DC} • High EMI for higher f_{PWM} • Passives are biggest	• Q1/Q2 see full V_{DC} • 4 PWM	• More complex control scheme • Shutdown sequencing critical • 6 PWM	• Lower efficiency than ANPC • More complex control • Shutdown sequencing critical	• Initial charging of flying capacitor • Shutdown sequencing critical

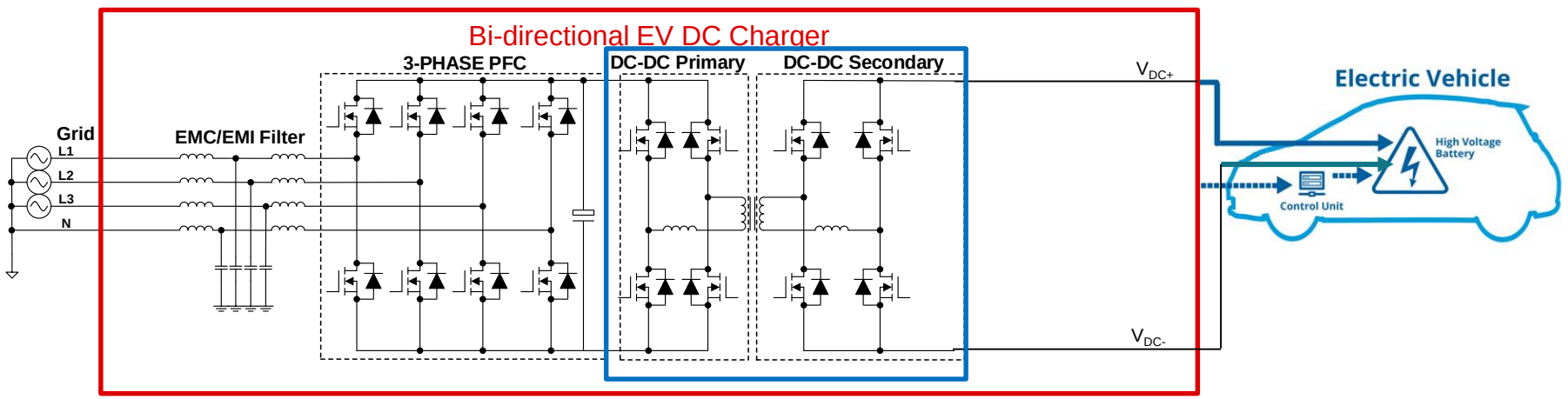
Visit:
https://ti.com/tool/TIDA-01606
https://ti.com/tool/TIDA-010210

Multilevel topologies benefits

Multilevel topologies in PFC/Inverter Stage

- Three level topologies keep the switching voltage to half of a 2-level converter which **improves overall EMI**
- Multilevel topology enables **FETs with significantly lower switching and conduction losses** which improves efficiency by using FETs with half the blocking voltage for the same DC bus voltage
- Faster f_{PWM} enables smaller passives with up to **50% reduction in size** for a 3-level converter vs. a 2-level converter. Can be further improved with 3-level flying cap topology.

Outlook



Isolated DC/DC converter will be covered in next video

THANKS