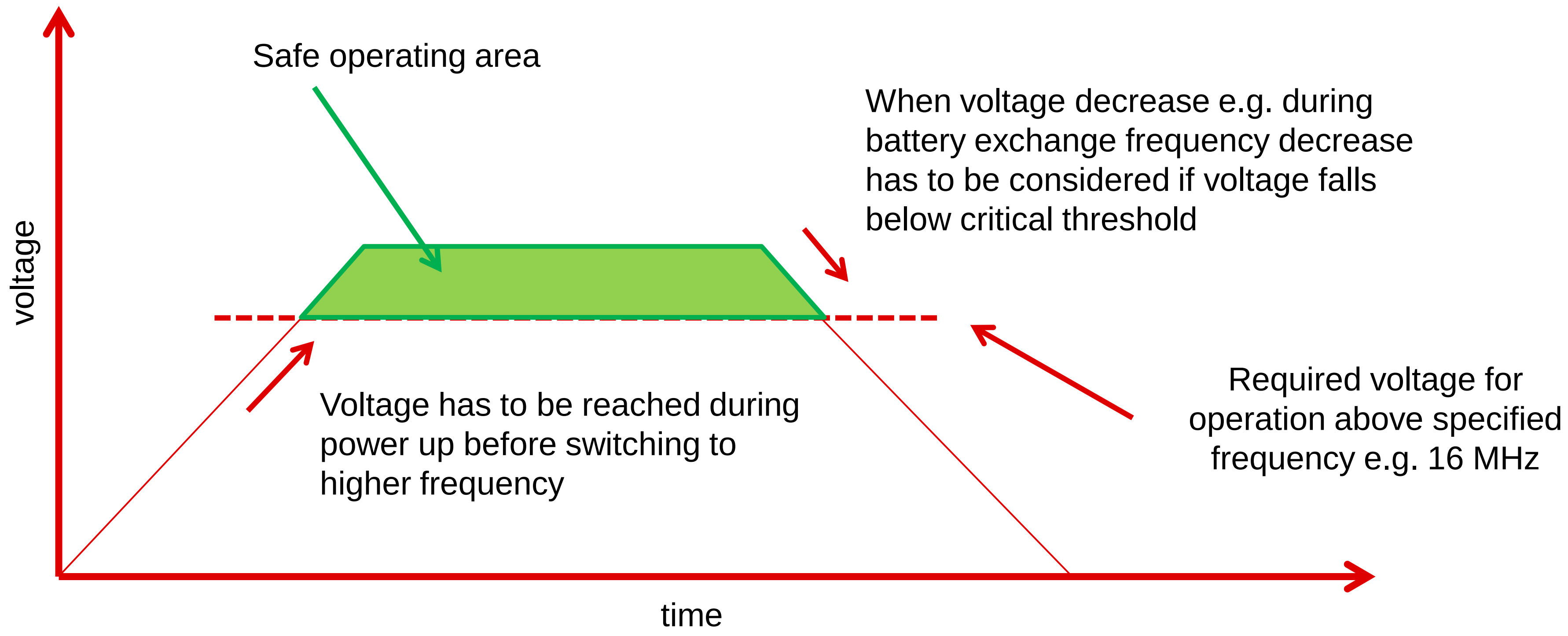
Power supply considerations using TI MSP430 Microcontrollers

Dietmar Walther – CMCU Quality

Power Supply Considerations



Used example code

msp430x22x4_clks.c

```
#include <msp430.h>

int main(void)
{
  int i=0;
  P2DIR |= 0x02;                          // P2.1 output direction
  P2SEL |= 0x02;                          // P2.1 = SMCLK

  P4OUT &= ~0x88;
  P4DIR |= 0x88;                          // P4.4 and P4.7 output direction

  WDTCTL = WDTPW + WDTHOLD;               // Stop Watchdog Timer
  if (CALBC1_16MHZ==0xFF)                 // If calibration constant erased
  {
    while(1);                             // do not load, trap CPU!!
  }

  P4OUT |= 0x08;
  DCOCTL = 0;                             // Select lowest DCOx and MODx settings
  BCSCTL1 = CALBC1_16MHZ;                  // Set DCO to 16MHz
  DCOCTL = CALDCO_16MHZ;
  P4OUT &= ~0x08;

  while (1)
  {
    P4OUT |= 0x080;
    // P4.7 = 1

    P4OUT &= ~0x080;                       // P4.7 = 0

  }
}
```

Implemented Supply Control Circuits!

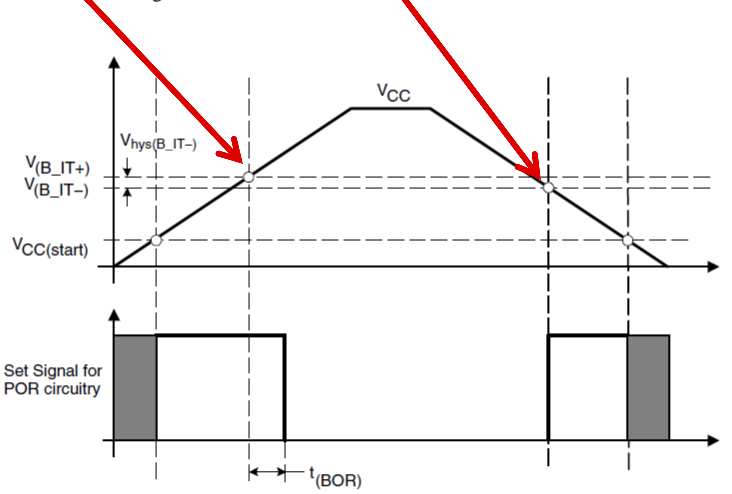
- Brownout circuit
  → fixed voltage supervisor which controls device release at the minimum allowed voltage (safety net)
  → hysteresis implemented to operate during power up and power down

1. Brownout reset (BOR) circuit occurs when the device is powering up initializes the system

2. Also functions when no SVS is enabled and a brownout condition occurs

3. Sustains this reset until the input power is sufficient for the logic

Figure 2–2. Brownout Timing



TEXAS INSTRUMENTS

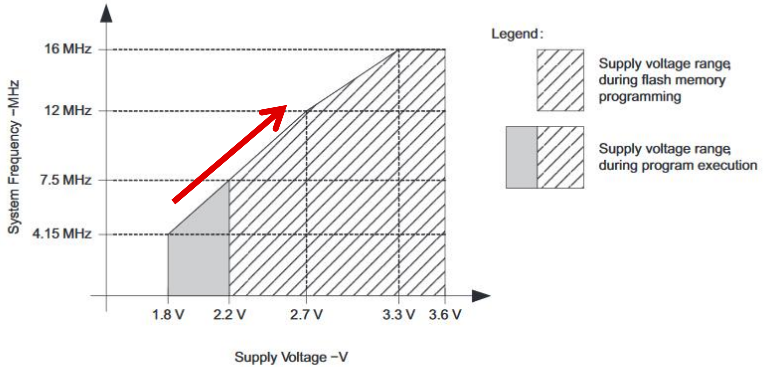
Used example code with delay loop

msp430x22x4_clks.c *

```c
#include <msp430.h>

int main(void)
{
  int i=0;
  P2DIR |= 0x02;                            // P2.1 output direction
  P2SEL |= 0x02;                            // P2.1 = SMCLK

  P4OUT &= ~0x88;
  P4DIR |= 0x88;                            // P4.4 and P4.7 output direction

  for(i=0;i<250;i++);                        // for turn on with 2ms ramp up time

  WDTCTL = WDTPW + WDTHOLD;                 // Stop Watchdog Timer
  if (CALBC1_16MHZ==0xFF)                   // If calibration constant erased
  {
    while(1);                               // do not load, trap CPU!!
  }

  P4OUT |= 0x08;
  DCOCTL = 0;                               // Select lowest DCOx and MODx settings
  BCSCTL1 = CALBC1_16MHZ;                    // Set DCO to 16MHz
  DCOCTL = CALDCO_16MHZ;
  P4OUT &= ~0x08;

  while (1)
  {
    P4OUT |= 0x080;
    // P4.7 = 1

    P4OUT &= ~0x080;                         // P4.7 = 0

  }
}
```

Differences in MSP430 device families!

- Which clock frequency at which voltage?
  1. For F1xx, F2xx and F4xx the supply voltage has to be reached sufficient level before increase operating frequency!



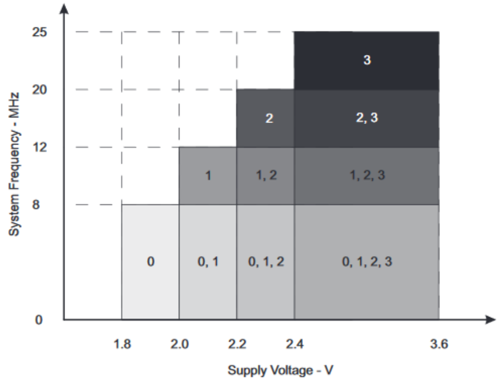
NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Operating Area

Differences in MSP430 device families!

- Which clock frequency at which voltage?
  1. For F1xx, F2xx and F4xx the supply voltage has to be reached sufficient level before increase operating frequency!

  2. For F5xx/F6xx the sub regulated onboard LDO voltage level has to be considered in addition.



NOTE: The numbers within the fields denote the supported PMMCOREVx settings.

Figure 5-1. Maximum System Frequency

Differences in MSP430 device families!

- Which clock frequency at which voltage?
  1. For F1xx, F2xx and F4xx the supply voltage has to be reached sufficient level before increase operating frequency!

  2. For F5xx/F6xx the sub regulated onboard LDO voltage level has to be considered in addition.

  3. For FRxx device family the supply vs. frequency dependencies are much more relaxed due to improved design.

5.3 Recommended Operating Conditions

Typical data are based on V_{CC} = 3.0 V, T_A = 25°C (unless otherwise noted)

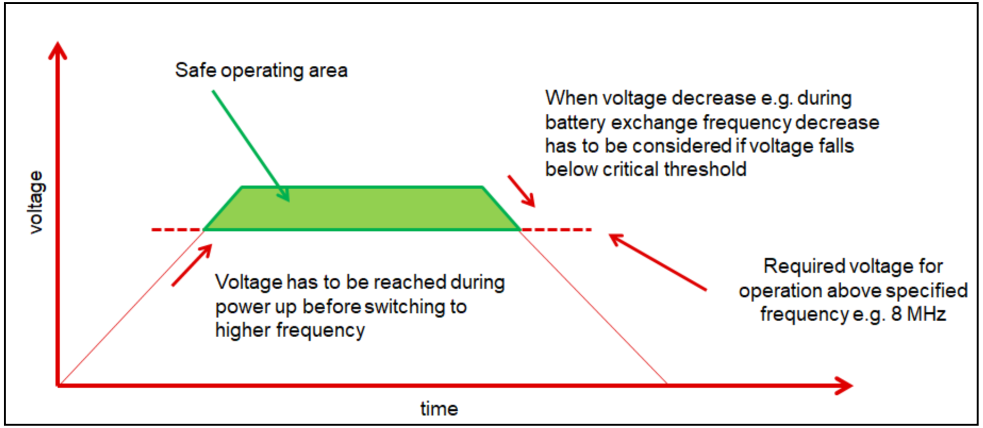
			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range applied at all DVCC and AVCC pins[1] [2] [3]		1.8[4]		3.6	V
V_{SS}	Supply voltage applied at all DVSS and AVSS pins			0		V
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature		–40		85	°C
C_{DVCC}	Capacitor value at DVCC[5]		$1_{-20\%}$			µF
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)[6]	No FRAM wait states (NWAITSx = 0)	0		8[7]	MHz
		With FRAM wait states (NWAITSx = 1)[8]	0		16[9]	
f_{ACLK}	Maximum ACLK frequency				50	kHz
f_{SMCLK}	Maximum SMCLK frequency				16[9]	MHz

Wrap Up

1. Check out device specific datasheet and users guide for dedicated operating conditions and implemented supply voltage control features!

2. Consider possible supply variation scenarios on application level meeting supply voltage control circuit specifications like
   - Voltage thresholds
   - Hysteresis voltage
   - Voltage slew rates for power up & down

3. Keep in mind!
   It is essential to consider the recommended operating conditions during whole operation window



Backup

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Implemented Supply Control Circuits!

- Brownout circuit
  → fixed voltage supervisor which controls device release at the minimum allowed voltage (safety net)

- Supply Voltage Supervisors
  → mostly configurable supervisors to react on supply changes aligned to application use case

- User configurable supply supervision using integrated ADC modules
  → user definable and configurable supply voltage control

5.21 PMM, Brownout Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(DVCC\_BOR\_IT-)}$	BOR_H on voltage, DV_{CC} falling level	$\lvert dDV_{CC}/d_t \rvert < 3$ V/s			1.45	V
$V_{(DVCC\_BOR\_IT+)}$	BOR_H off voltage, DV_{CC} rising level	$\lvert dDV_{CC}/d_t \rvert < 3$ V/s	0.80	1.30	1.50	V
$V_{(DVCC\_BOR\_hys)}$	BOR_H hysteresis		50		250	mV
t_{RESET}	Pulse duration required at $\overline{RST}$/NMI pin to accept a reset		2			µs

5.23 PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSH)}$	SVS current consumption	SVSHE = 0, DV_{CC} = 3.6 V		0		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 0		200		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 1		2.0		µA
$V_{(SVSH\_IT-)}$	SVS_H on voltage level(1)	SVSHE = 1, SVSHRVL = 0	1.59	1.64	1.69	V
		SVSHE = 1, SVSHRVL = 1	1.79	1.84	1.91	
		SVSHE = 1, SVSHRVL = 2	1.98	2.04	2.11	
		SVSHE = 1, SVSHRVL = 3	2.10	2.16	2.23	
$V_{(SVSH\_IT+)}$	SVS_H off voltage level(1)	SVSHE = 1, SVSMHRRL = 0	1.62	1.74	1.81	V
		SVSHE = 1, SVSMHRRL = 1	1.88	1.94	2.01	
		SVSHE = 1, SVSMHRRL = 2	2.07	2.14	2.21	
		SVSHE = 1, SVSMHRRL = 3	2.20	2.26	2.33	
		SVSHE = 1, SVSMHRRL = 4	2.32	2.40	2.48	
		SVSHE = 1, SVSMHRRL = 5	2.56	2.70	2.84	
		SVSHE = 1, SVSMHRRL = 6	2.85	3.00	3.15	
		SVSHE = 1, SVSMHRRL = 7	2.85	3.00	3.15	
$t_{pd(SVSH)}$	SVS_H propagation delay	SVSHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVSHFP = 1		2.5		µs
		SVSHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVSHFP = 0		20		
$t_{(SVSH)}$	SVS_H on or off delay time	SVSHE = 0→1, SVSHFP = 1		12.5		µs
		SVSHE = 0→1, SVSHFP = 0		100		
dV_{DVCC}/dt	DV_{CC} rise time		0		1000	V/s