RF PLLs and Synthesizers: Key Parameters and Specifications

TI Precision Labs – Clocks and Timing

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Phase lock loop (PLL) overview
Phase lock loop (PLL) overview

- Carefully *design loop filter* to meet phase noise, lock time and spurs requirement
- Key parameters and specifications for a design
  - Phase detector frequency
  - Charge pump current
  - VCO gain
  - PLL and VCO noise
  - Spurs
  - Lock time
- Design tools
  - Clock Architect
  - PLLatium Sim
PLL – Flicker noise and FOM

• Normalized PLL 1/f noise (Flicker noise)
  – Usually dominates at offset below 1 kHz
  – Typical value better than -120 dBc/Hz
• Normalized PLL noise floor (FOM)
  – Determines phase noise at mid-range offset
  – Typical value better than -230 dBc/Hz
PLL – N Divider noise

- Normalized PLL 1/f noise (Flicker noise)
  - Usually dominates at offset below 1 kHz

- Normalized PLL noise floor (FOM)
  - Determines phase noise at mid-range offset

- N-counter
  - Added noise = 20\log_{10}(N)
  - e.g. added noise = 40 dB for N = 100
PLL – Total PLL noise (in-band noise)

- Normalized PLL 1/f noise (Flicker noise)
  - Usually dominates at offset below 1 kHz

- Normalized PLL noise floor (FOM)
  - Determines phase noise at mid-range offset

- N-counter
  - Added noise = 20log(N)

- Total noise determines PLL in-band noise
Phase detector frequency, $f_{PD}$

- $f_{PD} = \text{Reference clock frequency} / R$
- Rising edge of R-divider signal triggers phase comparison
- Max. $f_{PD}$ is usually less than 300 MHz
Charge pump current

- Constant current source
- Turn-on time is variable
- Current is configurable
  - 100 µA to a few mA per step
VCO gain, $K_{\text{vco}}$

- Use a varactor diode to change the oscillator frequency

- Tuning range is limited

- $K_{\text{vco}}$
  - Changes in frequency against $V_{\text{tune}}$
  - Varies across the whole VCO tuning range
  - A few MHz/V to more than a 100 MHz/V

A typical Colpitts oscillator
VCO phase noise

• Determines closed-loop far-out phase noise
VCO phase noise

• Determines closed-loop far-out phase noise

• Phase noise
  – SSB power difference between the carrier and an offset, normalized in 1 Hz
  – Expressed in $xx$ dBc/Hz@ $yy$ Hz offset
  – Carrier frequency specific

-121 dBc/Hz @ 100 kHz offset at 2.1 GHz carrier
**Spurs**

- **Phase detector spurs**
  - Offset = $f_{PD}$
- **Fractional spurs**
  - Offset = $N_{frac} \times f_{PD}$
- **Sub-fractional spurs**
  - $\frac{1}{2}$, $\frac{1}{4}$ of fractional spurs
- **Crosstalk spurs**
  - Crosstalk between
    - Phase detector and VCO
    - Integer Boundary Spurs (IBS)
  - Phase detector and output
  - Reference clock and output
  - Reference clock and VCO
Lock time

- Lock time is how long it takes to change one frequency to another and get within a certain frequency tolerance
- Wide loop bandwidth reduces lock time
- Lock time $\approx \frac{4}{\text{loop bandwidth}}$
Applying key parameters and specifications
Phase detector frequency

\[ f_{PD} \] determines N-divider value
Charge pump current

Charge pump gain
VCO gain
VCO phase noise
PLL noise
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Quiz

• True or false: VCO phase noise determines closed-loop close-in phase noise

• True or false: N-divider will increase PLL noise by 20\log(N)

• True or false: Phase detector is triggered by the rising edge of the N-divider signal

• True or false: Turn-on time of the charge pump is proportional to the phase difference between the signals from R-divider and N-divider

• True or false: Phase detector spur frequency is not predictable
Quiz

• True or **false**: VCO phase noise determines closed-loop close-in phase noise

• **True** or false: N-divider will increase PLL noise by $20\log(N)$

• True or **false**: Phase detector is triggered by the rising edge of the N-divider signal

• **True** or false: Turn-on time of the charge pump is proportional to the phase difference between the signals from R-divider and N-divider

• True or **false**: Phase detector spur frequency is not predictable