Quiz

1. True or false: SYSREF is used to synchronize a JESD204B system when using subclass 1?
2. True or false: JESD204B simplifies PCB design for data traces?
3. True or false: The SYSREF valid window is the time in which a rising SYSREF edge must occur to deterministically mark a device clock as a time reference point?
4. True or false: AC coupling clocks simplifies the interface as common mode voltage is of no concern?
5. True or false: DC coupling the SYSREF simplifies synchronization of the JESD204B system?

Quiz: Answers

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