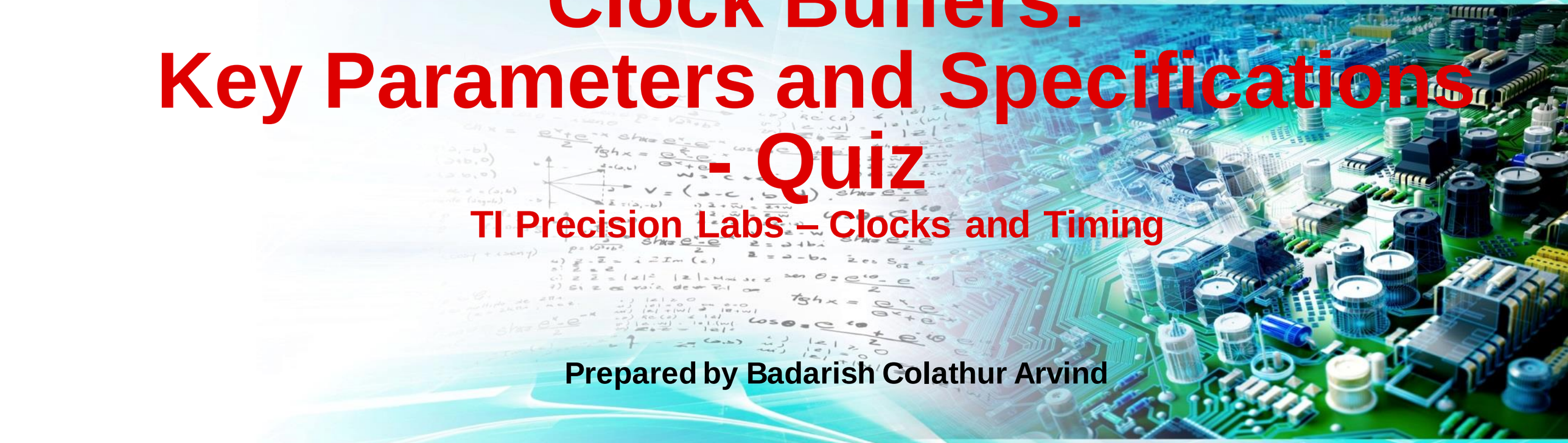
Clock Buffers: Key Parameters and Specifications - Quiz

TI Precision Labs – Clocks and Timing



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Quiz

- True or false: Single ended buffers are immune to external noise coupling
- True or false: For a given VDD, CMOS buffers provide the highest output amplitude
- True or false: Increasing the input slew rate and input amplitude reduces the output additive jitter of the buffer
- True or false: An university student connects 4 ADCs in parallel to increase the resolution of her EE101 lab measurement. She uses a 1:4 clock buffer to distribute the clock to the 4 ADCs. The ADC has a specification for device to device aperture delay variation of ±0.1 ns, while the buffer has a channel to channel skew of 250 ps. Does the skew specification of the buffer meet the ADC aperture delay requirements

Quiz

- True or false: Single ended buffers are immune to external noise coupling
- True or false: For a given VDD and a capacitive load, CMOS buffers provide the highest output amplitude
- True or false: Increasing the input slew rate and input amplitude reduces the output additive jitter of the buffer
- True or false: An university student connects 4 ADCs in parallel to increase the resolution of her EE101 lab measurement. She uses a 1:4 clock buffer to distribute the clock to the 4 ADCs. The ADC has a specification for device to device aperture delay variation of ±0.1 ns, while the buffer has a channel to channel skew of 250 ps. Does the skew specification of the buffer meet the ADC aperture delay requirements

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