Resolving high-voltage gate driver challenges in wide $V_{IN}/V_{OUT}$ converters

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What will I get out of this session?

• Purpose:
  ✓ Review full-bridge and buck-boost topologies (telecom/RRU/others)
  ✓ Understand gate driver challenges in these topologies
  ✓ Discuss possible solutions to these gate driver challenges
  ✓ Systems that have wide input wide output requirement will face the same challenges

• Part numbers mentioned:
  • UCC21225, UCC27710/2
  • UCD3138, LM5161

• Reference designs mentioned:
  • PMP20587

• Relevant end equipment:
  • Telecom power supplies
  • Automotive power supplies
  • Merchant supplies
Challenges in designing advanced power supplies?

- Robustness
- Efficiency
- Density
- Wide input/output range
- Cost sensitivity
Full-bridge – popular topology used in RRU power supplies

\[ V_o = N \times D \times V_{in} \]

Where –

- \( V_o \) = output voltage
- \( V_{in} \) = input voltage
- \( D \) = duty ratio (Ton/T)
- \( N \) = turns ratio

- Topology is also used in many other applications
Challenges/observations with full-bridge full-bridge topology

- Multiple primary and secondary side bias exist
- Secondary side control
- >100V half-bridge drivers for primary side
- >100V half-bridge driver for secondary side
- Isolated gate driver can replace isolator and primary side half-bridge driver

![Diagram](image)
Challenges/observations with full-bridge full-bridge topology

- Need two dual channel isolated driver
- If controller is on primary side, then use two isolated gate drivers on secondary side and 100V half-bridge driver on primary side
- Good switching characteristics, robustness, and size of the gate driver is important
Buck-boost popular topology used in RRU power supplies

\[ V_o = - V_{in} \times \left( \frac{D}{1-D} \right) \]

Where –

- \( V_o \) = output voltage
- \( V_{in} \) = input voltage
- \( D \) = duty ratio \( (T_{on}/T) \)

- No galvanic isolation
- Multiple phases required to match power rating of full-bridge
Challenges/observations with synchronous buck-boost

- Separate controller ground and driver ground
- Level shift between controller output and driver input is required
- Requires at least two bias supplies
- Isolated gate driver can be used
  - Better CMTI & noise immunity
  - Large package size
  - Cost

Vin: 36V-75V
Vo: 18V-55V
Controller
Driver
Isolated/Non-isolation?
Bus voltage?
Bias supply?
Ground?
Level Shift?
Challenges/observations with synchronous buck-boost

• For higher power multi-phase buck-boost is generally used
• Phases are generally interleaved for output ripple rejection
• Isolated driver and low-side driver can be used in multi-phase buck-boost if input to the low-side driver is isolated through normal signal isolator
What are key gate driver considerations?

- Voltage rating
- Number of channels
- Drive strength or rise/fall time
- Propagation delay
- Delay matching
- Robust (negative voltage handling)
- Package size
- Cost
Excellent switching characteristics (fast rise/fall times, low propagation delay, and low delay mismatch) of gate driver IC is a must requirement to achieve high efficiency
Gate driver considerations – UCC21225 characteristics

Input negative voltage (-5V)

Output negative voltage (-2V)
Another approach with synchronous buck-boost

- Separate controller ground and driver ground
- Level shift between controller output and driver input is a must
- Requires at least two bias supplies
- Half-bridge driver can be used
  - Good negative voltage handling
  - Smaller package size
  - Cost effective
  - Discrete level-shifter considerations
Discrete level shifter at the input of HB driver

Ch1=HO
Ch2=LO
Ch3=HI LS input
Ch4=LI LS input
$\text{DR_{Prop. Delay}} = 23\text{ns}$

- Additional prop. delay due to LS=4ns
- Additional delay mismatch due to LS=1ns
Level shifter implementation challenges/considerations

- **Digital controller output**
  - **3.3V or less voltage**
    - Low voltage makes it difficult to generate output voltage higher than gate driver input high threshold without increasing the level shifter load resistor \( R_L \) or without increasing the current
  - **10mA or less current**
    - Low digital controller output current forces the design toward high level shifter input resistor, which in turn causes larger propagation delay through level shifter and large rise/fall time
Level shifter implementation challenges/considerations

- Discrete transistors
  - Power dissipation
    - Better timing characteristic requires higher current through the transistor. This high current in combination with high bus voltage causes high power dissipation on the transistor.
  - Parameter variations
    - Variations in capacitance and other transistor characteristics might introduce larger prop delay and delay mismatch.
Possible solutions to level shifter challenges

- **Better level shifter**
  - Level shifter can be redesigned for better performance, but the component count will increase and therefore also the cost and area required on the board

- **Bigger/better transistor**
  - High bandwidth transistor can possibly improve the performance, but it will cost more

- **Reduce emitter current**
  - Increasing RE and RC will reduce the current further and that will reduce the power dissipation, but the propagation delay might increase
Level shifter performance with half-bridge driver

Ch1=HO
Ch2=LO
Ch3=HI LS input
Ch4=LI LS input
$R_B=300\,\Omega \quad R_L=390\,\Omega$

$I_B < 5\,mA$

Propagation delay increase by $\sim 8\,\text{ns}$

$Q_{P\text{-Diss}} = \sim 300\,\text{mW}$

Note: disregard second scope measurement (i.e. 72\,\text{ns}). This is due to triggering error of the scope. Actual measurement is close to the first one (33\,\text{ns}, 37\,\text{ns}).
Modified level shifter at the input of HB driver

- Resistor added to share the transistor power dissipation
- Resistor values increased to reduce current & dissipation

$R_B = 511\,\Omega$, $R_L = 650\,\Omega$, $R_C = 3.3k\,\Omega$,

$I_B < 3.3\,mA$ (compared to 10mA with original design)
Total prop. delay increases to $\sim50\,ns$

$Q_{P_{\text{Diss}}} = \sim175\,mW$
Modified level shifter performance with half-bridge driver

Ch1=LS input
Ch2=DR output

Total prop delay < 50ns
Delay mismatch < 5ns
Possible solution for applications where minimum dead time is 50ns-60ns
Summary

• Full-bridge topology with full-bridge synchronous rectifier and negative input synchronous buck-boost converters are commonly used power supply topologies in remote radio units (RRU)

• Half-bridge gate drivers rated at >100V, with good drive strength, small in size, and good negative voltage handling capability can be used in both full-bridge and synchronous buck-boost topologies

• External level shifter need to be used in conjunction with half-bridge drivers in these topologies but adds propagation delay, delay matching, and components

• Good isolated gate driver (size, performance, cost) can be the optimum solution in these applications
Thank you

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