Cosmic radiation effects on electronics and how to pick the right part

Kirby Kruckmeyer,
Radiation Effects and Applications Engineer
Agenda

Taken from TI’s “Radiation handbook for electronics”
www.ti.com/radbook

Talk will focus on space radiation effects

- **Destructive radiation effects**
  - TID, SEL, SEGR and Displacement Damage

- **Non-destructive radiation**
  - SET, SEFI and SEU

- **Risks of using COTS for space applications**

- **Radiation misconceptions**
  - SOI, epi, datecode, process control
Kirby Kruckmeyer

• Coauthor of TI’s Radiation handbook for electronics
• Applications and radiation engineer in TI HiRel group
• Experience
  – Came to TI from National acquisition in 2011
  – Radiation testing and qualification
  – Rad hard wafer processing
  – Mil/aero manufacturing, testing and qualification
• Previous experience
  – Bipolar and CMOS wafer processing
  – Automotive Q100 product development and qualification
• Name etched on wafer floating in space
Space radiation environment

Natural

- **Sources**
  - Cosmic rays from outside our solar system
  - Solar radiation
  - Particles trapped in the radiation belts
- **Particles**
  - Electrons
  - Low energy protons
  - High energy protons
  - Heavy ions
- **Exposure variables**
  - Orbit
  - Solar activity

Man made

- **Sources**
  - Nuclear detonation
- **Particles**
  - Neutrons
  - Photons
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TID – total ionizing dose

- Dielectric (oxide, nitride, etc.) charging and surface states at oxide/silicon interface
- Increased leakages and soft breakdowns; impacts
  - supply current
  - input parameters (bias current, offset voltage)
  - response time
  - output voltage
  - linearity
  - functionality
- Can be shielded to some extent
  - adds weight and cost
  - not 100% mitigation

TID units

• The units for TID are rad
  – rad(Si) for silicon based products
  – rad = “Radiation Absorbed Dose” (CGS units)
  – dose causing 100 ergs of energy absorbed by 1 g of matter

• 1 krad = 1000 rad
  – krad(Si) are most common units for electronics

• 1 Gy = 100 rad
  – Grey are in SI units
  – Gy is most commonly used in medical applications
TID testing

• Device under test (DUT) electrically tested
  – per datasheet or SMD
• DUT exposed to gamma rays
  – Cobalt-60 source
  – Radioactive decay of Co-60 emits gamma rays
  – DUT powered up while being irradiated
• Post irradiation:
  – DUT retested
• RLAT: radiation lot acceptance testing
  – Either wafer or wafer lot

TI’s HDR TID test system
ELDRS – enhanced low dose rate sensitivity

- Standard radiation test is an accelerated test
  - High dose rate (HDR): 50 to 300 rad/s
  - Less than 6 minutes to reach 100 krad
  - Space systems can take 10 years to reach 100 krad

- ELDRS discovered in 1990
  - Some bipolar linear products degraded more when lower dose rate used to attain same TID
  - Sometimes worse case when DUT unbiased during irradiation
  - Old way of testing (HDR biased) not valid for some products going into space environment

- Risk with classic linear bipolar
  - Not a risk for CMOS, digital or SiGe

HDR = high dose rate (50 to 300 rad/s)
LDR = low dose rate (0.01 rad/s)
ELDRS characterization and testing

- Bipolar linear products are now characterized for ELDRS
  - Some units irradiated at HDR (50 to 300 rad/s)
  - Some units irradiated at LDR (0.01 rad/s)
  - Results compared
  - If more drift at LDR, product is said to have ELDRS
    - RLAT must be done at LDR
    - If product does not show significantly more drift at LDR the part is considered ELDRS-free
    - RLAT done at either LDR or HDR
  - Testing to 100 krad at LDR (0.01 rad/s) takes almost 6 months
  - TI does RLAT on classic bipolar products (LM124, LM139, LM117, etc) at LDR even though the products are ELDRS-free
SEE – single event effects

• In space, a single heavy ion or high energy proton impacts a device
  – On earth can be caused by neutrons (not covered in this talk)

• Ion generates electron-hole pairs
  – Can cause non destructive effects
    SEU – single event upset
    SET – single event transient
    SEFI – single event functional interrupt
  – And destructive effects
    SEL – single event latch-up
    SEGR – single event gate rupture
    SEB – single event burnout
    SEDR – single event dielectric rupture

• Typically cannot be shielded
Single event on Qantas Flight 72


Single subatomic event has human-scale impact!
Examples of single events in space

Green spot is from an SEU on the Level-0 Landsat 7 Enhanced Thematic Mapper Plus (ETM+)
https://landsat.usgs.gov/single-event-upset-seu

SEUs on Image magnetosphere imaging satellite. It is believed that the satellite lost signal due to an SEU.
https://image.gsfc.nasa.gov/
SEL – single event latch-up

• Perhaps, SEE of most concern
  – Most CMOS products at risk and it can be destructive

• An ion strike turns on parasitic PNPN structure like a silicon controlled rectifier (SCR)
  – SCR will stay turned on until part is powered down
  – Draws more current than circuit design
  – Can cause product to malfunction
  – Can impact product life
  – Eventually will destroy device (can be less than one second)

• Some CMOS products inherently immune
  – Depends on design and/or technology node
  – Won’t know without testing or an intimate knowledge of design and process

• Unlikely in bipolar products (junction isolated)
  – TI will test new products anyway

• Mitigation for non rad hard ICs: redundancy and/or detect and reset circuits
  – Adds complexity, weight, and system downtime
SEFI – single event functional interrupt

- An ion strike causes a part to go into a different state
  - different effects
- **Product that is programmed:**
  - control register bit can flip causing the part to go into a different configuration
  - may be necessary to reprogram the part
- **Product with a reset circuit:**
  - ion strike may cause the part to go into reset
  - some will recover on their own,
  - some may need to be reconfigured after reset
- **Product with an off pin:**
  - part could go into the off state
- **Mitigation: periodic register scrub**
  - Additional resources needed; system downtime
SEU – single event upset

- Flipping of a digital bit from 1 to 0 or 0 to 1
  - At one time, SEU was used to describe any nondestructive SEE, such as transients or SEFI
    • Still may see this confusion

- Almost all products with a digital outputs will have SEUs under heavy ion testing
  - Need to determine probability of it occurring and energy required
  - Some products might not have SEUs with lower energy ions or with protons
  - Some products could be SEU immune for certain orbits
SET – single event transient

- An ion strike causes a transient on a analog output
  - This is called SEU in older papers
- Almost all analog products will have SETs under the right (wrong) operating conditions
- SETs highly dependent upon the operating conditions
  - Regulator: input voltage and output voltage, current and capacitance
  - Opamp: configuration, supply voltage, differential input, feedback loop, etc.
- Mitigation: operating and application conditions
Destructive SEEs

SEB – single event burnout

SEGR – single event gate rupture
  – SEB and SEGR are two different mechanisms but difficult to distinguish from one another
  – Concern for power MOSFETs
  – Gate oxide can be damaged from an ion strike
  – Voltage and current dependent
    • Commercial products must be derated for space missions
    • TI space products already characterized; derating not needed

SEDR – single event dielectric rupture
  – Similar to SEGR but on non power devices such as capacitor oxides
SEE testing

- **Heavy ion testing conducted at a cyclotron**
  - Only a few facilities in the US and in Europe; beam time can be hard to get
  - Cost: $1000 to $4000 per hour of beam time
  - Testing a product takes between 4 to 24 hours or more of beam time
  - Additional costs/time for test setup and analyzing data

- **Proton testing done at similar facilities but other accelerators may be used**

- **DUT delidded to expose die to beam**
  - Most facilities beams cannot penetrate packaging
  - Challenge for flipchips

- **DUT powered up and operating during testing**

- **Monitor part performance during beam run**
  - Supply current for SEL
  - Output for SEU or SET
  - Part functionality for SEFI

TI PXI SEE test board at TAMU cyclotron
SEE test results

- **LET** = linear energy transfer
  - amount of energy deposited in silicon by an ion
  - will be different for different ions
  - Units: MeV-cm$^2$/mg (sometimes shortened to MeV)

- **Record**
  - Fluence = number of ions shot at DUT during beam run
    - Units: #ions/cm$^2$
  - Number of errors during beam run

- **Calculate cross section**
  - Number of errors/fluence
    - Units: cm$^2$

- **Plot cross section vs LET**

- If LETs below 14 MeV-cm$^2$/mg it may be necessary to do proton testing
**SEE data analysis**

- **Fit Weibull curve to data**

\[ F(L) = A \left( 1 - \exp \left\{ - \left[ \frac{L - L_0}{W} \right]^s \right\} \right); \quad L > L_0 \]

\[ F(L) = 0; \quad L < L_0 \]

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<th>Symbol</th>
<th>Parameter</th>
<th>SEFI 2</th>
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<td>A</td>
<td>Saturated cross section</td>
<td>8.7E-06</td>
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<tr>
<td>L_0</td>
<td>Onset LET</td>
<td>48</td>
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<tr>
<td>W</td>
<td>Width</td>
<td>9</td>
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<td>s</td>
<td>Fit</td>
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- **Weibull fit parameters used to determine probability of SEE for a certain orbit**

<table>
<thead>
<tr>
<th>ORBIT TYPE</th>
<th>ONSET LET (MeV-cm²/mg)</th>
<th>CREME96 INTEGRAL FLUX (/day–cm²)</th>
<th>( \sigma_{\text{sat}} ) (cm²)</th>
<th>EVENT RATE (/day)</th>
<th>EVENT RATE (FIT)</th>
<th>MTBE (years)</th>
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<tr>
<td>LEO(ISS)</td>
<td>48.0</td>
<td>4.5E–04</td>
<td>8.7E–06</td>
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<td>1.3E–08</td>
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<td>0.53</td>
<td>2.1E+05</td>
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**MTBE – Mean time between event**
Protons in space can cause damage to the silicon lattice
  – This can cause traps that tie up carriers (electrons and holes)
  – Can also cause leakages

Dependent upon feature size and active junction depths
  – Some bipolar parts fail below $1 \times 10^{12}$ n/cm$^2$
  – CMOS tend to survive greater than $1 \times 10^{13}$ n/cm$^2$
  – Many programs with DDD requirements do not bother to test CMOS products

Test method
  – Stick bag of parts in neutron reactor
  – Wait to cool down
  – Electrically test units
  – Neutrons used instead of protons as protons also have TID effects
Prompt dose – flash x-ray

- Nuclear detonation can cause flash of high energy photons
  - The dose rate many orders of magnitude higher than used for TID testing
- Flash can cause photocurrents within a device
- The photocurrents cause effects similar to SEEs
  - Multiple effects can occur at once
- Also known as “dose rate” testing
  - Not to be confused with LDR/HDR TID testing
- Testing similar to heavy ion testing
  - DUT is powered up and operating and monitored
  - DUT is exposed to a flash x-ray
- Results highly dependent upon the operating conditions at the time of the flash
- Suppliers typically do not test
  - Dose rate and operating conditions usually classified
RHA - radiation hardness assurance

- RHA products tested and qualified to specific TID level
- Each lot goes through TID radiation lot acceptance testing (RLAT)
  - RLAT can be done on a wafer lot or a single wafer
  - RLAT either LDR or HDR depending upon the technology
  - TID report available for each lot
- RHA is TID only and does not cover the other radiation effects
  - Per mil standard definition
  - TI goes beyond the definition and tests for other radiation effects
- TID level shown in the SMD (5962) number
Test and mil standards, SMDs and DLA

- **MIL-PRF-38535** – how to manufacture, quality and test mil and space products
  - Replaced MIL-I-38510

- **MIL-STD-883** – test methods for meeting MIL-PRF-38535
  - TM1019 – TID test method

- **SMD** – standard microcircuit drawing
  - DOD datasheet
  - Contains electrical specifications; no app info (see TI datasheet)

- **DLA** – Defense Logistics Agency – Land and Maritime
  - Formally known as DSCC and DESC
  - Owner of SMDs and mil standards
SMD PIN – Part identification number

5962R9950402VCA

- Radiation rating:
  - R = 100 krad
  - P = 30 krad
  - L = 50 krad
  - F = 300 krad

- Year SMD started:
  - 99 = 1999

- Device number:
  - 02 = device ID 02
  - To distinguish part from other variants
  - In this SMD, 02 indicates ELDRS-free

- Grade:
  - V = Space
  - Q = Mil
  - Y = Space in non-hermetic ceramic package
  - S = Space; B = Mil in old 38510 system

- Package:
  - C = CDIP
  - D = CFP
  - Z = gullwing

- Lead finish:
  - A = SnPb
  - C = Au

- Letter is not universal
  - 9 = die
TI’s space grade product family (-SP)

• Manufactured, tested and qualified per QML-V flow of MIL-PRF-38535
  – Tri-temp tested
  – 100% burn-in
• Hermetic packaging with no matte Sn lead finish
• Mil temp range of -55°C to +125°C
• RHA – Radiation hardened
  – RHA and RLAT to the specified level (30, 50, 100 or 300 krad)
  – ELDRS-free or characterized
  – SEL immune to the specified level (>60 MeV-cm²/mg)
  – Other SEE characterized; reports available
  – DDD testing on new products
  – All new space products and most older products
    • some older space releases might not be RHA
## TI’s Range of Solutions

<table>
<thead>
<tr>
<th></th>
<th>Commercial</th>
<th>Q100</th>
<th>EP</th>
<th>QMLQ</th>
<th>SEP</th>
<th>QMLV</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Packaging</strong></td>
<td>Plastic</td>
<td>Plastic</td>
<td>Plastic</td>
<td>Ceramic</td>
<td>Plastic</td>
<td>Ceramic</td>
</tr>
<tr>
<td><strong>Single Controlled Baseline</strong></td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Bond Wires</strong></td>
<td>Au/Cu</td>
<td>Au/Cu</td>
<td>Au</td>
<td>Al</td>
<td>Au</td>
<td>Al</td>
</tr>
<tr>
<td><strong>Is Pure Sn used?</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td><strong>Production Burnin</strong></td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Typical Temperature Range</strong></td>
<td>-40°C - 85°C</td>
<td>-40°C - 125°C</td>
<td>-55°C - 125°C (majority)</td>
<td>-55°C - 125°C</td>
<td>-55°C - 125°C</td>
<td>-55°C - 125°C</td>
</tr>
<tr>
<td><strong>Radiation (SEL/SEE)</strong></td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Radiation (TID) Lot Acceptance (RLAT)</strong></td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td><strong>Lot Level Temp Cycle</strong></td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Group D</td>
<td>Lot Level</td>
<td>Group D</td>
</tr>
<tr>
<td><strong>Lot Level HAST</strong></td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>N/A</td>
<td>Yes</td>
<td>N/A</td>
</tr>
<tr>
<td><strong>Life Test Per Wafer Lot</strong></td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

**Quality / Reliability / Cost**

- TI’s Range of Solutions
- Quality
- Reliability
- Cost
Radiation risks for commercial (COTS) and Q100

- Most CMOS products at risk for SEL
- Power products can have SEGR or SEB and may need derating
- TID levels are unknown for most products and technologies
- Bipolar linear products might have ELDRS, making HDR test results invalid for space
- Radiation sensitivity can be highly dependent upon design
  - Two products on the same process can have different rad responses
- Semiconductor suppliers cannot share intimate details about process or design
  - Proprietary information that gives supplier competitive advantage
- Lot to lot variations can impact rad response
- Radiation testing is costly and time consuming
- Myths are out there
  - Epi or SOI does not mean SEL immunity
  - Datecode does not provide useful lot information
Epi does not guarantee SEL immunity

- One method of radiation hardness involves using an epi substrate
  - This is a highly engineered process and epi is just a part
  - Most commercial CMOS processes use epi but still have SEL

- Most CMOS processes use a p- substrate with p- epi grown on top
  - For SEL hardening to work, substrate must be p+
  - Using to a p+ substrate can impact the performance of some products

- epi must be thin enough to prevent SCR from turning on
  - Required epi thinness is typically thinner than standard substrates
  - Thinning the epi can cause performance problems such as lowering the well breakdown voltage
  - Much engineering work goes into developing the rad hard process

K. LaBel et al., “Single event effect characteristics of CMOS devices employing various epi-layer thicknesses”, RADECS, Sept. 1995, pp. 258-262
SOI does not guarantee SEL immunity

- **SOI – Silicon on insulator**
  - The active area of device sits on a buried oxide layer (BOX)
- **Deep trench isolation (DTI)**
  - If isolation trench is deep enough to reach down to the BOX, structure cannot have SEL
- **Shallow trench isolation (STI)**
  - If isolation trench does not reach BOX, SEL is still a risk
  - Common in BiCMOS to use DTI for bipolar and STI for CMOS

![Diagram showing DTI isolating N and P wells, preventing SEL](image1)

![Diagram showing STI not deep to isolate N and P wells, SEL still a risk](image2)
Micro SELs are not safe

- Modern, complex CMOS products can have micro SELs
  - A latch-up event causes a small rise in current
  - Current is limited either by power supply to latched circuit or size of the SCR
  - Part remains mostly functional
  - Part runs several minutes until power reset without apparent damage
  - Common to see multiple small rises in current

- Product life risk
  - Area that is latched can draw more current than designed for
  - Latched circuit will eventually fail after repeated events
Process variation vs. radiation

• Wafer fab controls are to maintain consistent electrical performance and quality
  – Different variables impact radiation performance

• Variables impacting TID
  – Passivation stack and stoichiometry
  – Field oxide processes
  – Metal alignment
  – Surface doping levels

• Variables impacting SEE
  – Substrate parameters
  – Epi thickness
  – Junction profiles
  – Die layout
Process variation impact on SEL

Typical process control

- EPI thickness \((\pm 20\%)\)
- EPI doping \((\pm 20\%)\)
- Substrate doping \((\pm 33\%)\)
- EPI and substrate doping impact effective EPI thickness

\[
\rho_{EPI} = 5.8 - 8.4 \ \Omega \cdot \text{cm}
\]
\[
\rho_{sub} = 0.01 - 0.02 \ \Omega \cdot \text{cm}
\]

**CAN Exhibits SEL based on 0.5um variation**

<table>
<thead>
<tr>
<th>EPI (um)</th>
<th>Temp</th>
<th>LET</th>
<th>SEL</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.5</td>
<td>25</td>
<td>85</td>
<td>No</td>
</tr>
<tr>
<td>9.5</td>
<td>125</td>
<td>85</td>
<td>No</td>
</tr>
<tr>
<td>10</td>
<td>25</td>
<td>85</td>
<td>Yes</td>
</tr>
<tr>
<td>10</td>
<td>125</td>
<td>60</td>
<td>Yes</td>
</tr>
</tbody>
</table>

To ensure SEL immunity of SN65HVD233-SP EPI process must be controlled tighter than typical commercial process.
# LM108 TID variations

<table>
<thead>
<tr>
<th>LM108</th>
<th>HDR TID (krad)</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lot #1</td>
<td>100</td>
<td>Pass</td>
</tr>
<tr>
<td>Lot #2</td>
<td>30</td>
<td>Pass</td>
</tr>
<tr>
<td>Lot #3</td>
<td>10</td>
<td>Fail</td>
</tr>
</tbody>
</table>

Lot #1 and #3 processed one month apart

<table>
<thead>
<tr>
<th>LM108</th>
<th>LDR TID (krad)</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer #2</td>
<td>80</td>
<td>Pass</td>
</tr>
<tr>
<td>Wafer #3</td>
<td>50</td>
<td>Pass</td>
</tr>
<tr>
<td>Wafer #15</td>
<td>30</td>
<td>Pass</td>
</tr>
</tbody>
</table>

Three wafers from the same lot
Commercial/automotive manufacturing flow

- Many products manufactured in multiple wafer fabs
  - Allows manufacturing flexibility
  - Fab transfers and closures
- Equipment and processing not the same in each fab
- Sometimes radical changes during fab transfers
  - Die shrink
  - Process topography
- Differences can impact rad performance
  - Different passivation tools have different TID response
  - Junction profiles changes will impact SEE response
Process changes and transfer impacts

- **Unitrode (UC18xx-SP) fab transfer**
  - 50 krads $\rightarrow$ 5 krads

- **Introduction of nitride**
  - Excellent moisture barrier for improved quality on plastic packaged parts
  - 100 krads $\rightarrow$ 10 krads and causes ELDRS

- **LM139 quad comparator transfer and die shrink**
  - Output transient impact
  - TID impact
    - Channel 1: 10 krads
    - Channel 2: 80 krads
    - Channel 3: 100 krads
    - Channel 4: 80 krads

![Graph showing amplitude vs time for old and new parts after die shrink](chart.png)
Commercial Flow (real example: SN74HC138)

3-Line To 8-Line Decoders/Demux

Commercial Process Variables
3 active wafer fabs

- TI SFAB in Sherman, Texas
- ATC (subcontractor) in Hsinchu, Taiwan
- ASMC (subcontractor) in Shanghai, China

Each wafer fab runs a similar BUT NOT identical baseline

- Glassivation (protective overcoat)
- Base silicon wafers (vendor and doping spec)
- EPI versus non-EPI (doping profile/yield)
- Diffusion and metal profiles
- Process equipment
- Process recipes
- Process control limits
Commercial Flow (real example: SN74HC138)

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- Process equipment
- Process recipes
- Process control limits

Commercial Assembly Baseline Flows
3 assembly/test sites
- TI Mexico
- TI Taiwan
- ALP (subcontractor) in Thailand

Each assembly site runs a similar BUT NOT identical baseline
- Lead-frame source and geometries
- Mold compound (encapsulant)
- Mount compound (die attach)
- Wire bonder type and profile
- Wire type and other materials
- Injection mold press type and profile
Datecode tells you nothing

- Four digit datecode is the date product was assembled
  - Encapsulated in plastic for commercial products
  - Lid sealed for hermetic packages
- Datecode has no wafer lot information for commercial/automotive products
  - Wafers can be stored for years before being assembled
  - One datecode is likely to be assembled from more than one wafer
  - One datecode can include different wafer lots
  - One datecode could have units that came from different wafer fabs
Summary

• Many radiation effects in space that can impact product’s life and performance
• Predicting a product’s radiation response requires intimate knowledge of design and process
  – Usually not available to customers
• Choosing and testing parts can be expensive and time consuming
• Standard commercial/automotive fab variations can impact product rad performance
• Customer has no insight into lot variations
  – Datecode does not provide meaningful wafer lot information
• No guarantee that product used will have same performance as units tested
• TI space products are tested and qualified up front
  – We do the testing and verification so you don’t have to
Online technical training from Texas Instruments…

**ti.com/space**
Just type that into any browser!

**Radiation handbook for electronics**
[www.ti.com/radbook](http://www.ti.com/radbook)

**Aerospace & Defense Training Series – Available Now**
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Visit the technical documents tab of the –SP product pages on ti.com