PLL Building Blocks Part 1
TI Precision Labs – Clocks and Timing

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Prepared by Liam Keese
Phase lock loop (PLL) block diagram
Voltage controlled oscillator (VCO)
**VCO resonator**

\[ f = \frac{1}{2\pi \sqrt{L \cdot C}} \]

- \( f \) = resonant frequency
- \( L \) = inductance
- \( C \) = capacitance

\[ \tau = 2\pi \sqrt{\frac{L}{g}} \]

- \( \tau \) = period
- \( L \) = length of the pendulum
- \( g \) = acceleration due to gravity
The real-world inductor

\[ Q_L(f) = \frac{X_L}{R_L} = \frac{2\pi f L}{R} \]
Now add the stimulus

Amplified signal from emitter is lightly coupled into the circuit to sustain oscillation
Example VCO circuit
VCO tuning range

Switched Capacitor Bank

C_{Varactor} \quad C_{Fixed} \quad C \quad 2C

Traditional VCO
Silicon VCO (Band 3)
Silicon VCO (Band 2)
Silicon VCO (Band 1)
Silicon VCO (Band 0)

Overlap

Tuning voltage

frequency

\( f_{Max} \)

\( f_{Min} \)

\( V_{Min} \)

\( V_{Max} \)
Phase lock loop overview

Reference Oscillator

R Divider

Phase Detector/Charge Pump

Loop Filter

VCO

Output Divider

Reference

Divider Reference

Oscillator

1/N

1/D

Output

 Divider

K_{PD}

Z(s)

1/N

N Divider

f_{OSC}

f_{N}

f_{PD}

f_{VCO}

f_{OUT}
High-frequency feedback (N) divider

- N counter value
  \[ N = \frac{f_{\text{VCO}}}{f_N} = \frac{f_{\text{VCO}}}{f_{\text{PD}}} \]
- Input to this counter can be high frequency
- Prescalers are typically inside this counter
High frequency feedback (N) divider

Single Modulus Prescaler
High-frequency feedback (N) divider

- Dual modulus prescaler
  - \( N = A \times (P+1) + (B-A) \times P = P \times B+A \)

### Prescaler Table

<table>
<thead>
<tr>
<th>Prescaler</th>
<th>Minimum Continuous Divide</th>
</tr>
</thead>
<tbody>
<tr>
<td>4/5</td>
<td>12</td>
</tr>
<tr>
<td>8/9</td>
<td>56</td>
</tr>
<tr>
<td>( P/(P+1) )</td>
<td>( P \times (P-1) )</td>
</tr>
</tbody>
</table>
Fractional dividers (Simple 1st order modulator)
Fractional dividers (Simple 1st order modulator)

Fractional divide timing error

<table>
<thead>
<tr>
<th>Phase Detector Cycle</th>
<th>Accumulator (Cycles)</th>
<th>N Value</th>
<th>Time for Rising Edge for Dividers (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.2</td>
<td>900</td>
<td>999.7778</td>
</tr>
<tr>
<td>2</td>
<td>0.4</td>
<td>900</td>
<td>1999.5557</td>
</tr>
<tr>
<td>3</td>
<td>0.6</td>
<td>900</td>
<td>2999.3335</td>
</tr>
<tr>
<td>4</td>
<td>0.8</td>
<td>900</td>
<td>3999.1113</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>901</td>
<td>5000.0000</td>
</tr>
</tbody>
</table>
Fractional dividers (High-order modulators)

<table>
<thead>
<tr>
<th>Delta-Sigma Order</th>
<th>Delta-Sigma Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0, 1</td>
</tr>
<tr>
<td>2(^{nd})</td>
<td>-1, 0, 1, 2</td>
</tr>
<tr>
<td>3(^{rd})</td>
<td>-3, -2, -1, 0, 1, 2, 4</td>
</tr>
<tr>
<td>4(^{th})</td>
<td>-7, ..., +8</td>
</tr>
<tr>
<td>(k)^{th}</td>
<td>(-2^{k-1}, ... , 2^{k})</td>
</tr>
</tbody>
</table>
Fractional dividers performance \( (f_{PD} = 10 \text{ MHz}) \)

Spur and Fractional Noise Shaping

Spur Example for fraction of 1/10

Graphs showing the performance of fractional dividers with various noise shaping techniques.
To find more clocks and timing technical resources and search products, visit ti.com/clocks
1. True or False:

The relationship between $f_{VCO}$ (VCO frequency), $f_{PD}$ (phase detector frequency), $f_n$ (N divider output frequency) is $f_{VCO}/f_N = f_{VCO}/f_{PD} = N$
1. **True** or False:

The relationship between $f_{\text{VCO}}$ (VCO frequency), $f_{\text{PD}}$ (phase detector frequency), $f_n$ (N divider output frequency) is $f_{\text{VCO}}/f_n = f_{\text{VCO}}/f_{\text{PD}} = N$.
Short Quiz

2. Choose one:

Which techniques can be used to increase VCO tuning range?
(a) Fractional N divider
(b) Switchable capacitor or inductor array
(c) Output divider
2. Choose one:

Which techniques can be used to increase VCO tuning range

(a) Fractional N divider

(b) Switchable capacitor or inductor array

(c) Output divider
3. True or False:

A fractional N modulator decreases the noise generated at higher frequencies.
3. True or False:

A fractional N modulator decreases the noise generated at higher frequencies
4. Choose all that apply:

Which of below statements apply when using a dual modulus prescaler?

a) Counter will divide by (P+1) A times
b) B < A
c) N= P x B+A
Short Quiz

4. Choose all that apply:

Which of below statements apply when using a dual modulus prescaler?

a) Counter will divide by \((P+1)\) A times
b) \(B < A\)
c) \(N = P \times B + A\)