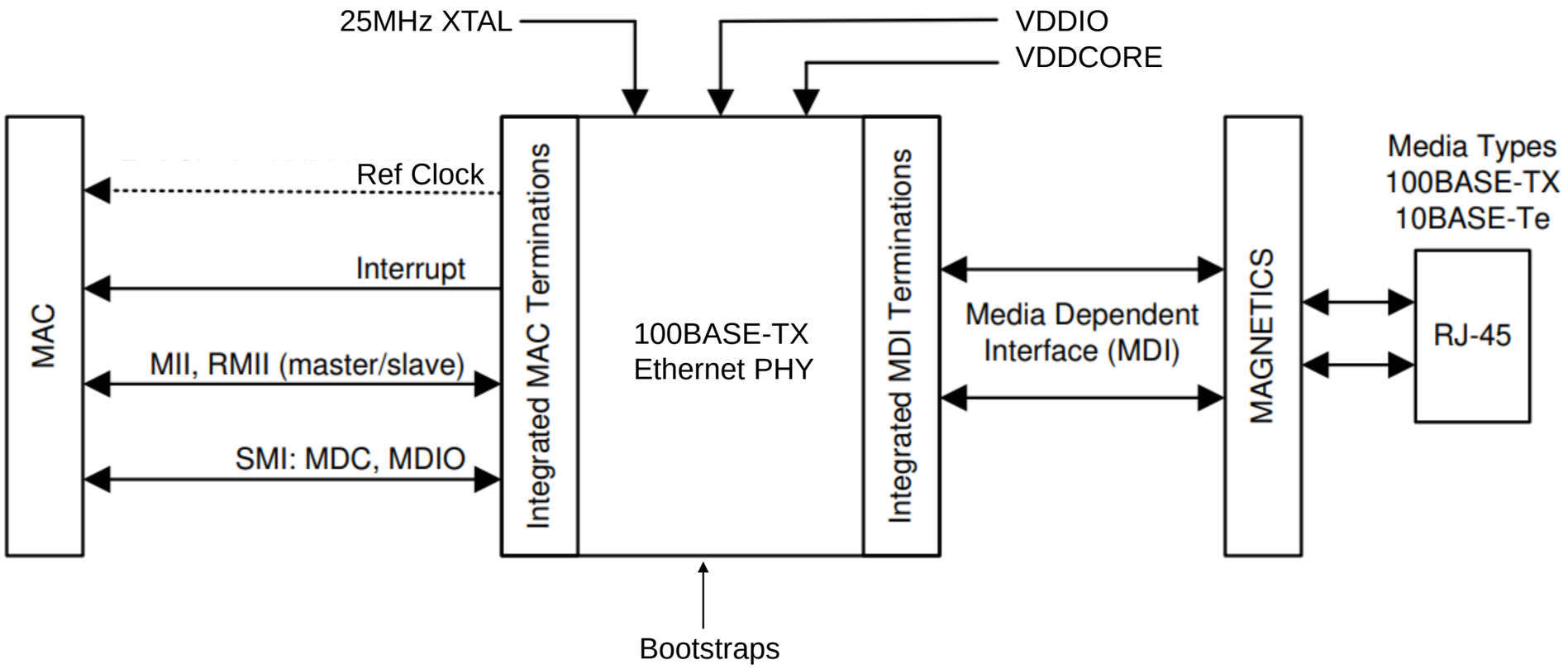
# Schematic Design Guide for 100BASE-TX Ethernet PHYs

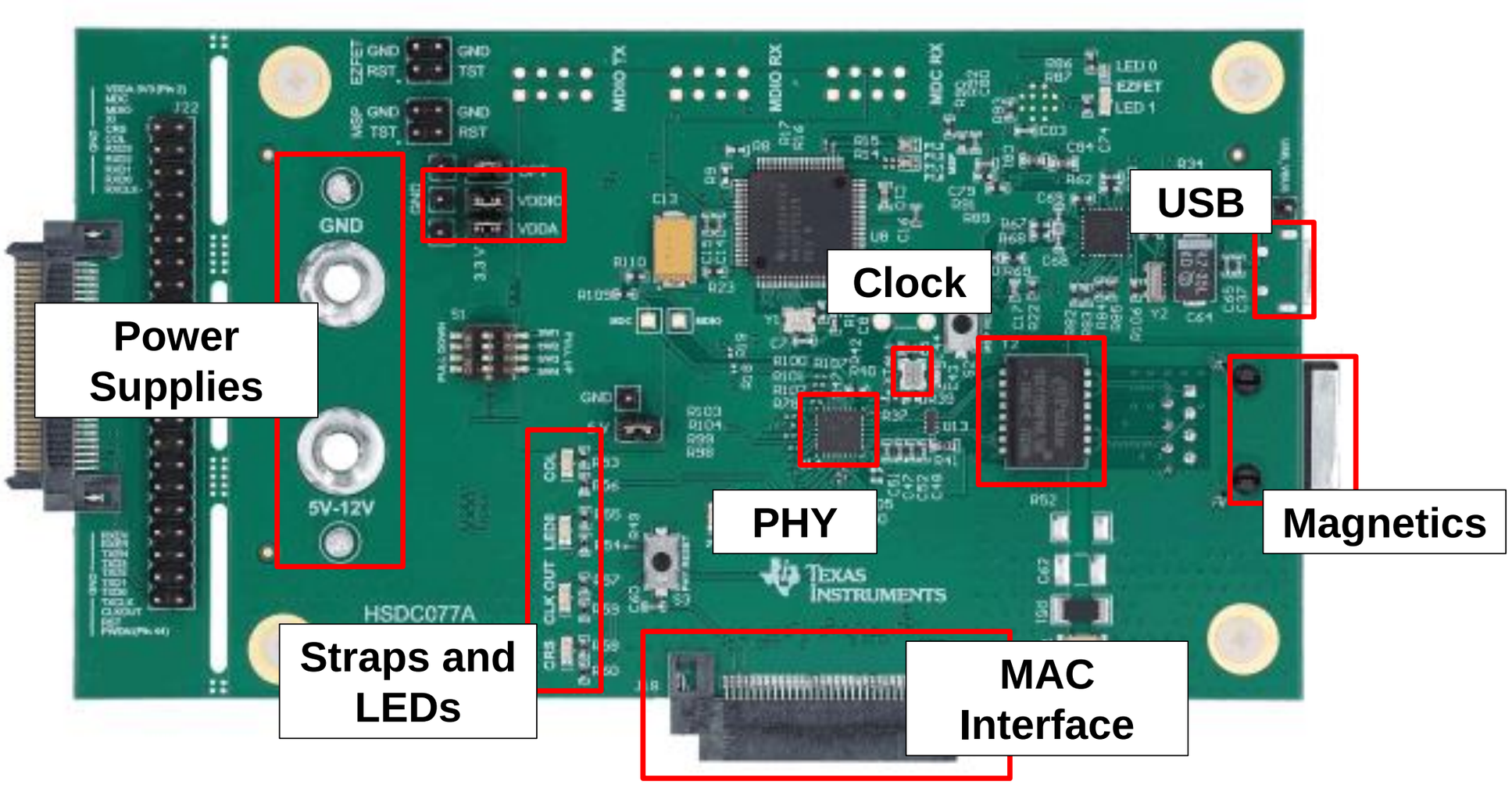
## TI Precision Labs - Ethernet

**Prepared and presented by Cecilia Reyes**

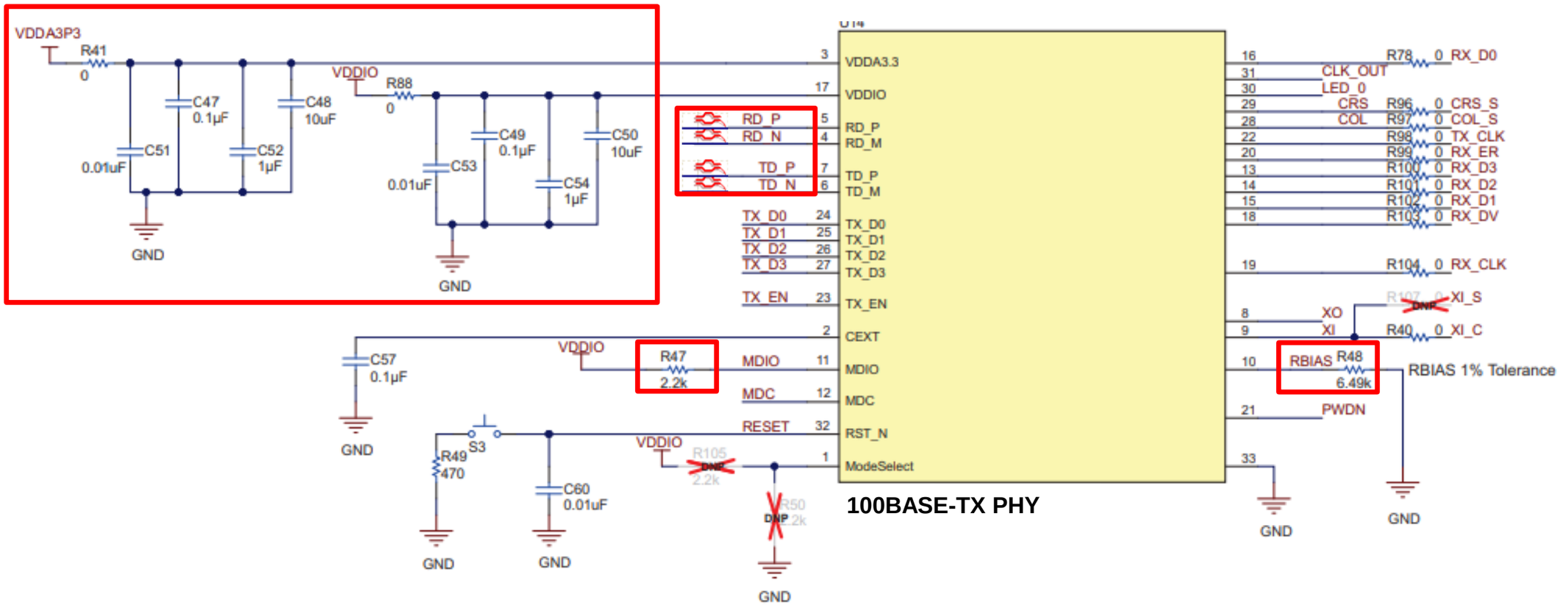
# Introduction and typical block diagram



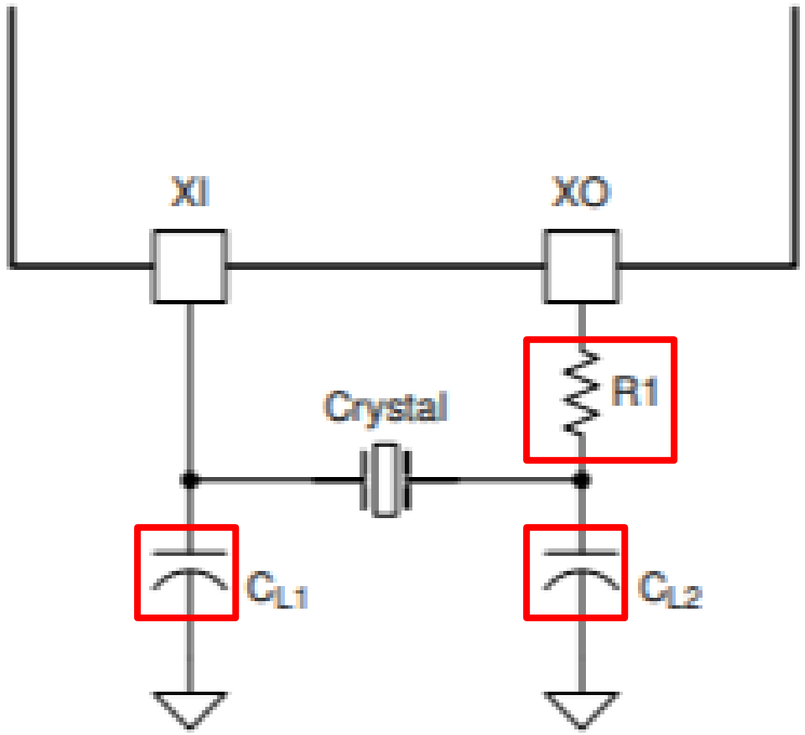
# Schematic requirements – where to focus



# Schematic requirements – PHY



# Schematic requirements




**Clock**

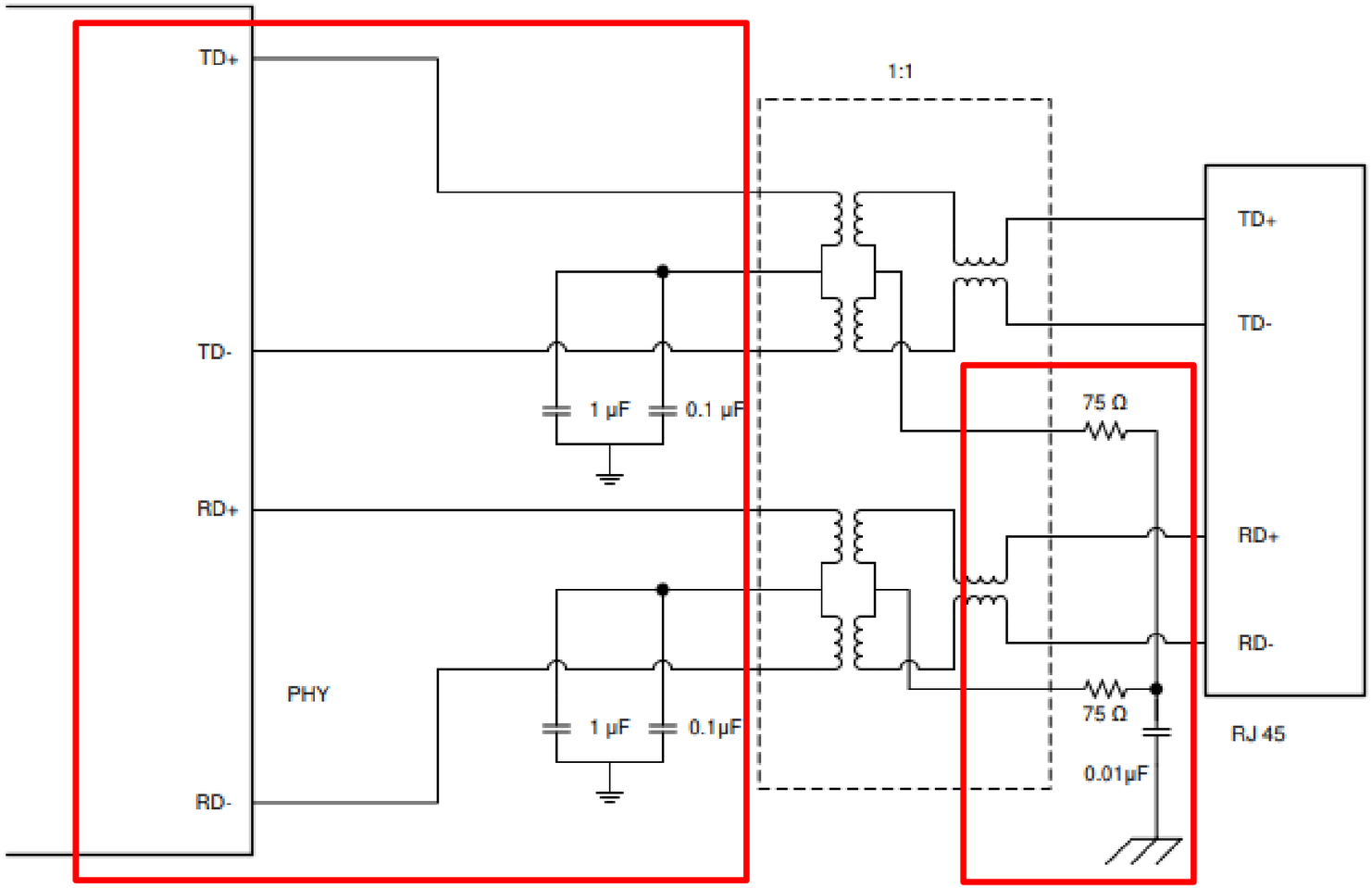
Important specs to consider:

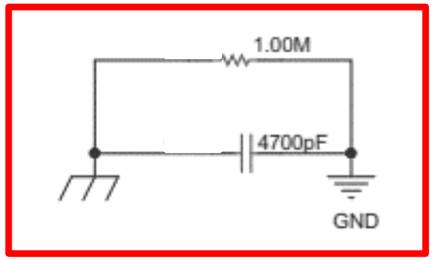
- frequency tolerance
- stability
- load capacitance

MAC requirements for clock speeds:

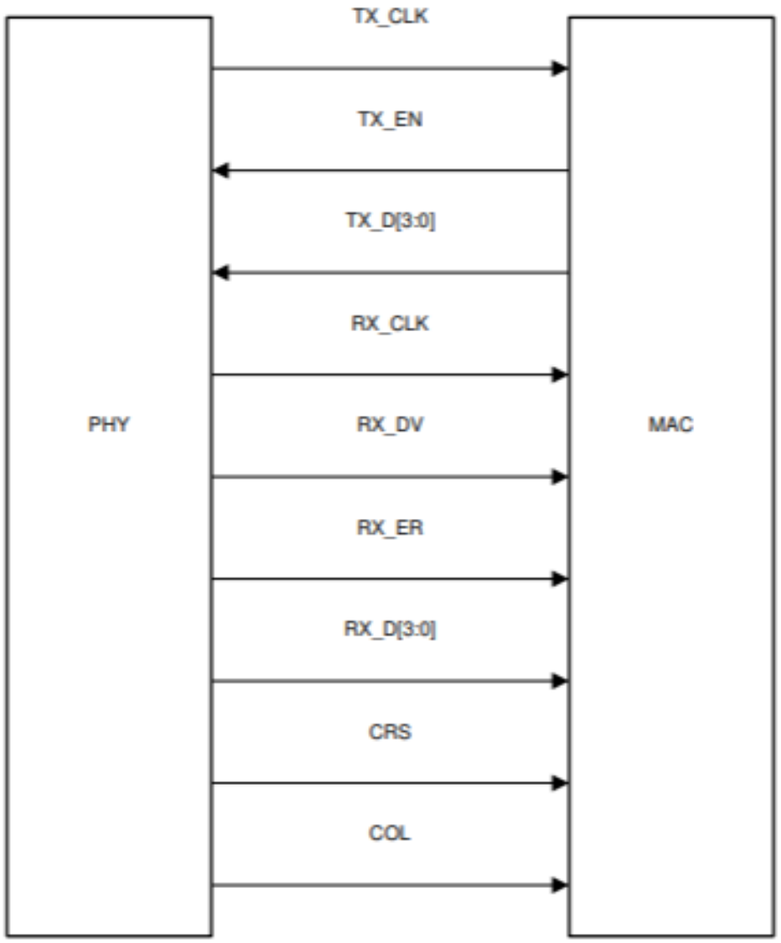
- MII mode: 25MHz input
- RMII Master mode: 25MHz input
- RMII Slave Mode: 50MHz input

# Schematic requirements – MDI



# Schematic requirements



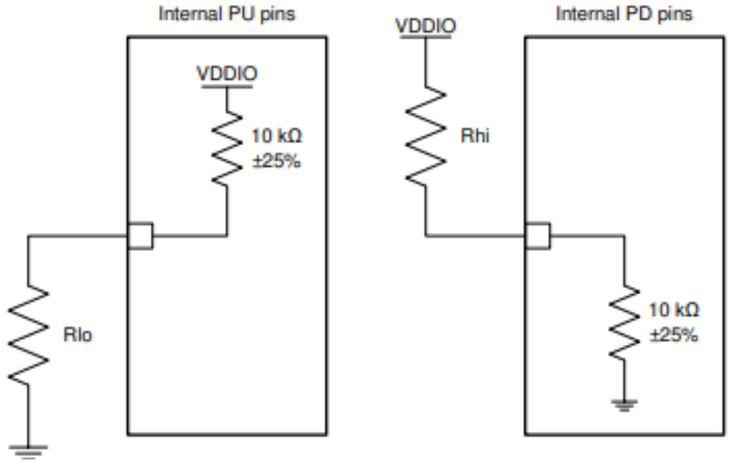

**Media Access Control (MAC) Interface**

Two interfaces:

- MII (media-independent interface)
- RMII (reduced media-independent interface)

PHY to MAC typically directly connected

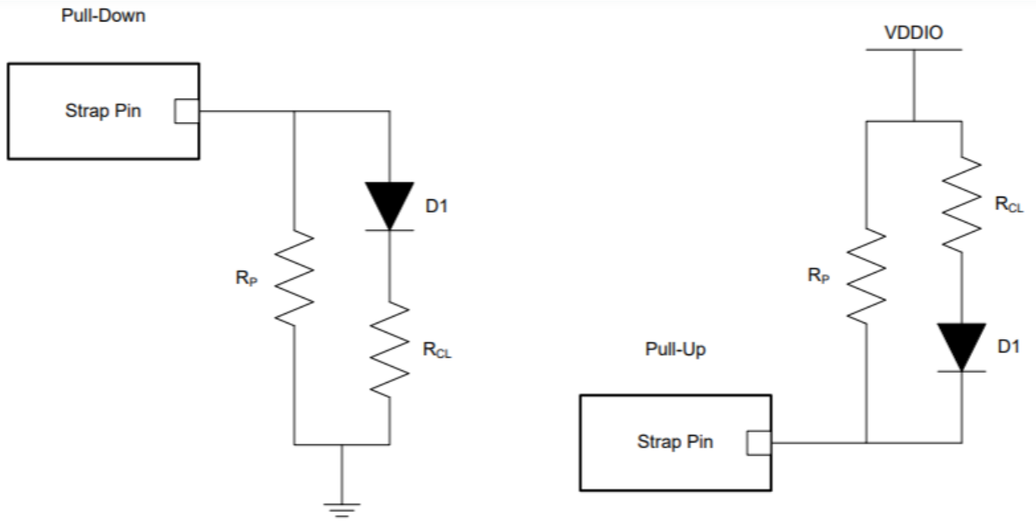
# Schematic requirements




| Mode (1) | SUGGESTED RESISTORS | |
|---|---|---|
| | $R_{HI}$ (kΩ) | $R_{LO}$ (kΩ) |
| **INTERNAL 10-kΩ PULLDOWN (PD) PINS** | | |
| 0-DEFAULT | OPEN | OPEN |
| 1 | 2.49 | OPEN |
| **INTERNAL 10-kΩ PULLUP (PU) PINS** | | |
| 0 | OPEN | 2.49 |
| 1-DEFAULT | OPEN | OPEN |

## Straps

- Internal pull up or pull down resistors depending on the pin on the PHY
- PU or PD resistors are used to change strap mode
- Polarity of LED will change automatically depending on strap mode



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